560 GHz f_t, f_{max} InGaAs/InP DHBT in a novel dry-etched emitter process

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Through the combined use of vertical and lateral device scaling, InP-based transistors will exceed THz bandwdiths and subsequently enable a new generation of mm-wave and sub-mm-wave systems. Such devices will be realized by continued lithographic, epitaxial, and contact resistance scaling [1]—where the specific challenges to DHBT scaling include emitter contact resistivity, fabrication of deep submicron emitter-base junctions, and continued thinning of the base-collector heterojunction grade. We report here the first device results from a newly developed deep sub-micron emitter DHBT process. This process employs TiW emitter contacts that show both low resistivity and high thermal stability [2], and dry etch techniques for formation of both the emitter contact and the emitter-base semiconductor junction. We report the first RF device results in this process at the 250nm emitter node, demonstrating record simultaneous bandwidths of 560 GHz for f_t and f_{max}. While not yet employed in an RF device, this process has shown the ability to produce emitter junctions ~ 100nm wide where the metal height is ≥ 600nm.

The semiconductor epitaxial stack consists of a 22nm $In_{0.53}Ga_{0.47}As$ base (doping gradient 9-5×$10^{19}cm^{-3}$) and a 70nm thick collector, T_c. To minimize the effects of the InGaAs/InP conduction band offset in the collector-base junction, a 5 nm InGaAs setback combined with a 11 nm InGaAs/InAlAs submonolayer superlattice grade is utilized. The setback and grade have been thinned compared with earlier UCSB designs [3]. The thinner setback and grade show a substantially higher breakdown voltage compared with otherwise identical collector design with a thicker setback and grade. All InAlAs layers in this grade are grown as 0.5 mono layers in order to form a quasi-quaternary InAlGaAs grade between the InGaAs setback and InP collector. The nominal collector doping of $N_d=2\times10^{17}cm^{-3}$ is designed to have an essentially fully depleted collector at $V_{cb}=0$. To form the emitter metal stack, a 5nm Ti, 500nm $Ti_{0.1}W_{0..9}$ layer is blanket sputtered on the wafer, 100nm thick SiO_2 is deposited by PECVD, and lastly 35nm Cr is deposited by e-beam evaporation. The SiO_2 protects the Ti/TiW during the subsequent dry etch steps, permitting easy removal of the Cr mask. The Cr layer is patterned by I-line lithography and the associated Cr dry-etch emitter mask formed by Cl_2/O_2 ICP etch. Using this technique, Cr line widths down to 150 nm are routinely obtained. Once the Cr-mask is formed, the SiO_2 and Ti/TiW stack is etched from the field using SF6/Ar ICP. A slight tapering of the TiW is observed, such that the TiW width increases by 50-100nm at the metal, semiconductor interface. To date, the smallest TiW emitter metal feature produced using this approach has been around 150nm. Narrower emitters can be realized in this III-V process by the use of electron beam lithography. To protect the ohmic contact and to improve adhesion, a 25 nm thick SiN_x sidewall is then formed using PECVD deposition followed by an CF_4/O_2 etch. Once the emitter contact has been formed, a 25nm thick SiN_x sidewall is then formed around the ohmic contact for its protection and to improve adhesion—using blanket PECVD deposition followed by an anisotropic CF_4/O_2 ICP etch. A low power Cl_2/N_2 ICP etch is then performed at 200°C to etch through the n^{++} InGaAs cap and is stopped inside the InP emitter layer. The protective SiO_2 and Cr layers are removed in a buffered-HF solution. Lastly, a short chemical wet-etch is used to complete the InP etch to the base in order to complete the formation of the emitter mesa. The reduced wet-etch time substantially improves emitter mesa undercut reproducibility, as well as unwanted excess InP undercut at the ends of the contact when compared with conventional semiconductor wet-etch processes utilized in a self-aligned base HBT processes. The remaining device features are formed in the same manner as the InP DHBTs previously reported from UCSB.

Standard TLM measurements show base $\rho_{sheet} = 780\ \Omega/\square$, and $\rho_c=15\ \Omega/\mu m^2$ and a collector $\rho_{sheet} = 12\ \Omega/\square$, and $\rho_c=10\ \Omega/\mu m^2$. $R_{ex} \sim 5\ \Omega/\mu m^2$ from RF extraction. The HBTs show $\beta \sim 20\text{-}25$, $BV_{ceo} \sim 3.3V$ and $BV_{cbo} \sim 3.8V$ ($I_{breakdown}=150\mu A/\mu m^2$, here defined as at 1% of the current at peak f_t,f_{max}). RF characterization was carried out at 1-67 GHz, after off wafer LRRM calibration. On wafer open and short pads identical to the ones used by the devices were used for de-embedding of pad capacitance and lead inductance. Single pole fits extract a maximum balanced f_t and f_{max} of 560 GHz, at a current density of $15mA/\mu m^2$ for an emitter area of $A_{je}=0.25\times5.5\mu m^2$, and a total collector area of $0.6\times6\mu m^2$. C_{cb}/I_c is a low 0.26pS. This is the first report of a device simultaneously having f_τ and f_{max} above 500 GHz. A longer device having $A_{je} = 0.25\times9.5\mu m^2$ demonstrated a peak f_τ = 600 GHz with f_{max} = 430 GHz. Due to the relative wide 250nm emitter junction, coupled with the thin 70nm collector, peak f_τ and f_{max} appears not to be limited by the Kirk effect. No increase in C_{bc} is observed as the current is increased beyond that of peak f_τ. Instead, the device performance is believed to be limited by excessive device self-heating. Continued lateral scaling of the emitter will allow for more efficient heat transfer and thus higher J_e and bandwidth.

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[1] *M. J.W. Rodwell et al.,* IEEE Trans. Electron Devices*, Vol. 48, No. 11, 2001, pp. 2606-2624*

[2] *A. M. Crook, submitted to Applied Physics Letters*

[3] *Z. Griffith et al.,*IPRM*,, 2006, pp. 96-99*

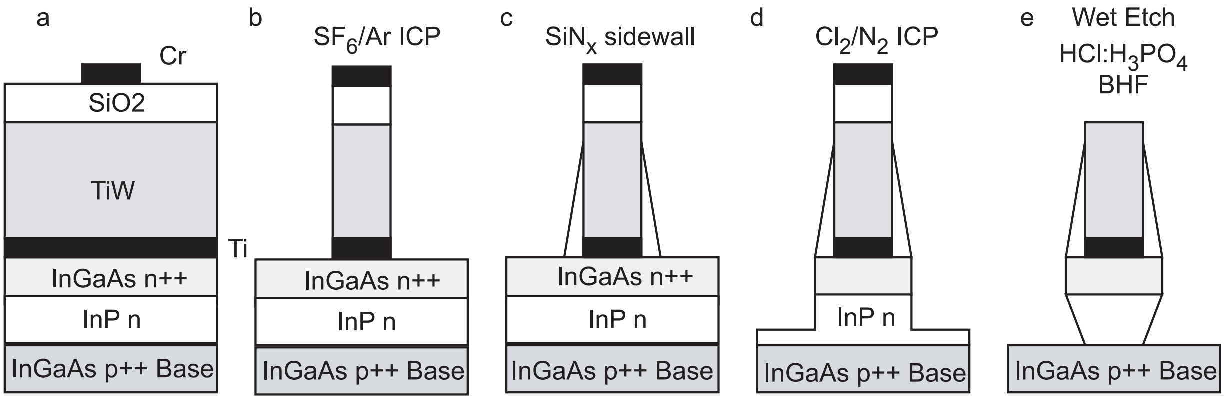

Figure 1. Emitter formation process: a) Blanket sputter Ti/TiW, blanket deposition of SiO_2 by PECVD, and a Cr mask is defined. b) SiO_2 and TiW etch. c) SiN_x sidewall formed. d) InGaAs and partial InP emitter etch. e) Chemical wet-etches completes the emitter mesa formation and removes SiO_2 cap.

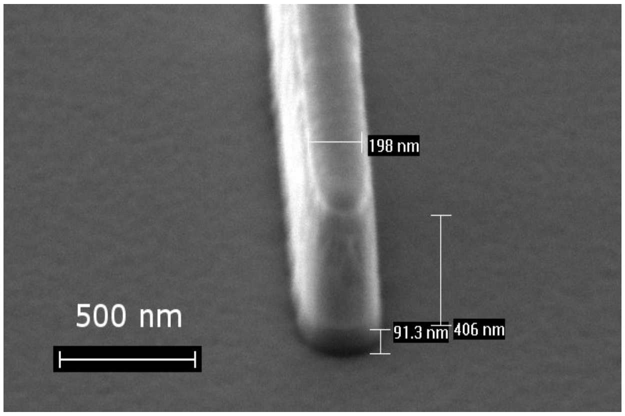

Figure 2. SEM at 60° angle of TiW emitter before InP wet etch

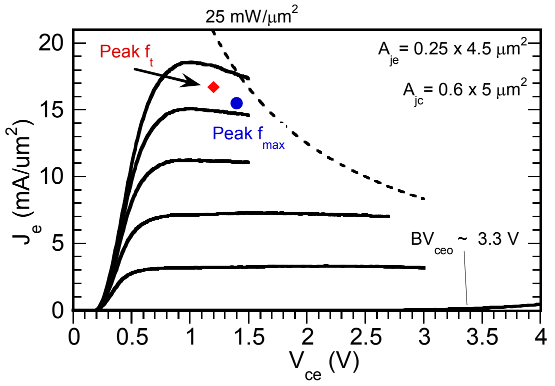

Figure 3. Common-emitter I-V characteristics

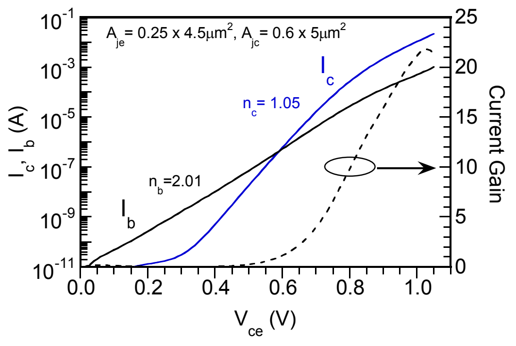

Figure 4. Gummel characteristics

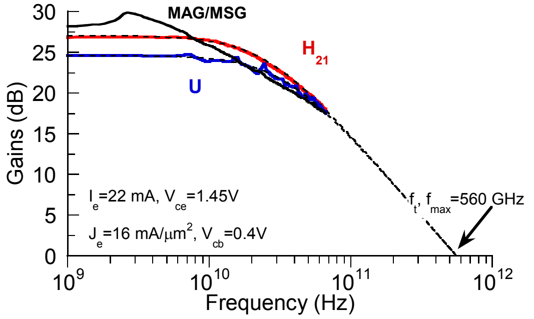

Figure 5. RF gains and single pole fits for fitting of f_t and f_{max}.

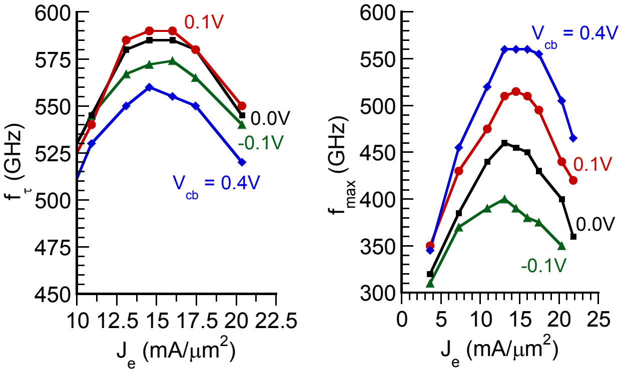

Figure 6. f_t and f_{max} versus J_e and V_{cb}

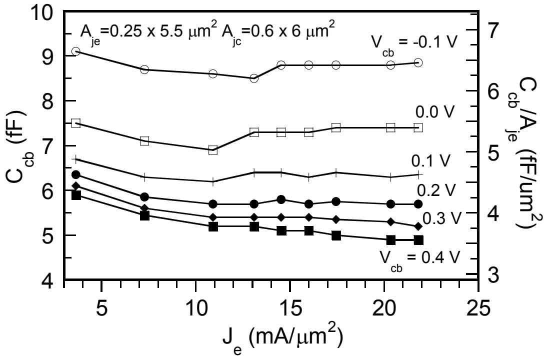

Figure 7. Ccb variation with bias / current density