THz Bipolar Transistor Circuits: Technical Feasibility, Technology Development, Integrated Circuit Results

Mark Rodwell, E. Lobisser, M. Wistey, V. Jain, A. Baraskar, E. Lind, J. Koo
University of California, Santa Barbara

Z. Griffith, J. Hacker, M. Urteaga, D. Mensa, Richard Pierson, B. Brar
Teledyne Scientific

***Abstract*—We examine the feasibility of developing bipolar transistors with current-gain and power-gain cutoff frequencies of 1-3 THz. High bandwidths are obtained by scaling; the critical limits to such scaling are the requirements that the current density increase in proportion to the square of bandwidth and that the metal-semiconductor contact resistivities vary as the inverse square of device bandwidth. Transistors with 755 GHz f_{max} and 324 GHz amplifiers have been demonstrated. Contacts with resistivity sufficient for the 64 nm scaling geneation (1 THz f_τ, 2 THz f_{max}) have been developed.**

We here examine the high-frequency performance limits of InP-based bipolar transistors, and their potential for operation at low THz frequencies [1].

In most semiconductor devices, signal currents are generated by modulating electron flow though depletion regions. The resulting displacement currents are coupled to the external circuit via Ohmic contacts to doped semiconductor layers. Electron device bandwidths are thus determined by depletion layer transit times and capacitances, and by bulk and contact resistivities; currents are limited by bulk, contact, and equivalent-space-charge resistances and by device heating. Device bandwidths are increased by reducing junction dimensions (lithographic scaling), reducing layer thicknesses (epitaxial scaling) and by reducing Ohmic contact resistivities and thermal resistivities.Consideration of these *classic* effects remains the central imperative in the development of any proposed THz semiconductor electron device.

First consider scaling of a PIN photodiode. To double bandwidth, we must reduce all capacitances and transit times 2:1 while maintaining constant the diode resistance, operating current, and voltage. To reduce carrier transit time 2:1, we reduce the depletion layer thickness 2:1. We have doubled the capacitance per unit area, hence to reduce the capacitance 2:1, we must now reduce the junction area 4:1. We seek to maintain constant contact resistance in the presence of 4:1 reduced junction area, and consequently must reduce the contact resistivity 4:1. The same current must be carried through a junction of 4:1 smaller area; thermal resistance per unit junction area must be reduced 4:1.

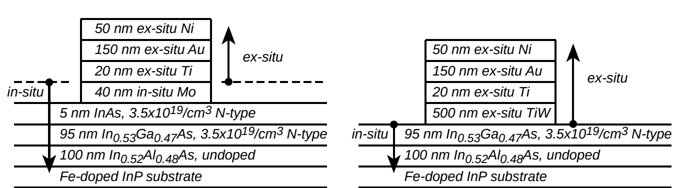
The design and scaling laws for bipolar transistors differs only trivially from the above. Each doubling in device bandwidth demands a 2:1 thinning of epitaxial layers, a 4:1 reduction in junction widths, a 4:1 increase in current densities, and a 4:1 reduction in contact resistivities. In highly scaled devices, contact resistivities ***dominate*** over bulk resistivities.

Given these scaling principles, electrical contact resistances and device and IC thermal resistances are the critical limits to further improvements in the bandwidth of bipolar transistors and the integrated circuits which employ them. Table 1 shows a proposed technology scaling roadmap extending through the 32 nm (~1.4 THz f_τ and ~ 2.8 THz $f_{\max}$) generation. Such a technology would permit construction of ~1.4 THz tuned amplifiers and of small-scale digital circuits operating at 600 GHz digital clock frequency. It is no surprise that to construct such a transistor presents formidable challenges. In particular, resistivities of the emitter and base contacts must be below 1 $\Omega-\mu\text{m}^2$, and both the contacts and the semiconductor junctions must be stable at current densities of almost 100 mA/μm^2. Development of thermodynamically stable and low resistance Ohmic contacts is clearly central to the development of THz transistors.

Given demonstrated values of contact resistivity to n-InGaAs and p-InGaAs, devices extending through the 64 nm scaling generation are feasible. Our present efforts in developing THz InP bipolar transistors include not only development of process flows for fabricating devices with 128 nm (and subsequently 64 nm) emitter and base contact widths but also in the development of stable and low-resistance Ohmic contacts. While contact resistivities of order 10 $\Omega-\mu\text{m}^2$ are routinely obtained with simple nonalloyed contacts to e.g. InAs, obtaining resistivities of c.a. 1 $\Omega-\mu\text{m}^2$ requires particular attention to the removal of semiconductor oxides of other contaminants at the interface. To date, we have attained <1 $\Omega-\mu m^2$ resistivity in contacts to N-InGaAs through either *in-situ* deposition of Mo contact metal during semiconductor MBE growth [2] or through *ex-situ* deposition of refractory TiW contacts after surface cleaning and passivation by soaking in concentrated ammonia [3]. We are now exploring similar processes for contacts to P-type materials.

Table 1: Bipolar transistor scaling laws and InP HBT scaling roadmap. Junction temperature rise is of an isolated HBT, and is computed for 2 µm L_e and V_{ce}=1.5 V. Noise figure assumes β=40.

Parameter	scaling law	Gen. 3 (256 nm)	Gen. 4 (128 nm)	Gen 5 (64 nm)	Gen 5 (32 nm)
MS-DFF speed	γ^1	240 GHz	330 GHz	480 GHz	660 GHz
Amplifier center frequency	γ^1	430 GHz	660 GHz	1.0 THz	1.4 THz
Emitter Width	$1/\gamma^2$	256 nm	128 nm	64 nm	32 nm
Resistivity	$1/\gamma^2$	8 Ω-µm²	4 Ω-µm²	2 Ω-µm²	1 Ω-µm²
Base Thickness	$1/\gamma^{1/2}$	250 Å	212 Å	180 Å	180 Å
Contact width	$1/\gamma^2$	175 nm	120 nm	60 nm	30 nm
Doping	γ^0	7 10¹⁹ /cm²	7 10¹⁹ /cm²	7 10¹⁹ /cm²	7 10¹⁹ /cm²
Sheet resistance	$\gamma^{1/2}$	600 Ω	708 Ω	830 Ω	990 Ω
Contact ρ	$1/\gamma^2$	10 Ω-µm²	5 Ω-µm²	2.5 Ω-µm²	1.25 Ω-µm²
Collector Width	$1/\gamma^2$	600 nm	360 nm	180 nm	90 nm
Thickness	$1/\gamma$	106 nm	75 nm	53 nm	37.5 nm
Current Density	γ^2	9 mA/µm²	18 mA/µm²	36 mA/µm²	72 mA/µm²
$A_{collector}/A_{emitter}$	γ^0	2.4	2.9	2.8	2.8
f_τ	γ^1	520 GHz	730 GHz	1.0 THz	1.4 THz
f_{max}	γ^1	850 GHz	1.30 THz	2.0 THz	2.8 THz
$V_{BR,CEO}$		4.0 V	3.3 V	2.75 V	?
ΔT		50 K	61 K	72K	83 K
I_E / L_E	γ^0	2.3 mA/µm	2.3 mA/µm	2.3 mA/µm	2.3 mA/µm
τ_f	$1/\gamma$	240 fs	180 fs	130 fs	95 fs
C_{cb}/I_c	$1/\gamma$	280 fs/V	240 fs/V	170 fs/V	120 fs/V
$C_{cb}\Delta V_{logic}/I_c$	$1/\gamma$	85 fs	74 fs	52 fs	36 fs
$R_{bb}/(\Delta V_{logic}/I_c)$	γ^0	0.47	0.34	0.26	0.23
$C_{je}(\Delta V_{logic}/I_C)$	$1/\gamma^{3/2}$	180 fs	94 fs	50 fs	33 fs
$R_{ex}/(\Delta V_{logic}/I_c)$	γ^0	0.24	0.24	0.24	0.24
670 GHz gain	--	--	4.3 dB	8.7 dB	12.8 dB
670 GHz Fmin	--	--	7.4 dB	5 dB	3.8 dB
1030 GHz gain	--	--	--	4.9 dB	7.9 dB
1030 GHz Fmin	--	--	--	7.3 dB	5.0 dB



(a) (b)

Figure 1: Layer structures for < 10^{-8} Ω-cm² resistivity emitter contacts. (a) *in-situ* Molybdenum contacts and (b) TiW contact deposited *ex-situ* after UV-ozone and NH_3OH surface treatment.

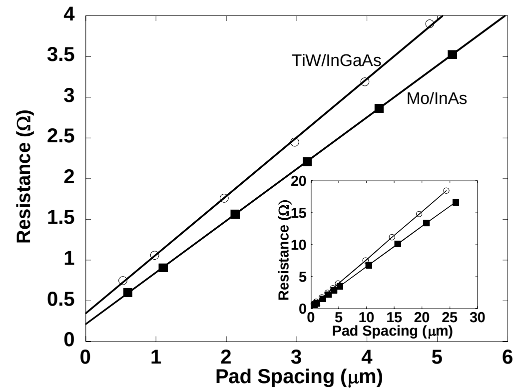
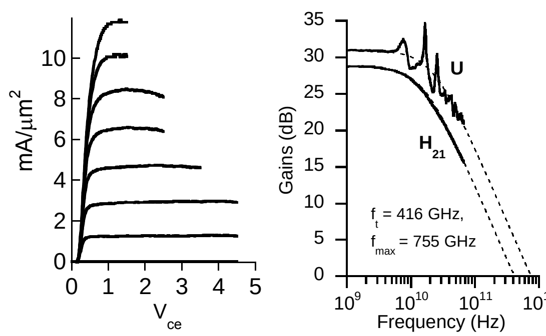
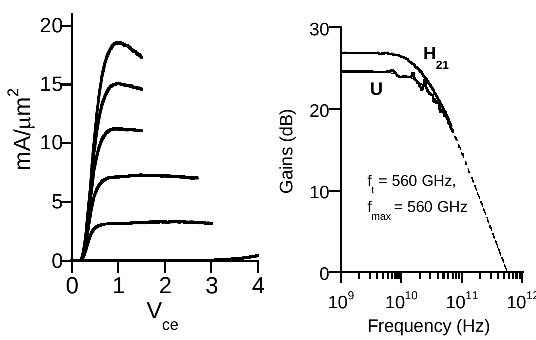


Figure 2: Resistance measurement, by the TLM method with test structures of 26.6 µm width, for TiW/InGaAs ex-situ and Mo/InAs in-situ emitter Ohmic contacts. The extracted contact resistivities are 0.7 and 0.5 Ω-µm² respectively.



(a) (b)

Figure 3: Measured common-emitter characteristics (a) and RF gains (b) of a DHBT having T_c=150 nm, T_b=30 nm, and W_e=250 nm, biased at J_e=12 mA/µm². The DHBT exhibits $V_{br,ceo}$ =5.6V at I_c/A_e=10 kA/cm².



(a) (b)

Figure 4: Measured common-emitter characteristics (a) and RF gains (b) of a DHBT having T_c=70 nm, T_b=22 nm, and W_e=250 nm biased at J_e=13 mA/µm². The DHBT exhibits $V_{br,ceo}$ =3.3V at I_c/A_e=15 kA/cm² [4].

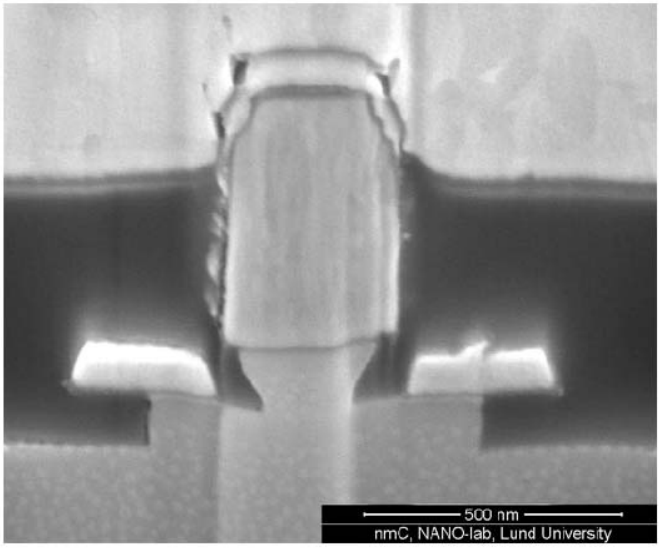


Figure 5: Focused-ion-beam cross section of a DHBT with a 180 nm emitter-base junction width. This HBT was fabricated using ICP reactive-ion (dry) etches to define both the emitter metal contact and the emitter-base junction

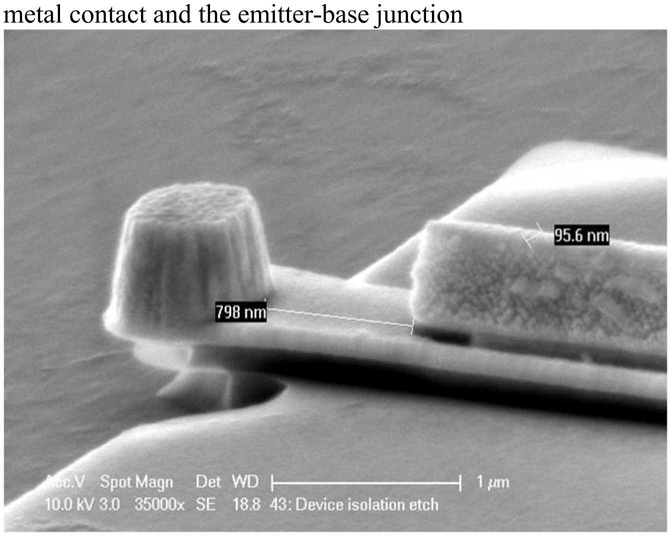


Figure 6: Electron Micrograph of 128 HBT in fabrication, immediately before deposition of the collector contact. The emitter and base contacts are both 100-120 nm wide.

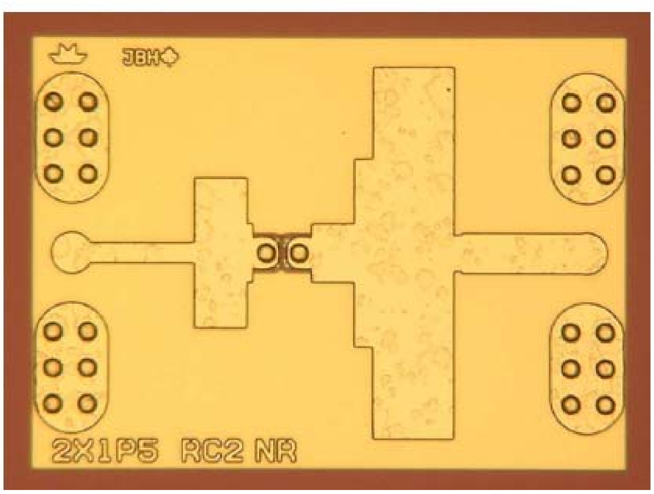


Figure 7: Single-stage InP DHBT common base 324 GHz power amplifier with microstrip lines on thick 10µm BCB. The IC was fabricated in Teledyne's 256 nm InP DHBT technology The amplifier produces 4.8 dB gain at 324 GHz.

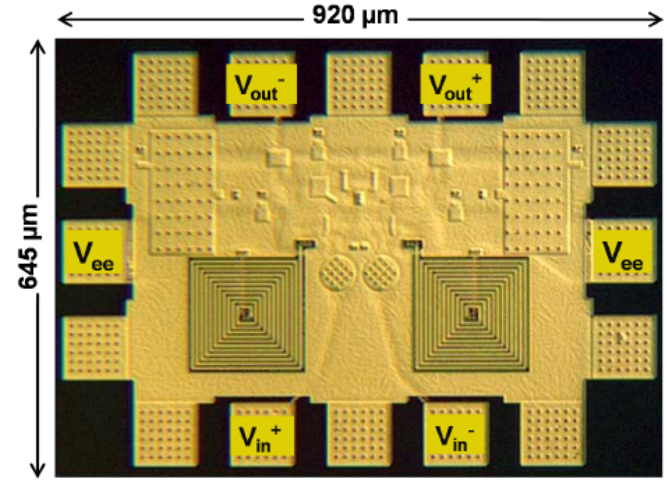


Figure 8: Single-loop current-mode microwave feedback amplifier The amplifier dissipates 1.0 W, and exhibits a 53 dBm output-referred 3rd-order intercept at 2 GHz.

REFERENCES

[1] Mark Rodwell, Minh Le Member, Berinder Brar, "InP Bipolar ICs: Scaling Roadmaps, Frequency Limits, Manufacturable Technologies" IEEE Proceedings, Volume 96, Issue 2, Feb. 2008 Page(s):271 - 286 and addendum, IEEE Proceedings Volume 96, Issue 4, April 2008 Page(s):748 - 748

[2] U. Singisetti, A. M. Crook, E. Lind, J. D. Zimmerman, M. A. Wistey, A. C. Gossard, and M. J. W. Rodwell: "Ultra-Low Resistance Ohmic Contacts to InGaAs/InP", 2007 IEEE Device Research Conference, June 18-20, Univ. of Notre Dame, South Bend, Illinois

[3] Adam M. Crook, Erik Lind, Zach Griffith, Mark J. W. Rodwell, Jeremy D. Zimmerman, Arthur C. Gossard, Seth R. Bank, "Low resistance, nonalloyed Ohmic contacts to InGaAs", Applied Physics Letters, Vol. 91, 192114, 2007

[4] Erik Lind, Adam M. Crook, Zach Griffith, Mark J.W. Rodwell, Xiao-Ming Fang, Dmitri Loubychev, Ying Wu, Joel M. Fastenau, and Amy W.K. Liu: "560 GHz ft, fmax InGaAs/InP DHBT in a novel dry-etched emitter process", 2007 IEEE Device Research Conference, June 18-20, Univ. of Notre Dame, South Bend, Illinois