Ultralow resistance *in situ* Ohmic contacts to InGaAs/InP

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We report a sharp reduction in the resistivity of Ohmic contacts using *in situ* deposition of molybdenum (Mo) contacts onto *n*-type $In_{0.53}Ga_{0.47}As$ grown on InP. The contacts were formed by evaporating Mo onto the wafer using an electron beam evaporator connected to a molecular beam epitaxy chamber under ultrahigh vacuum. Transmission line measurements showed specific contact resistivities of $0.5\pm0.3\ \Omega\ \mu m^2$ ($2.90\ \Omega\ \mu m$), $0.9\pm0.4\ \Omega\ \mu m^2$ ($4.3\ \Omega\ \mu m$), and $1.3\pm0.4\ \Omega\ \mu m^2$ ($4.7\ \Omega\ \mu m$) for Mo on abrupt InAs/InGaAs heterojunctions, graded InAs/InGaAs, and InGaAs films, respectively. These low resistances meet the requirements for terahertz transistors. © *2008 American Institute of Physics*. [DOI: 10.1063/1.3013572]

Resistance at metal-semiconductor contacts is one of the major obstacles to increasing speeds in analog and digital transistors, along with lateral scaling to sub-50 nm dimensions and vertical scaling of intrinsic electron transport layers.[1] For example, a contact resistivity of $\sim 2\times10^{-8}\ \Omega\ cm^2$ ($2\ \Omega\ \mu m^2$) is required for realizing heterojunction bipolar transistors (HBTs) with simultaneous 1 THz f_t and f_{max}.[1] Furthermore, if transistors are scaled assuming constant supply voltages, a twofold increase in transistor bandwidth demands a fourfold decrease in contact resistivity. Similarly, in potentially high drive current InGaAs field effect transistors (FETs), a source contact resistivity of just $1\ \Omega\ \mu m^2$ degrades drive current by 10%.[2] $In_{1-x}Ga_xAs$ based channel FETs have higher electron velocity than Si and may serve as the channel at sub-22-nm gate node,[2] so there exists strong motivation to develop reliable, low-resistance Ohmic contacts to InGaAs.

Low resistance contacts to III–V semiconductors have traditionally been obtained by alloying AuGe eutectic and semiconductor and also by increasing the doping levels in the semiconductor, but surface oxides and defects must also be removed before depositing contact metals. Previously, *n*-type contact resistivity of $2.7\ \Omega\ \mu m^2$ was reported by using an Ar^+ sputter clean of the surface.[3] Contact resistivity of $<1\ \Omega\ \mu m^2$ has been achieved by strong NH_4OH treatment of the surface[4] and also with the use of an InAs cap layer.[5] But *ex situ* contacts are very sensitive to the exact details of surface preparation. Unlike H passivation of Si by HF treatment, III–V semiconductors do not have a good surface passivation technique. Hence the time between surface cleaning step and metal deposition is very important. The semiconductor surface invariably gets oxidized and contaminated with cleanroom atmospheric elements in the time between surface cleaning and metal deposition. Because of this sensitivity to surface history, it is difficult to obtain reproducibly contact resistivity of $<1\ \Omega\ \mu m^2$ using *ex situ* contacts. We have observed an order of magnitude variation in *ex situ* contact resistivity over the course of more than ten runs. Most *ex situ* contacts use a titanium (Ti) interface layer for both adhesion and oxygen gettering, but Ti diffuses into the semiconductor during high temperature processing of devices, degrading the contact resistance.[5]

To study whether an oxygen-free environment would improve contact reproducibility, we studied *in situ* formed contacts where the contact metal is deposited immediately after semiconductor growth without breaking the vacuum. Even trace oxidation adds surface states, depleting electrons and increasing both the Schottky barrier width and height, thus increasing contact resistance.[6] Highly degenerate doping of the semiconductor is required to promote low-resistance tunneling through the potential barrier at the interface. Refractory metal contacts are preferred because of their stability under high temperature and high current density. *In situ* aluminum (Al) contacts were previously studied because of the ready availability of Al sources in molecular beam epitaxy (MBE), but epitaxial Al on III–V semiconductor has a very rough surface, making Al unusable in scaled devices.[7] Also, Al rapidly forms an insulating oxide when exposed to air,

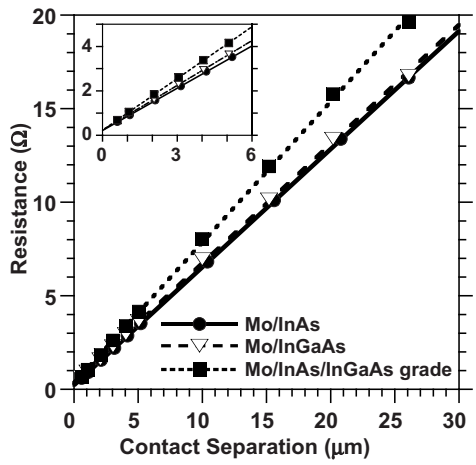

FIG. 1. Measured resistance vs contact separation for the contacts. Contact width is 25 μm. The inset magnifies the range from 0.6 to 5 μm. The sheet resistance and contact resistance are calculated from the slope and *y*-intercept of the line fit.

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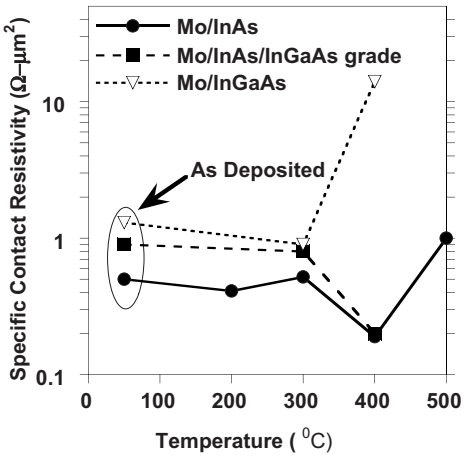

FIG. 2. Specific contact resistivity as a function of annealing temperature.

which complicates device fabrication. Also, Al, like Ti, will intermix with semiconductors, leading to unreliable contacts, particularly at high currents or after high temperature processing.

Here we report *in situ*, refractory molybdenum (Mo) contacts to $In_{0.53}Ga_{0.47}As$. The contact metal was deposited in an electron beam evaporator attached to a MBE chamber by ultrahigh vacuum (UHV). Three types of *in situ* contacts were studied. First, *in situ* Mo contacts to relaxed InAs on $In_{0.53}Ga_{0.47}As$ were studied since the Fermi level pins above the conduction band of InAs.[8] Second, the InAs-InGaAs junction was graded to remove the abrupt heterojunction barrier due to the conduction band offset. Finally, Mo deposited directly on $In_{0.53}Ga_{0.47}As$ was studied.

All the samples were grown by solid-source MBE. First, an unintentionally doped 1000 Å of InAlAs buffer was grown on (100) semi-insulating InP. For the step and graded junctions, 950 Å of highly doped InGaAs (Si=8.0 $\times 10^{19}$ cm^{-3}) was grown. For the InAs/InGaAs step junction contacts, an additional 50 Å of Si doped InAs was grown; for the graded contact, additional InGaAs was digitally graded to InAs over 200 Å, followed by 100 Å of InAs. Both the graded layer and the top InAs were doped with Si. For the InGaAs contact, 1000 Å of Si doped InGaAs was grown. Hall measurement on the *n*-InGaAs layer gave 3.6 $\times 10^{19}$ cm^{-3} active carrier concentration and a mobility of 1266 $cm^2\ V^{-1}\ s^{-1}$. The wafers were then transferred under UHV to an electron beam evaporator with a base pressure of 10^{-9} Torr. 100 Å of Mo was deposited on the Mo/InGaAs sample, and 200 Å on the others. The samples were then processed into transmission line method (TLM) structures for contact resistance measurement. Ti(200 Å)/Au(1500 Å)/Ni(500 Å) contact pads were patterned using *i*-line optical lithography and lift-off. Mo was then dry etched in a SF_6/Ar plasma using Ni as an etch mask. The TLM structures were then isolated using a second round of photolithography and wet etched to define mesas.

A four-point probe technique was used to measure resistances using an Agilent 4155C semiconductor parameter analyzer. The TLM method was used to measure contact resistance because of the high accuracy of the technique.[9] The TLM contact geometry was designed to accurately measure contact resistivities on the order of 1 $\Omega\ \mu m^2$.[4] Contact separations varied from 500 nm to 25 μm, and contact widths were 25 μm. Contact resistance dominates the total resistance at small contact separations, and sheet resistance dominates at larger separations.

Figure 1 plots the measured resistance versus the contact separation in the TLM structures. Specific contact resistivity and InGaAs sheet resistance were calculated respectively from the *y*-intercept and slope of the linear fit to the measured data. The transfer length of the contacts was calculated from the *x*-intercept of the line fit. The specific contact resistivity (ρ_c) for the InAs/InGaAs step junction contact, the InAs/InGaAs graded contact, and the InGaAs contact are $0.5 \pm 0.3\ \Omega\ \mu m^2$, $1 \pm 0.5\ \Omega\ \mu m^2$, and $1.3 \pm 0.5\ \Omega\ \mu m^2$, respectively, with error analysis according to Ref. 10. The InAs/InGaAs step junction contact and the InGaAs contact showed a sheet resistance of 16.5 $\Omega/\square$. The InAs/InGaAs graded junction contact has a sheet resistance of 19.5 $\Omega/\square$. The transfer lengths of the InAs/InGaAs step junction contact, the InAs/InGaAs graded junction contact, and the InGaAs contacts are 175, 225, and 280 nm respectively, an order of magnitude smaller than the contact length. We conclude that the one-dimensional current flow assumption slightly overestimates the extracted contact resistivity.[4] The variation in contact resistivity of these *in situ* contacts was less than 30% in ten different process runs. This variation was within the calculated error margin of the TLM measurement.

The InAs/InGaAs step junction contact gave the lowest contact resistance, which we attribute to pinning of the Fermi level inside the InAs conduction band.[8] The InAs/InGaAs graded junction contact was intended to evaluate the contri-

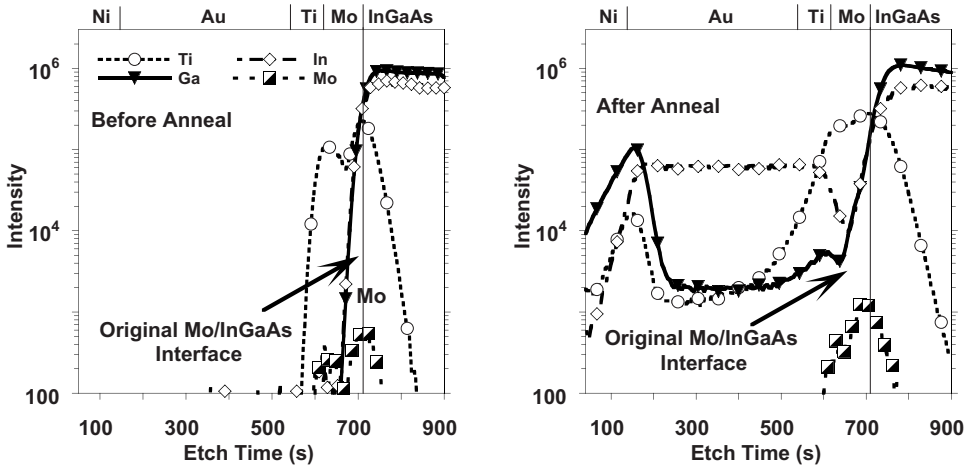

FIG. 3. SIMS analysis of Mo/InGaAs contact as deposited and after 400 °C, 1 min anneal. Au, Ni, and As profiles have been omitted for clarity. Top of the plot delineates approximate boundary of the layers.

bution of the InAs/InGaAs conduction band offset to contact resistance. The measured contact resistance and sheet resistance are slightly higher than the step junction contact. This could be ascribed to an unintentional higher doping in InAs for the step junction contact since the Si dopant cell may not have had time to cool to its temperature for the lower growth rate of InAs. This may have effectively doped the top InAs in the step junction higher than the graded junction contact. Nevertheless, we show an upper bound of 0.5 $\Omega\ \mu m^2$ for the resistance associated with the InAs/InGaAs conduction band offset. The contact resistance of the Mo/InGaAs contact was higher than in either of the InAs-capped contacts, which we attribute to Fermi level pinning within the InGaAs band gap.

Thermal stability studies on the contacts were carried out by annealing the contacts under N_2 flow for 1 min at various temperatures. All the contacts exhibited linear *I-V* behavior before and after annealing. Figure 2 plots the specific contact resistivity as a function of temperature. For all contacts the specific contact resistivity degradation is $<10\%$ even after annealing at 300 °C. The specific contact resistivity of the Mo/InGaAs contact increased to 14 $\Omega\ \mu m^2$ after 400 °C, 1 min anneal, while no degradation was observed for the other two contacts. Secondary ion mass spectroscopy (SIMS, not shown) on the InAs/InGaAs step junction and graded junction contacts showed negligible interdiffusion of In, Ga, and Ti. SIMS of the annealed Mo/InGaAs contact (Fig. 3) showed diffusion of In and Ga into Au and diffusion of Ti into the semiconductor. We attribute this difference to the thinner Mo on this sample (100 Å versus 200 Å); it appears that 100 Å of Mo was ineffective as a diffusion barrier at 400 °C, perhaps due to porous gaps between grains for the thinner Mo film. But a 200 Å layer of Mo was an effective diffusion barrier to Au and Ti at these temperatures.

In conclusion, we show that low resistance *in situ* metal contacts with specific contact resistivity of 0.5 $\Omega\ \mu m^2$ (2.9 $\Omega\ \mu m$) can be formed to InAs/InGaAs layers. These low-resistance, thermally robust, metal-semiconductor contacts remove one of the major obstacles to terahertz bandwidth InGaAs/InP HBTs, millimeter-wave InGaAs high electron mobility transistor technologies, and potentially high drive current III–V metal-oxide-semiconductor field-effect transistor technologies.

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