Performance Comparison of Scaled III-V and Si Nanowire MOSFET

Lingquan Wang*, Bo Yu*, Peter Asbeck*, Yuan Taur*, Mark Rodwell[+]
*University of California, San Diego; [+]University of California, Santa Barbara

Recently, scaled MOSFET structures based on nanowires have received intensive research interest since they can provide superior control over short channel effects (SCE) as compared to conventional bulk structures [1]. For devices with ultra-short gate lengths (comparable to the mean free path of carriers) where these structures are likely to be employed, transport within the devices is expected to be ballistic or quasi-ballistic. In this paper, we compare the ballistic limit performance for III-V and Si nanowire MOSFETs (NWMOSFET). The simulation reveals interesting tradeoffs between the two types of materials. High mass and multi-valley degeneracy may have a positive or negative influence on the saturation current, depending on the effective oxide thickness (EOT) of the device. On the other hand, high mass and multi-valley degeneracy result in much smaller turn on resistance at low drain bias in the ballistic limit.

The structure simulated is a gate-all-around (GAA) MOSFET, as shown schematically in Fig.1. The two types of MOSFETs under study only differ in the core (channel) material. For the III-V case, $In_{0.53}Ga_{0.47}As$ with effective mass of $0.041m_0$ was used. The simulation employs a self-consistent Schrödinger Poisson solver for cylindrical coordinates [2] to account for the quantum effects. Ballistic current computation is based on an extension of Natori's model, as reported in [1, 3]. In our simulation, Si was approximated as an isotropic material with effective mass of 0.258 ($3*m_t*m_l/(2m_t+m_l)$) and degeneracy factor of 6. Fig. 2 shows representative output characteristics for two types of MOSFETs, where current is normalized to the nanowire circumference. EOT's for both cases equal to 0.55nm. Two features are observed here: InGaAs MOSFET delivers higher saturation current, whereas Si MOSFETs exhibits much smaller turn-on resistance at low V_{DS}. To understand the higher current in III-V NWMOSFETs, the total charge density and average carrier velocity are shown in Fig. 3 and 4, respectively. It is intuitive that with low density of state (low mass and degeneracy), less charge exists in III-V NWMOSFET. However, for the same reason, the Fermi level within the nanowire follows closely the gate voltage, driving the core into heavy degeneracy, which further induces a sharp increase on average carrier velocity. In this representative example, the increment in carrier velocity outweighs the disadvantage of less charge, thus yielding a higher saturation current for III-V NWMOSFET.

To further understand the tradeoffs associated with effective mass and valley degeneracy, we analyze the structure at T=0K, to avoid involved mathematics. The capacitance network along the radial direction is schematically shown in Fig. 5. The density of states factors in as an energy dependent capacitance: $C_{DOS} = (q^2 g/\pi\hbar)\sqrt{m^*/2(E_f - E_1)}$, where E_f and E_1 are Fermi level and energy of the first eigen-state, respectively. Assume that C_{qw} is slow varying as a function of gate bias, at T=0K, the ballistic current can be written as $I = gq(E_f - E_1)/\pi\hbar$. ($E_f$-$E_1$) can be solved via the capacitance network through the relation $d(E_f - E_1) = qd(V_G - V_{th}) \cdot C_{ox}'/(C_{ox}' + C_{DOS})$. The ballistic current can thus be expressed as:

$$I = \frac{q^2 g}{\pi\hbar}[(V_G - V_{th}) - \frac{m^* q^3 g^2}{\pi^2\hbar^2 C_{ox}'^2}(\sqrt{1 + \frac{2\hbar^2\pi^2 C_{ox}'^2 (V_G - V_{th})}{q^3 g^2 m^*}} - 1)].$$

Under the condition when $C_{ox}' >> C_{DOS}$, the current approaches a constant value $(gq^2/\pi\hbar)(V_G - V_{th})$, which is proportional to degeneracy factor; whereas in case of $C_{ox}' << C_{DOS}$, expanding the square root term to the second order yields the following: $I = \pi\hbar C_{ox}'^2 (V_G - V_{th})^2/(2m^* gq)$, indicating that the current decreases with increased effective mass and valley degeneracy. This tendency is shown in Fig. 6, associated numerical computation is shown in Fig. 7, showing the same trend.

In conclusion, III-V NWMOSFETs may outperform Si NWMOSFETs in terms of saturation current depending on the available equivalent insulator thickness. Large mass and valley degeneracy always provide a smaller turn on resistance at low drain bias in the ballistic limit (although mobility differences between materials will further affect the comparison). Valley degeneracy may have positive or negative influence on saturation current depending on EOT.

[1] B. Yu, L. Wang, Y, Yuan, Y, Taur, P. Asbeck, "Scaling of nanowire transistors", submitted to Trans. of Elec. Dev.
[2] L. Wang, D. Wang, P. Asbeck, "A numerical Schrödinger-Poisson solver for radially symmetric nanowire core-shell structures", Solid State Electronics, vol. 50, pp 1732-1739
[3] K. Natori, "Ballistic metal-oxide-semiconductor field effect transistor", J. Appl. Phys. vol. 76, pp. 4879-4890

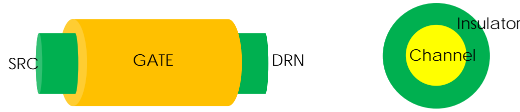

Figure 1 Schematic drawing of nanowire transistor.

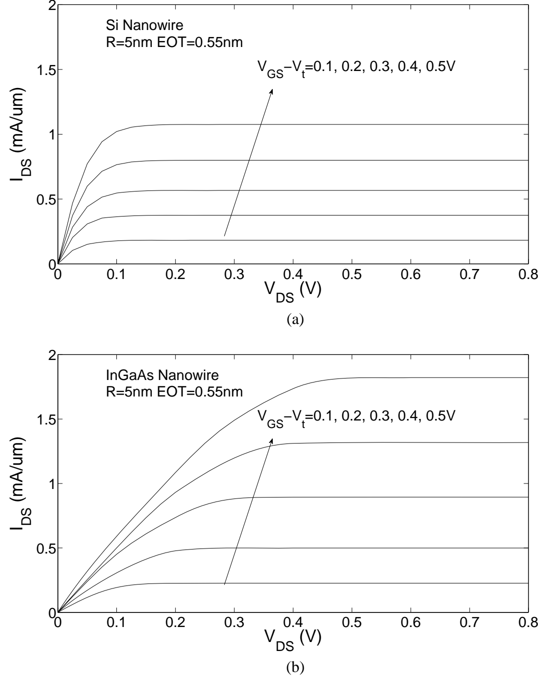

Figure 2 Computed ballistic output characteristic as function of drain bias for (a) Si nanowire and (b) InGaAs nanowire. Current is normalized to the nanowire circumference.

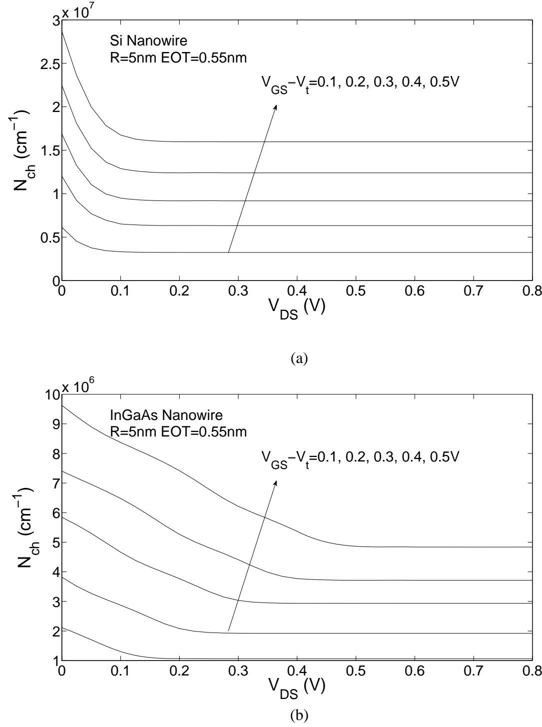

Figure 3 Computed line charge density under ballistic condition as function of drain bias for (a) Si nanowire and (b) InGaAs nanowire.

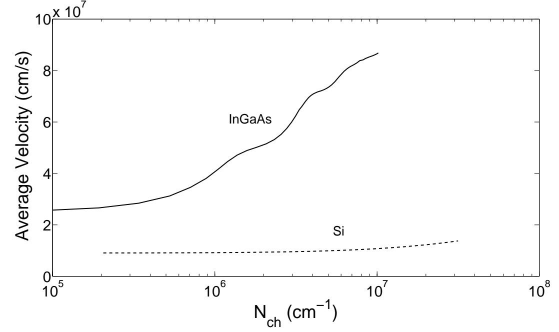

Figure 4 Average injection velocity of Si and InGaAs at the virtual source. Parabolic band model has been used.

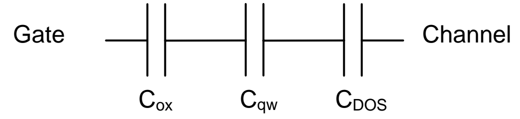

Figure 5 Schematic capacitance network. Here:

$C_{qw} = \frac{\partial Q_s}{\partial (E_1 - E_c)/q}$ where E_1 and E_c are the first eigenstate energy and conduction band edge at the interface, respectively.

$C_{DOS} = \frac{\partial Q_s}{\partial (E_f - E_1)/q}$ where E_f is the Fermi level.

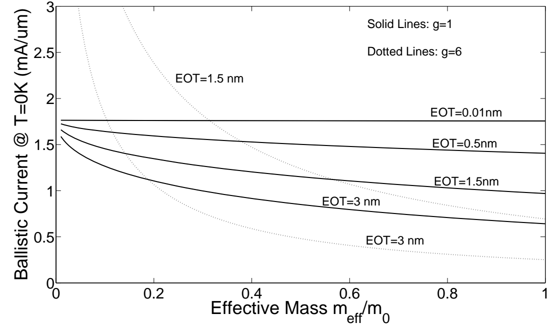

Figure 6 Computed ballistic saturation current at T=0K with one subband only, with gate overdrive as 0.5V. The EOT considered here includes both oxide thickness and finite wave function depth. Solid curves are for single valley situation, dotted curves are for valley degeneracy as 6. Radius of nanowire is 5nm; current is normalized to the nanowire circumference.

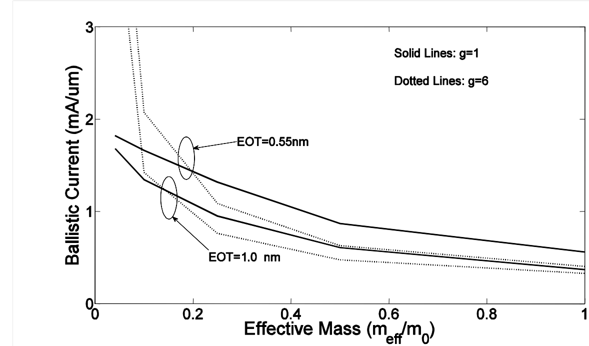

Figure 7 Coupled Schrödinger Poisson simulation on ballistic saturation current at room temperature with gate overdrive as 0.5V. The EOT considered here includes ONLY the oxide thickness. Solid curves are for single valley situation, dotted curves are for valley degeneracy of 6. Radius of nanowire is 5nm; current is normalized to the nanowire circumference.