DEVELOPMENT OF THZ TRANSISTORS AND (300-3000 GHZ) SUB-MM-WAVE INTEGRATED CIRCUITS

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ABSTRACT

We examine the feasibility of developing bipolar transistors with power-gain cutoff frequencies of 1-3 THz. High bandwidths are obtained by scaling; the critical limits to such scaling are the requirements that the current density increase in proportion to the square of bandwidth and that the metal-semiconductor contact resistivities vary as the inverse square of device bandwidth. Transistors with 755 GHz $f_{\max}$ and 324 GHz amplifiers have been demonstrated. Transistors with target $f_{\max}$ over 1 THz are in development.

I. INTRODUCTION

Continued scaling of CMOS processes, driven the desire to increase digital integrated circuit complexity and clock frequency, has rapidly increased the transistor small-signal cutoff frequencies. MOSFETs with 45 nm gate lengths have shown 450 GHz power-gain cutoff frequencies [1] ($f_{\max}$) and devices with 29 nm gate length (65 nm lithographic half-pitch) [2] have shown 360 GHz current-gain cutoff frequency (f_τ) and 420 GHz $f_{\max}$. These technologies will enable a new generation of inexpensive yet high-frequency communications ICs, including CMOS optical fiber transceiver chip-sets at 40 Gb/s and above [3] and mm-wave radio links at 60 GHz [4] and above 100 GHz [5]. Further scaling will bring further increases in device and circuit bandwidths, but it is not yet clear whether scaling can continue much beyond the 22 nm (half-pitch) generation [6].

Despite the rapid progress with Si CMOS, InP-based heterojunction bipolar transistors (HBTs) [7] and high-electron-mobility field effect transistors (HEMTs) [8,9] continue to show superior device bandwidth. At a given process minimum feature size, both InP-based HBTs and HEMTs attain a higher bandwidth than is obtained in CMOS. Compared to CMOS, much higher breakdown voltage is obtained for InP DHBTs of comparable bandwidths. Detailed HBT scaling analysis [7], to be summarized below, strongly suggests that HBTs of at least 1 THz f_τ , 2 THz $f_{\max}$, ~7 dB noise figure at 1 THz, and ~2.5 V breakdown are feasible. While to date there have been published no scaling analyses of similar detail for InGaAs/InP HEMTs, a first-order hand analysis suggests that ~1.5 THz f_τ and $f_{\max}$ should be attainable under the limiting assumptions of ballistic transport [10], 22 nm gate length [11] (about the minimum feasible given limits to both quantum well thickness and to device aspect ratio), extremely low source access resistance, and a high-*K* gate insulator.

These scaling analyses, together with recent III-V device and at 300-340 GHz [7, 8, 9, 12] strongly suggest the feasibility of sub-mm-wave integrated circuits operating in the 300-1000 GHz frequency range. Potential applications include sub-mm-wave spectroscopy [13] and sub-mm-wave radar [14] for imaging and for vehicle collision avoidance.

Because transistors are general-purpose electronic control elements, a sub-mm-wave IC serving such an application could perform all necessary high-frequency signal-processing operations, including LO generation by frequency synthesis, modulation, frequency conversion between RF and baseband, RF and IF filtering, transmitter power amplification, and receiver low-noise amplification. THz transistors will thus enable compact and functionally complex sub-mm-wave systems.

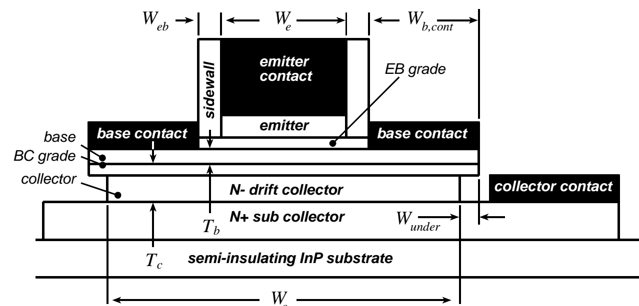

Figure 1: HBT cross-section and critical dimensions. The emitter stripe extends a distance L_e perpendicular to the figure. W_e is the emitter junction width, W_{eb} the base-emitter sidewall spacer thickness, $W_{b,cont}$ the width of the base Ohmic contact, and W_{under} the undercut of the collector junction under the base contacts. The base thickness is T_{cb} while the collector depletion layer thickness is $T_{c.}$

While there are important applications for THz transistors in sub-mm-wave ICs, broad application of sub-mm-wave and THz radio links is constrained by very high atmospheric attenuation during heavy rain, dense fog, or very humid air [15, 16]. It is likely that the main application in THz-bandwidth transistors will be in ICs operating at microwave or lower mm-wave frequencies.

The application of THz-bandwidth transistors is not limited exclusively to the processing of near-THz signals. In the greatest number of modern transistor circuits (and with the limited exception of MMICs), the ratio of transistor bandwidth to signal frequency is typically of order 100:1 to

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1000:1. This large excess transistor bandwidth provides high circuit precision at the intended frequency of operation. ADCs and DACs demand transistor cutoff frequencies vastly exceeding the sample rate. Transistors with ~2 THz cutoff frequencies would also permit construction of negative feedback amplifiers with ~200 GHz feedback loop bandwidths and hence 20 dB feedback loop gain at 20 GHz. Such strong feedback, would greatly reduce amplifier intermodulation distortion. Given high excess transistor bandwidth, circuit distortion can also be reduced using translinear [17] and similar topologies.

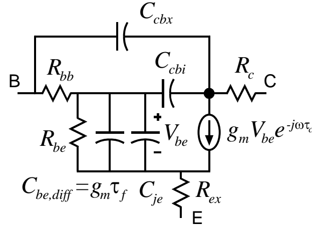


Figure 2: Simplified HBT small-signal equivalent circuit.

II. HBT Parameters and Figures-of-Merit

The small-signal parameters and cutoff frequencies of bipolar transistors are readily calculated from hand analysis. From this, scaling laws and scaling limits can be quickly identified. By here reviewing the development of HBT scaling laws, we seek to make evident the key challenges faced in developing THz transistors.

The device cross-section is shown in Figure 1. For simplicity, we will ignore the small effects of the emitter sidewall thickness W_{eb} and collector undercut W_{under}, and we will constrain W_E and W_c to scale proportionally. The small-signal equivalent circuit is shown in Figure 2. Here, $g_m = qI/kT$, I_C is the collector current, R_{ex} and R_{bb} the emitter and base parasitic resistances, C_{je} the emitter depletion capacitance, C_{cbx} and C_{cbi} the components of the collector-base capacitance C_{cb} external to and internal to R_{bb}, and τ_f the sum of base τ_b and collector τ_c transit times.

The collector transit time is $\tau_c \sim T_c / 2v_{eff}$ and the base transit time $\tau_b \sim T_b^2 / 2D_n + T_b / v_{eff}$. For InGaAs/InP DHBTs, typically the (InP) collector high-field velocity is $v_{eff} \sim 3.5 \cdot 10^7$ cm/s while the (InGaAs) base minority carrier diffusivity is $D_n \sim 40$ cm^2/s.

The emitter resistance is $R_{ex} = \rho_{ex} / A_E = \rho_{ex} / L_E W_E$, where the normalized emitter access resistivity ρ_{ex}. The base resistance is the sum of vertical access resistance through the base contacts, lateral semiconductor spreading resistance under the base contact, and spreading resistance under the emitter:

$$R_{bb} = R_{b,contact} + R_{spread,contact} + R_{spread}$$

$$\cong \frac{\rho_{b,v}}{2L_e W_{b,cont}} + \frac{\rho_s W_{b,cont}}{6L_e} + \frac{\rho_s W_E}{12L_e}, \quad (1)$$

where ρ_s is the base sheet resistance, and $\rho_{b,v}$ the base specific (vertical) contact resistivity. Similarly the collector-base capacitance is the sum of junction capacitances under the emitter and under the two base contacts:

$$C_{cb} = C_{cb,e} + C_{cb,excess} = \frac{\varepsilon L_e W_e}{T_c} + \frac{2\varepsilon L_e W_{eb}}{T_c}. \quad (2)$$

Equations (1,2) compute from the device structure three components to R_{bb} and two components to C_{cb}, while the standard simplified bipolar model (Figure 2) more approximately models the same structure with three elements, R_{bb}, C_{cbx}, and C_{cbi}, computed as follows [18]:

$$\begin{aligned} \tau_{cb} &= (R_{b,contact} + R_{spread,contact}/2)C_{cb,excess} \\ &\quad + (R_{b,contact} + R_{spread,contact} + R_{spread})C_{cb,e} \\ C_{cbi} &= \tau_{cb} / R_{bb} \\ C_{cbx} &= C_{cb} - C_{cbi} \end{aligned} \quad (3)$$

Heat and current density are paramount considerations. Ignoring lateral collector current spreading, Kirk effect limits the maximum collector current to:

$$I_{c,\max} \approx 2\varepsilon v_{eff} L_E W_E (V_{ce} + V_{ce,depletion}) / T_c^2, \quad (4)$$

where V_{ce} is the operating bias and $V_{ce,depletion}$ the bias voltage required to fully deplete the collector region. Finally, approximating heat flow as half-cylindrical at radii $r < L_E/2$ and as hemispherical at greater distances [19], the junction temperature rise of an isolated HBT on a thick substrate is

$$\Delta T \approx \frac{P}{\pi K_{InP} L_E} \ln\left(\frac{L_E}{W_E}\right) + \frac{P}{\pi K_{InP} L_E}. \quad (5)$$

K_{InP} is the substrate thermal conductivity and P the dissipated power.

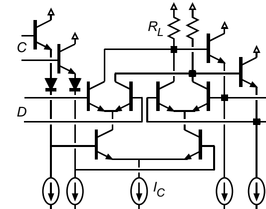


Figure 3: ECL latch. A master-slave latch is formed from two cascaded latches with opposite clock phases. C=clock, D=data, Q=latch output.

Transistor figures-of-merit can now be calculated. The transistor current-gain cutoff frequency f_τ is

$$\begin{aligned} 1/2\pi f_\tau &\cong (kT/qI_c)(C_{je} + C_{cbx} + C_{cbi}) + \tau_f \\ &\quad + (R_{ex} + R_c)(C_{cbx} + C_{cbi}), \end{aligned} \quad (6)$$

while the power-gain cutoff frequency $f_{\max}$ is

$$f_{\max} \cong \sqrt{f_\tau / 8\pi\tau_{cb}}. \quad (7)$$

$f_{\max}$ defines the highest frequency at which power gain can be obtained in a reactively-tuned amplifier; amplifiers with useful gain useful can be constructed at signal frequencies f_{signal} of approximately $f_{\max}/2$ or below. Finally, we require a transistor figure-of-merit for digital and mixed-signal speed. For this we use the maximum toggle frequency

$f_{\text{clk,max}} = 1/2T_{gate}$ of an emitter-coupled logic (ECL) master-slave (M-S) latch (Figure 3) configured as a 2:1 static frequency divider:

$$\begin{aligned} T_{gate} \approx\ & (\Delta V_L / I_C)(C_{je} + 6C_{cbx} + 6C_{cbi}) + \tau_f \\ & +(kT/qI_C)(0.5C_{je} + C_{cbx} + C_{cbi} + 0.5\tau_f I_C/\Delta V_L) \\ & + R_{ex}(-0.3C_{je} + 0.5C_{cbx} + 0.5C_{cbi} + 0.5\tau_f I_C/\Delta V_L) \\ & + R_{bb}(0.5C_{je} + C_{cbi} + 0.5\tau_f I_C/\Delta V_L)\ , \end{aligned} \tag{8}$$

where $\Delta V_L = I_C R_L$ is the logic voltage swing, R_L the load resistance, and I_C the collector current.

III. HBT Scaling Laws and Scaling Roadmap

Consider now how to increase by 2:1 the bandwidth of an arbitrary circuit using the transistor, requiring a 2:1 reduction of all capacitances and transit delays while maintaining constant all parasitic resistances, all bias and signal voltages, the transconductance g_m, and the operating current I_C.

We must first reduce transit times, hence we must reduce the collector thickness T_c by 2:1 and the base thickness T_b by slightly more than $2^{1/2}$:1. Reducing T_c by 2:1 would *increase* C_{cb} if junction areas were held constant; instead, we must reduce all junction areas by 4:1 to reduce C_{cb} in the desired 2:1 proportion. Because the emitter parasitic resistance R_{ex} must remain constant in the presence of 4:1 reduced emitter junction area, the emitter contact resistivity ρ_{ex} must be reduced 4:1. Because a fixed collector current I_c must be carried in 1/4 the emitter junction area, the current density J_E has increased 4:1. Given the 2:1 reduction in T_c, the Kirk effect (eq. (4)) permits this increased J_E, but device failure from emitter contact electromigration becomes a concern.

The required 4:1 reduction in junction areas can be obtained by either reducing junction widths or reducing junction lengths. Critically, it is device thermal resistance which (eq. (5)) determines this choice: reducing L_E with scaling will result in very rapid increases in self-heating. Instead, the desired 4:1 reduction in junction areas is obtained by maintaining a constant L_E but reducing all junction widths (W_E, W_{eb}, W_c) by 4:1. This results in a moderate logarithmic increase with scaling in the temperature *of an isolated HBT*. Minimum feature size then decreases in proportion to the inverse square of IC bandwidth.

Scaling of the base parameters is a final consideration. Because junction widths are varying as the inverse square of bandwidth, the two spreading components ($R_{spread,contact}$, R_{spread}) of R_{bb} become negligible in highly scaled (THz) devices. To maintain constant $R_{b,contact}$ in the presence of a 4:1 reduction in junction area, we must reduce 4:1 the base contact resistivity $\rho_{b,v}$.

Each 2:1 increase in device bandwidth requires a ~2:1 thinning of epitaxial layers, a 4:1 reduction in lithographic feature size, a 4:1 increase in current density, and a 4:1 reduction in metal-semiconductor contact resistivities. From these (Table 1) we show a scaling roadmap extending from the 256 nm through 32 nm generations. Amplifier noise figures and associated gain were determined from circuit simulations by adding standard noise generators to the device model (Figure 1). At the 64 nm generation, 1.0 THz amplifiers and 500 GHz digital logic becomes feasible.

Table 1 Bipolar transistor scaling laws and InP HBT scaling roadmap. The temperature rise ΔT is calculated at V_{CE} =1.5 Volts and L_E =2 μm

Parameter	scaling law	Gen. 3 (256 nm)	Gen. 4 (128 nm)	Gen 5 (64 nm)	Gen 5 (32 nm)
MS-DFF speed	γ^1	240 GHz	330 GHz	480 GHz	660 GHz
Amplifier center frequency	γ^1	430 GHz	660 GHz	1.0 THz	1.4 THz
Emitter Width	$1/\gamma^2$	256 nm	128 nm	64 nm	32 nm
Resistivity	$1/\gamma^2$	8 Ω-μm²	4 Ω-μm²	2 Ω-μm²	1 Ω-μm²
Base Thickness	$1/\gamma^{1/2}$	250 Å	212 Å	180 Å	180 Å
Contact width	$1/\gamma^2$	175 nm	120 nm	60 nm	30 nm
Doping	γ^0	7 10¹⁹ /cm²	7 10¹⁹ /cm²	7 10¹⁹ /cm²	7 10¹⁹ /cm²
Sheet resistance	$\gamma^{1/2}$	600 Ω	708 Ω	830 Ω	990 Ω
Contact ρ	$1/\gamma^2$	10 Ω-μm²	5 Ω-μm²	2.5 Ω-μm²	1.25 Ω-μm²
Collector Width	$1/\gamma^2$	600 nm	360 nm	180 nm	90 nm
Thickness	$1/\gamma$	106 nm	75 nm	53 nm	37.5 nm
Current Density	γ^2	9 mA/μm²	18 mA/μm²	36 mA/μm²	72 mA/μm²
$A_{collector}/A_{emitter}$	γ^0	2.4	2.9	2.8	2.8
f_τ	γ^1	520 GHz	730 GHz	1.0 THz	1.4 THz
$f_{\max}$	γ^1	850 GHz	1.30 THz	2.0 THz	2.8 THz
$V_{BR,CEO}$		4.0 V	3.3 V	2.75 V	?
ΔT		50 K	61 K	72K	83 K
I_E / L_E	γ^0	2.3 mA/μm	2.3 mA/μm	2.3 mA/μm	2.3 mA/μm
τ_f	$1/\gamma$	240 fs	180 fs	130 fs	95 fs
C_{cb}/I_c	$1/\gamma$	280 fs/V	240 fs/V	170 fs/V	120 fs/V
$C_{cb}\Delta V_{\text{logic}}/I_c$	$1/\gamma$	85 fs	74 fs	52 fs	36 fs
$R_{bb}/(\Delta V_{\text{logic}}/I_c)$	γ^0	0.47	0.34	0.26	0.23
$C_{je}(\Delta V_{\text{logic}}/I_C)$	$1/\gamma^{3/2}$	180 fs	94 fs	50 fs	33 fs
$R_{ex}/(\Delta V_{\text{logic}}/I_c)$	γ^0	0.24	0.24	0.24	0.24
670 GHz gain	--	--	4.3 dB	8.7 dB	12.8 dB
670 GHz Fmin	--	--	7.4 dB	5 dB	3.8 dB
1030 GHz gain	--	--	--	4.9 dB	7.9 dB
1030 GHz Fmin	--	--	--	7.3 dB	5.0 dB

IV. Scaling: Challenges and Limits

Contact resistivities, thermal resistivity, and reliability under high current density operation are the *critical* barriers to scaling. Contact resistivities must vary as the *inverse square* of circuit bandwidth; 2.5 $\Omega-\mu$m² base $\rho_{v,b}$ contact resistivity and 2 $\Omega-\mu$m² emitter ρ_{ex} access resistivity are required for the 64 nm (1 THz amplifiers) scaling generation, while ~1 $\Omega-\mu$m² are required for the subsequent generation. Resistivity of contacts deposited after atmospheric exposure is strongly influenced by surface oxides and cleaning procedures. For the emitter, with appropriate surface cleaning and passivation, ~ 1 $\Omega-\mu$m² resistivity is obtained [20], while solid-phase-reaction base contacts, which penetrate the oxides, provide 2-5 $\Omega-\mu$m² [21]. By depositing appropriate metals immediately after semiconductor growth and before removing the wafer from vacuum [22], contact resistivities

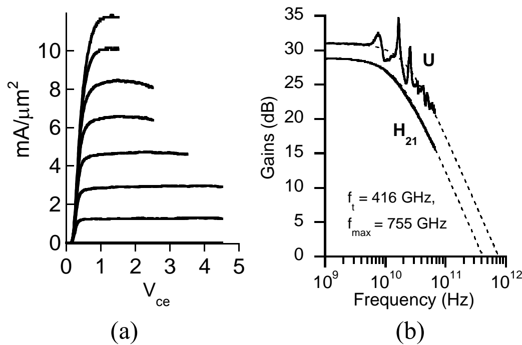
well below $1\,\Omega-\mu m^2$ have been obtained for the emitter. We are developing similar methods for forming the base contact.

V. Device Results

The 512 nm generation is now established in industrial pilot production, and the 256 nm generation has recently been transferred to industry. Figure 4 and Figure 5 show DC and RF characteristics of devices of this generation. 755 GHz f_{max} and 560 GHz simultaneous f_τ and f_{max} have been obtained.

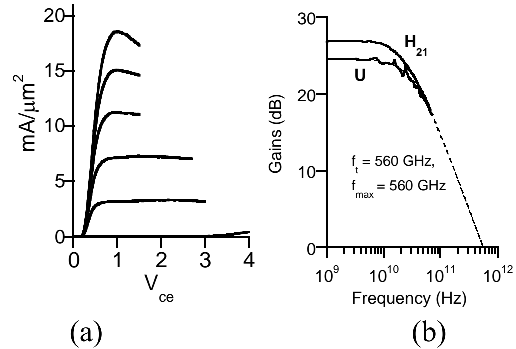
We are exploring a range of high-frequency integrated circuits using these scaled HBTs. Efforts include development of amplifiers for the 340 GHz band, and digital ICs with target 220 GHz clock rate, both using 256 nm generation HBTs. As a demonstration of the utility of wideband transistors even in lower-frequency (microwave) circuits, we have demonstrated operational amplifiers with 20-40 GHz loop bandwidths using 512 nm (350 GHz) DHBTs [23]. With such high loop bandwidths, the feedback loop transmission is high at low microwave frequencies, and the strong negative feedback results in very low intermodulation distortion.

The 128 nm and 64 nm generation HBTs are in development (Figure 8). Process development and fabrication runs at 128 nm are near completion, and device parameters are close to those of Table 1. Substantial effort has been devoted in the past year to development of contacts for the 64 and 32 nm generations. Both P-type and N-type contacts of resistivity sufficient for the 64 nm generation are feasible, as are N-contacts for the 32 nm generation. Robust fabrication processes must now be developed for these very small devices.



(a) (b)

Figure 4: Measured common-emitter characteristics (a) and RF gains (b) of a DHBT having T_c=150 nm, T_b=30 nm, and W_e=250 nm, biased at J_e=12 mA/µm^2. The DHBT exhibits $V_{br,ceo}$ =5.6V at I_c/A_e=10 kA/cm^2.



(a) (b)

Figure 5: Measured common-emitter characteristics (a) and RF gains (b) of a DHBT having T_c=70 nm, T_b=22 nm, and W_e=250 nm biased at J_e=13 mA/µm^2. The DHBT exhibits $V_{br,ceo}$ =3.3V at I_c/A_e=15 kA/cm^2.

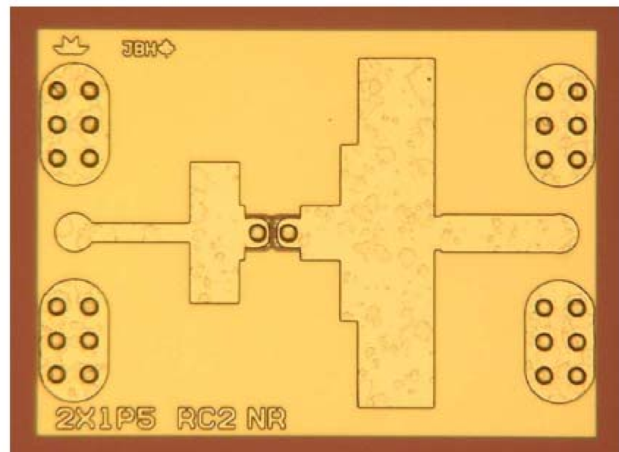


Figure 6: Single-stage InP DHBT common base 324 GHz power amplifier with microstrip lines on thick 10µm BCB. The IC was fabricated in Teledyne's 256 nm InP DHBT technology The compact die measures 300 µm by 414 µm; the amplifier produces 4.8 dB gain at 324 GHz.

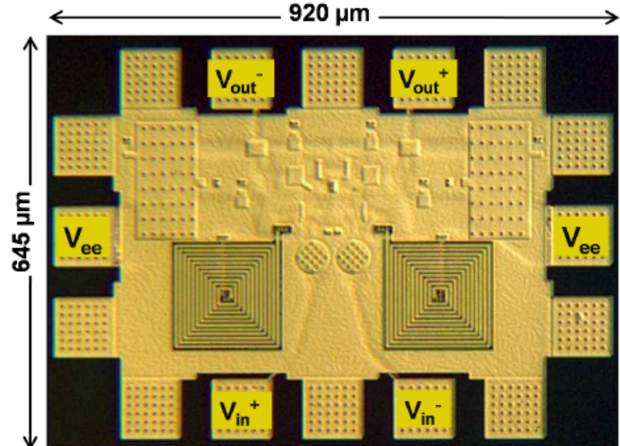


Figure 7: Single-loop current-mode microwave feedback amplifier in Teledyne's 500 nm InP DHBT technology. The amplifier dissipates only 1.0 W, yet exhibits a 53 dBm output-referred 3rd-order intercept at 2 GHz.

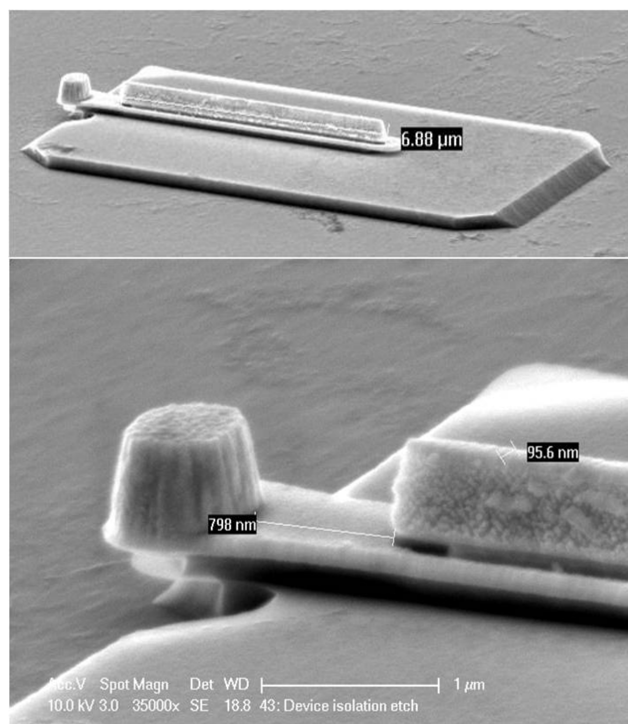


Figure 8: Electron Micrographs of 128 HBT in fabrication, immediately before deposition of the collector contact. The emitter and base contacts are both 100-120 nm wide.

VI. Conclusions

Electron device bandwidths are increased by reducing junction dimensions (lithographic scaling), reducing layer thicknesses (epitaxial scaling) and by reducing Ohmic contact resistivities and thermal resistivities. With bipolar transistors, low required contact resistivities and high required current and power densities are the key impediments to scaling. FETs face the same constraints, and must in addition have very high capacitance density gate dielectrics. With bipolar transistors, contact resistivities sufficient for the 64 nm generation have been reproducibly demonstrated. Fabrication processes must be developed; THz ICs appear clearly feasible.

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