On the Feasibility of few-THz Bipolar Transistors

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***Abstract*—We review the limits faced in scaling of InP-based bipolar transistors for increased device bandwidth. Emitter and base contact resistivities and IC thermal resistance are the major limits to increased device bandwidth. Devices with 1-1.5 THz simultaneous f_τ and f_{max} are feasible; these will enable 750 GHz monolithic amplifiers and medium-scale digital ICs at ~400-500 GHz clock rate.**

I. Introduction

Transistor bandwidths are rapidly increasing, and THz-bandwidth devices will soon be realized in both III-V and Si and SiGe technologies. 250 nm Indium Phosphide (InP) heterojunction bipolar transistors (HBTs) have demonstrated 416 GHz f_τ and 755 GHz f_{max} [1], and 125 nm devices now in development are expected to be $\sqrt{2}$:1 faster. InP HEMTs [2] attain over 500 GHz f_τ. Such wideband III-V process technologies have historically served low-integration-scale high-frequency applications, but are now under considerable competitive pressure from silicon VLSI.

Production 130 nm Si/SiGe HBTs [3] have obtained 350 GHz f_{max} and 300 GHz f_τ. Silicon CMOS processes exhibit ~450 GHz f_{max} [4]. 45 nm [5] and subsequent processes should be significantly faster. It is likely that Si CMOS IC processes will exceed 1 THz f_τ and f_{max} in the next few years.

SiGe BiCMOS may render III-V transistors obsolete. Similarly, RF and mm-wave CMOS may capture the bulk of the markets now addressed by SiGe BiCMOS. It is today difficult to judge the probable outcome. A key advantage of SiGe bipolar transistors over InP has been their integration into BiCMOS processes; do the markets justify the cost of adding high-quality bipolar transistors to 90 nm and 65 nm CMOS processes? MOSFETs now achieve cutoff frequencies exceeding those of SiGe bipolar transistors, but their poor breakdown voltage and variable DC parameters makes mixed-signal design difficult [6]; can ADC designers work effectively with such devices, or will bipolar processes be retained to address such applications? Serious difficulties will be faced in scaling CMOS processes beyond the 22 nm generation; MOSFETs with InGaAs and InP channels are being explored as one of several high-risk alternatives to scale beyond this generation [7,8,9] .

InP bipolar transistors obtain high bandwidth with less aggressive scaling and with simpler fabrication processes than are required for Si devices of comparable bandwidth. This is an advantage for low-volume fabrication of small-scale high-performance circuits. InP HBTs obtain significantly larger breakdown voltage that SiGe HBTs of a comparable bandwidth. This is an advantage for both mixed-signal ICs and mm-wave power amplifiers. InP HBTs appear to be far from their scaling limits, and cutoff frequencies beyond 1.5 THz appear to be feasible; this suggests new potential applications at sub-mm-wave frequencies.

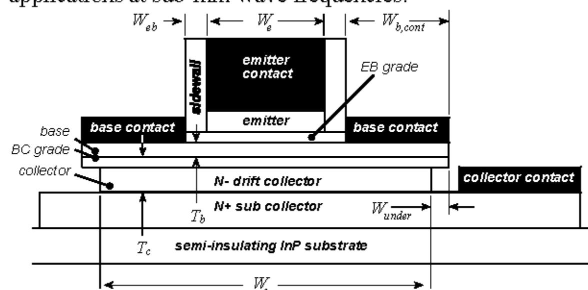

Figure 1: HBT cross-section and critical dimensions. The emitter stripe extends a distance L_e perpendicular to the figure. W_e is the emitter junction width, W_{eb} the base-emitter sidewall spacer thickness, $W_{b,cont}$ the width of the base Ohmic contact, and W_{under} the undercut of the collector junction under the base contacts.

II. InP Bipolar Transistors

Present InP HBTs [1] with 250 nm minimum feature size have attained 755 GHz power-gain cutoff frequencies (f_{max}) simultaneous with 416 GHz current-gain cutoff frequencies (f_τ) ; devices at the 65 nm generation should attain cutoff frequencies well above 1 THz. This would enable digital ICs at ~450 GHz clock rate, 750 GHz monolithic power amplifiers, and compact ICs for sub-mm-wave systems.

Table 1 summarizes HBT scaling laws [10] and provides a scaling roadmap through 63 nm. The principles are straightforward. If we wish to improve by 2:1 the bandwidth of *any* circuit employing the HBT, we must reduce by 2:1 all transit delays and capacitances while retaining constant all resistances, all bias and signal voltages, and all bias and signal currents. Thinning the collector depletion layer by 2:1 will reduce the collector depletion-layer transit time by the required proportion but doubles junction capacitances per unit area; the collector and emitter junction areas must therefore also be reduced 4:1 so as to obtain the required 2:1 reduction in depletion capacitances. The emitter junction area has

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decreased 4:1; yet the emitter current and the emitter access resistance must both remain constant. Both the emitter current density and the emitter specific access resistivity (resistance normalized to the contact area) must both be reduced 4:1. The 4:1 required increase in current density is consistent with the space-charge-limited current density (the Kirk effect) as this varies as the inverse square of depletion layer thickness.

In submicron InP HBTs, base access resistance is *dominated* by the Ohmic contact, the contact width is much less than the contact transfer length, and consequently the base resistance is approximately the base specific contact resistivity divided by the base Ohmic contact area. With a 4:1 reduction in junction areas, the base specific contact resistivity must thus be reduced 4:1.

Table 1: Bipolar transistor scaling laws and InP HBT scaling roadmap.

Parameter	scaling law	Gen. 2 (500 nm)	Gen. 3 (250 nm)	Gen. 4 (125 nm)	Gen 5 (62.5nm)
MS-DFF speed	γ^1	150 GHz	240 GHz	330 GHz	440 GHz
Amplifier center frequency	γ^1	245 GHz	430 GHz	660 GHz	750 GHz
Emitter Width	$1/\gamma^2$	500 nm	250 nm	125 nm	62.5 nm
Resistivity	$1/\gamma^2$	16 Ω-µm²	8 Ω-µm²	4 Ω-µm²	2 Ω-µm²
Base Thickness	$1/\gamma^{1/2}$	300Å	250 Å	212 Å	180 Å
Contact width	$1/\gamma^2$	300 nm	175 nm	120 nm	70 nm
Doping	γ^0	$7\ 10^{19}$ /cm²	$7\ 10^{19}$ /cm²	$7\ 10^{19}$ /cm²	$7\ 10^{19}$ /cm²
Sheet resistance	$\gamma^{1/2}$	500 Ω	600 Ω	708 Ω	830 Ω
Contact ρ	$1/\gamma^2$	20 Ω-µm²	10 Ω-µm²	5 Ω-µm²	5 Ω-µm²
Collector Width	$1/\gamma^2$	1.2 µm	0.60 µm	0.36 µm	0.20 µm
Thickness	$1/\gamma$	1500 Å	1060 Å	750 Å	530 Å
Current Density	γ^2	4.5 mA/µm²	9 mA/µm²	18 mA/µm²	36 mA/µm²
$A_{collector}/A_{emitter}$	γ^0	2.4	2.4	2.9	2.8
f_τ	γ^1	370 GHz	520 GHz	730 GHz	1.0 THz
f_{max}	γ^1	490 GHz	850 GHz	1.30 THz	1.5 THz
$V_{BR,CEO}$		4.9 V	4.0 V	3.3 V	2.75 V
I_E/L_E	γ^0	2.3 mA/µm	2.3 mA/µm	2.3 mA/µm	2.3 mA/µm
τ_f	$1/\gamma$	340 fs	240 fs	180 fs	130 fs
C_{cb}/I_c	$1/\gamma$	400 fs/V	280 fs/V	240 fs/V	190 fs/V
$C_{cb}\Delta V_{logic}/I_c$	$1/\gamma$	120 fs	85 fs	74 fs	57 fs
$R_{bb}/(\Delta V_{logic}/I_c)$	γ^0	0.76	0.47	0.34	0.39
$C_{je}(\Delta V_{logic}/I_C)$	$1/\gamma^{3/2}$	380 fs	180 fs	94 fs	50 fs
$R_{ex}/(\Delta V_{logic}/I_c)$	γ^0	0.24	0.24	0.24	0.24

HBT lithographic scaling laws are now primarily driven by thermal constraints. Approximating heat flow as half-cylindrical at radii $r < L_E/2$ and as hemispherical at greater distances the junction temperature rise of an isolated HBT on a thick substrate is

$$\Delta T \approx \frac{P}{\pi K_{InP} L_E}\ln\left(\frac{L_E}{W_E}\right) + \frac{P}{\pi K_{InP} L_E}. \qquad (1)$$

K_{InP} is the substrate thermal conductivity and P the dissipated power. We must reduce the emitter junction area $L_E W_E$ by 4:1; maintaining constant emitter stripe length L_E while reducing the stripe width W_E by 4:1 results in only a moderate (logarithmic) increase in junction temperature with scaling.

We have now found the requirements for HBT scaling; the full scaling laws are shown in Table 1. The table shows not only transistor cutoff frequencies (f_τ, f_{max}) but also key time constants (e.g. $C_{cb}\Delta V_{logic}/I_c$) associated with digital gate delay [10]. Transistors for mm-wave amplification are designed for highest f_{max} and for $f_\tau > f_{max}/2$, while HBTs for mixed-signal ICs are designed for minimum ECL gate delay [10]; transistors designed for highest feasible f_τ but having $f_{max} << f_\tau$ are of extremely limited utility in circuits.

Contact and thermal resistivities are presently the most serious barriers to scaling. On large ICs, thermal resistance places the most severe constraint. On an IC, transistor spacings D are small and must scale in inverse proportion to circuit bandwidth in order to scale wiring delays. Heat flow is then approximately half-cylindrical at radii $r < L_E/2$, hemispherical at radii $L_E/2 < r < D/2$, and planar at radii $D/2 < r < T_{sub}$, where T_{sub} is the substrate thickness. The substrate temperature rise is then

$$\Delta T_{InP} \sim \Delta T_{cylindrical} + \Delta T_{hemisperical} + \Delta T_{planar}$$
$$= \left(\frac{P}{\pi K_{InP} L_E}\right)\ln\left(\frac{L_e}{W_e}\right) + \left(\frac{P}{\pi K_{InP}}\right)\left(\frac{1}{L_E} - \frac{1}{D}\right) + \left(\frac{P}{K_{InP}}\right)\frac{T_{sub} - D/2}{D^2} \qquad (2)$$

In addition to the logarithmic temperature increase arising from narrow emitters, at fixed T_{sub} scaling causes ΔT_{planar} to scale in proportion to the square of circuit bandwidth. The planar term can be reduced by extreme thinning of the substrate using wafer lapping or thermal vias [11].

Given a square IC of linear dimensions W_{chip} on a large copper heat sink, the package thermal resistance is approximated by planar and spherical regions, giving $\Delta T_{package} \cong (1/2 + 1/\pi)(P_{chip}/K_{Cu} W_{chip})$. Because transistor spacings vary as the inverse of IC bandwidth, W_{chip} must vary by the same law, and $\Delta T_{package}$ therefore increases in direct proportion to increases in circuit bandwidth with scaling.

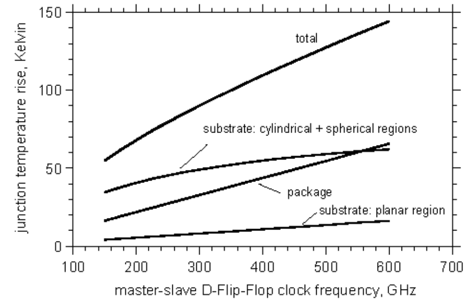

Figure 2: Calculated package and substrate temperatures rise, as a function of digital clock rate, for a 2048-HBT CML integrated circuit.

Using these thermal relationships, and scaling from an existing UCSB/Teledyne 150 GHz IC design the dissipation, wire lengths, transistor parameters, and circuit bandwidths, we can project (Figure 2) the resulting total junction temperature rise of a 2048-HBT CML digital integrated circuit as a function of digital clock rate. The substrate is thinned

aggressively with the assumed use of thermal vias: $T_{sub} = 40\,\mu\text{m}\cdot(150\,\text{GHz}/f_{clock})$ to obtain these results.

IC design constraints are application specific, hence Figure 2 only illustrates ΔT calculation. It appears however that 450 GHz f_{clock} is thermally feasible in 2000-transistor ICs, an integration scale typical of many ADCs and DACs. Higher clock rates than indicated in Figure 2 may be thermally feasible given improved circuit design. Adding transimpedance input termination to a logic gate can provide low-impedance loading of interconnects for low associated delay while requiring less stage bias current than required for resistive loading of equal termination impedance [12] .

Consider scaling limits associated with contact resistivities. These must decrease in proportion to the inverse *square* of circuit bandwidth; 5 $\Omega-\mu\text{m}^2$ base $\rho_{v,b}$ contact resistivity and 2 $\Omega-\mu\text{m}^2$ emitter ρ_{ex} access resistivity are required for the 62 nm generation (440 GHz digital clock rate). In addition to the effects of doping and barrier potential, resistivity of ***ex-situ*** deposited contacts is strongly influenced by surface oxides and cleaning procedures. For the base contacts, we observe the lowest resistivity with Pd solid-phase-reaction contacts [13], which penetrate oxides.

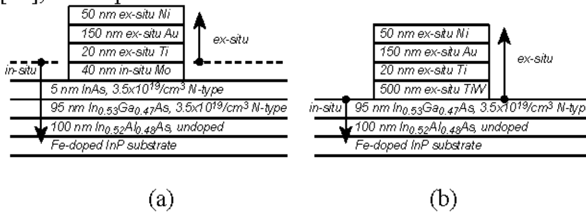

Figure 3: Layer structures for < 10^{-9} Ω-cm^2 resistivity emitter contacts. (a) *in-situ* Molybdenum contacts and (b) TiW contact deposited *ex-situ* after UV-ozone and NH_3OH surface treatment.

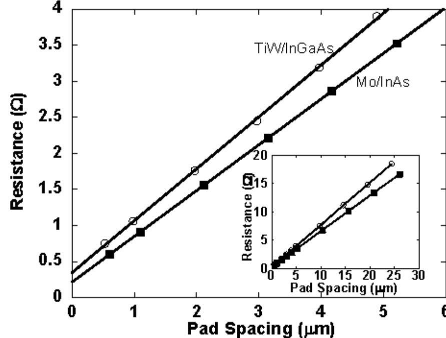

Figure 4: Resistance measurement, by the TLM method with test structures of 26.6 μm width, for TiW/InGaAs ex-situ and Mo/InAs in-situ emitter Ohmic contacts. The extracted contact resistivities are 0.7 and 0.5 Ω-μm^2 respectively.

For the 250 nm-generation HBTs [14,15] developed at UCSB during 2005-2006, the emitter access resistivity was 5 $\Omega-\mu\text{m}^2$, while the base access resistivity was ~3-5 $\Omega-\mu\text{m}^2$. Development of InP HBTs meeting the 125 nm scaling goals (Table 1) thus required substantially less resistive emitter contacts. Identifying surface oxides as a key contributor to contact resistance, we have recently fabricated emitter Ohmic contacts [16] by depositing Molybdenum contact metal in the molecular beam epitaxy (MBE) growth system immediately after growth of the N+ InAs emitter cap layer (Figure 3a). The contact is deposited before the semiconductor surface is exposed to air, and oxidation is avoided. Further, Molybdenum is refractory, and significant intermixing at the interface of the metal and semiconductor is thereby avoided. By this method (Figure 4), 0.5 $\Omega-\mu\text{m}^2$ contact resistivity is obtained. These ***in-situ*** contacts are readily integrated into the InP HBT process flow. A second method for forming (Figure 3b) low-resistance contacts is to deposit the metal ***ex-situ*** after first removing the surface oxides. We have found empirically that low 0.7 $\Omega-\mu\text{m}^2$ contact resistivity is obtained if, immediately prior to TiW contact metal deposition, the wafer surface is first exposed to UV-generated ozone and subsequently rinsed in concentrated ammonia.

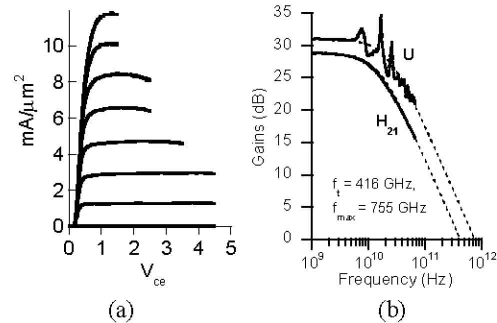

Figure 5: Measured common-emitter characteristics (a) and RF gains (b) of a DHBT having T_c=150 nm, T_b=30 nm, and W_e=250 nm, biased at J_e=12 mA/μm^2. The DHBT exhibits $V_{br,ceo}$ =5.6V at I_c/A_e=10 kA/cm^2, and shows ~ 52 K self-heating at 15 mW/μm^2 dissipation.

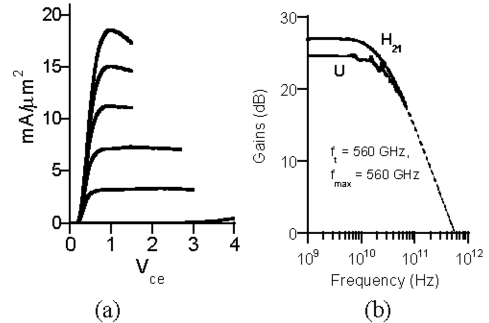

Figure 6: Measured common-emitter characteristics (a) and RF gains (b) of a DHBT having T_c=70 nm, T_b=22 nm, and W_e=250 nm biased at J_e=13 mA/μm^2. The DHBT exhibits $V_{br,ceo}$ =3.3V at I_c/A_e=15 kA/cm^2.

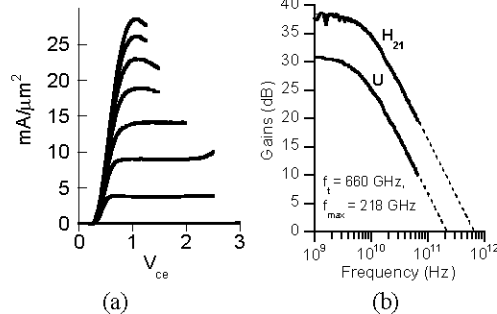

Figure 7: Measured common-emitter characteristics (a) and RF gains (b) of a DHBT having T_c=60 nm, T_b=14 nm, and W_e=400 nm biased at J_e=13 mA/μm^2. The DHBT exhibits $V_{br,ceo}$ =3.0V at I_c/A_e=10 kA/cm^2.

The target emitter access resistivity (Table 1) is the sum of contact resistance, bulk semiconductor resistance, and transport effects. Electron degeneracy in the emitter-base depletion layer contributes an effective increase in the aggregate emitter resistance, proportional to $1/m^*_{InP}$, of ~1.0 $\Omega - \mu m^2$. Excessively thick emitter depletion layers, or poorly-graded or lightly-doped InP/InGaAs or InGaAs/InP heterojunctions can contribute significant resistance.

Including the effects of emitter-base degeneracy, the emitter and base contact resistivities we now achieve are sufficient to meet the requirements for both the 125 nm and 65 nm scaling generations. Junction widths must be reduced and epitaxial layers thinned, but this simply requires efforts, albeit extensive, in development of the necessary device fabrication processes. Transistors with simultaneous 1.0 THz f_τ and 1.5 THz f_{max} appear to be feasible. Such transistors would enable 450 GHz digital clock rates and 750 GHz power amplifiers. We are now developing the 125 nm scaling generation device of Table 1. With future efforts to further reduce the base and emitter contact resistivities, requirements for the 31 nm scaling generation may be met. This would be a device $\sqrt{2}:1$ faster than the 62 nm device of Table 1. Figure 5, Figure 6, and Figure 7 show recent results [1,15,17]. Dielectric sidewall processes [18] are being developed [19, 20] to provide the yield necessary to fabricate mixed-signal ICs at the complexity of 1,000-10,000 transistors.

III. InP vs. SiGe: Bipolar Transistors

We now examine scaling requirements for Si/SiGe bipolar transistors. We have limited knowledge of the limits of SiGe process steps, hence only general observations are made

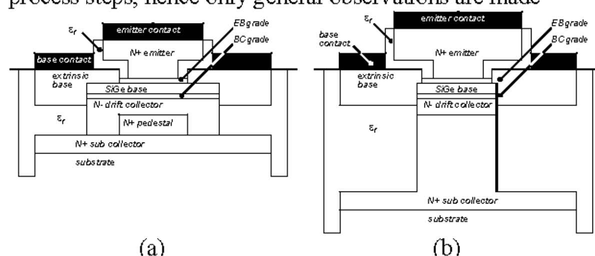

Figure 8: Device Schematic (a) of typical Si/SiGe HBT, and a device (b) with a tall etched collector post to which the emitter window is tightly aligned.

For extremely small devices, Ohmic contact resistances dominate over bulk semiconductor resistivities, hence the comparative limits upon bulk resistivity are of only secondary importance in comparing the ultimate high-frequency potential of Si/SiGe and InP HBTs. The collector velocity is lower (10^7 cm/s) in Si than in InP ($3.5 \cdot 10^7$ cm/s), and the contact resistivities (~10 $\Omega - \mu m^2$) of typical (but not state-of-art) self-aligned silicide contacts are ~10:1 higher than those of InP contacts [21].

If a simple device structure (Figure 1) is considered, the scaling potential of SiGe and InP HBTs are easily compared. With 3.5:1 smaller electron velocity, to achieve equal τ_c, C_{cb}, and $C_{cb}\Delta V_{logic}/I_{c,Kirk}$, the SiGe device must have 3.5:1 smaller collector thickness and 3.5:1 smaller emitter and collector junction areas. The areas of junctions and contacts are proportionally reduced, hence for equal R_{ex} and R_{bb} the required resistivities of emitter and base contacts are 3.5:1 lower for the SiGe device, yet the actual resistivities are typically 10:1 higher. Since the scaling laws require contact resistivity to vary as the inverse square of device bandwidth, this suggests that SiGe HBTs should attain $\sqrt{35}:1$ -- about 6:1 -- smaller bandwidth than InP HBTs. When base spreading and link resistance are considered, the performance disparity further increases.

To attain their very high bandwidth, SiGe HBTs employ emitter and base contacts much larger than the associated junction areas (Figure 8a). The N+ polysilicon emitter growth forms a flared emitter structure, providing wide emitter contacts to narrow emitter junctions. The growth of a P+ polysilicon extrinsic base over a SiO_2-filled trench provides a wide base contact without a proportional increase in the collector junction area and C_{cb}. The required base contact resistivity is thereby reduced. The collector pedestal implant provides a similar benefit.

We cannot project the detailed difficulties faced in further scaling these device structures, but some general features are clear. For a $\gamma:1$ increase in transistor bandwidth, the junction widths vary as γ^{-2} but layer thicknesses only as γ^{-1}. Consequently, in future more highly scaled devices the lateral ion straggle will reduce the utility of the implanted collector pedestal, and this structure may be omitted. If contact resistivities cannot be reduced, then junction areas must be reduced in scaled devices while maintaining constant areas for the emitter and base contacts. The device then evolves into the form of Figure 8b. Overlap capacitances between the extrinsic base and the extrinsic emitter, and fringing capacitances between the extrinsic base and the N+ collector post then limit performance. It therefore appears that even with complex device structures now typical of SiGe (Figure 8a), small transistors must use relatively small contacts, and each $\gamma:1$ increase in transistor bandwidth requires a $\gamma^2:1$ reduction in the emitter and base contact resistivities. As with InP HBTs, efforts to reduce contact resistivities are of substantial importance to future scaling of SiGe devices.

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