# Heterodyne Locking of an Integrated Optical Phase-Locked Loop

S. Ristic[1], A. Bhardwaj[1], M. J. Rodwell[1], L. A. Coldren[1,2], and L. A. Johansson[1]
[1]Department of Electrical and Computer Engineering
[2]Materials Department
University of California, Santa Barbara
Santa Barbara, USA
ristic@ece.ucsb.edu

***Abstract*—We demonstrate proof-of-concept heterodyne locking of the first optical phase-locked loop photonic integrated circuit. The circuit contains two sampled-grating distributed reflector lasers monolithically integrated with optical amplifiers, multimode interference splitters/couplers, and high-speed modulators and photodetectors.**

## I. Introduction

An optical phase-locked loop (OPLL) is a control system that exhibits both essential similarities and fundamental differences when compared to its RF counterpart. In an RF phase-locked loop (PLL), a mixer is used to detect a phase difference between an input signal and an output of a local voltage-controlled oscillator (VCO). The mixer produces a phase error signal that is filtered and applied to the VCO, tuning its output frequency to have a fixed phase relation with the input signal frequency. In an OPLL, however, a photodetector detects a phase difference between an input optical signal and an output of a local current-injection tunable laser, which effectively plays a role of a current-controlled oscillator (CCO) and is a direct equivalent of the VCO [1]. The phase error signal produced by the photodetector is filtered and applied to the CCO, tuning its output frequency to have a fixed phase relation with the input optical signal frequency. This locking can be implemented in a homodyne fashion, where the frequencies of the input light and the CCO output light are the same, or in a heterodyne fashion, where these frequencies are different (also referred to as offset locking). Because in heterodyne locking the photodetector produces a beat signal at an offset frequency, the beat signal is usually down-converted by mixing with an RF reference at the same frequency in order to generate the phase error signal that tunes the CCO.

There are many applications that utilize homodyne and heterodyne locking. For example, homodyne locking provides high receiver sensitivities [2] and can be used for coherent demodulation in double-sideband suppressed carrier (DSB-SC) communications [3]. Heterodyne locking of several "slave" lasers at the same frequency, which is offset relative to a reference "master" laser's frequency, can be used to produce a high-power coherent beam combination (CBC) [4]. In addition, heterodyne locking of two lasers has been successfully demonstrated in producing coherent optical beats with frequencies in the GHz region [5]. This single-sideband source can find many applications in microwave photonics.

Unlike an RF PLL, an OPLL is not easily locked. In an RF PLL, the RF oscillator is spectrally pure, and the feedback loop bandwidth is relatively large in comparison to the frequency of the input signal. The large loop bandwidth can easily compensate for the small phase noise of the RF oscillator. In an OPLL, however, the tunable laser linewidth can be in the MHz range, and the feedback loop bandwidth is small compared to the frequency of the input signal, which is ~193 THz (1550 nm). The feedback loop bandwidth is typically smaller, and its latency is larger, compared to the RF PLL because of the large size of optical components and interconnects. Consequently, for successful locking of an OPLL, researchers have used either a very narrow linewidth lasers (kHz range) with large and slow feedback loops [6], or wide linewidth semiconductor lasers with very compact bulk optics necessary to achieve small loop latencies [5], [7].

Recently, we have demonstrated homodyne locking of the first OPLL photonic integrated circuit (OPLL-PIC) [8]. The OPLL-PIC is monolithically integrated, and its compactness allows the use of wide linewidth tunable semiconductor lasers. The small OPLL-PIC is robust and provides for easy packaging. In this work, we demonstrate proof-of-concept heterodyne locking the OPLL-PIC.

## II. An Optical Phase-Locked Loop Photonic Integrated Circuit

Fig. 1 shows a schematic of an OPLL-PIC and the external feedback electronics used in the heterodyne experiment. In

This work is supported by DARPA under United States Air Force Contract #FA8760-08-1-7856.

this section, we describe the OPLL-PIC. The details about the feedback loop and the heterodyne locking experiment are presented in Section III.

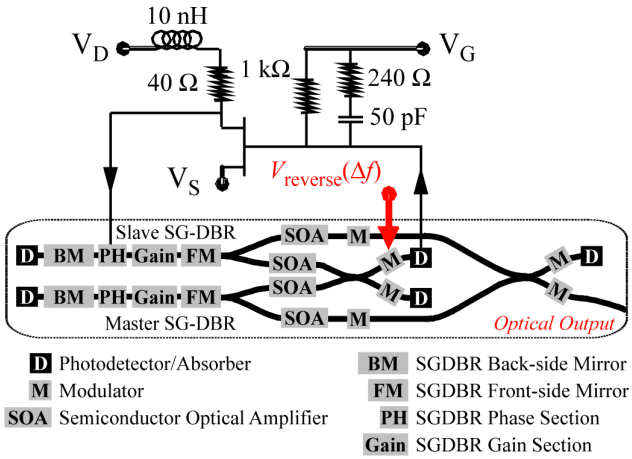


Figure 1. A schematic of the OPLL-PIC and the electronic feedback circuit used in a heterodyne locking experiment.

The monolithically integrated OPLL-PIC contains two widely tunable sampled-grating distributed reflector (SG-DBR) lasers, as well as semiconductor optical amplifiers (SOAs), multimode interference splitters/couplers (MMIs), and high-speed modulators and photodetectors. Light from each SG-DBR laser is split equally using a 90-µm-long 1x2 MMI, and each of the four output components is amplified using a 400-µm-long SOA. After amplification, the outputs from the two SG-DBR lasers are combined in two different 340-µm-long tunable 2x2 MMIs. One of the two MMIs is part of the OPLL-PIC feedback loop, and it has a 250-µm-long high-speed modulator followed by a 50-µm-long high-speed photodetector on each of its two output waveguides. The two photodetectors are used to provide the phase error signal to the feedback loop and can be used either separately or in a balanced pair configuration. The other MMI is part of the OPLL-PIC output. This MMI has a high-speed modulator on each of its two input waveguides, and similar to the feedback MMI, it also has a high-speed modulator on each of the two output waveguides. The output MMI, however, has a high-speed photodetector following a high-speed modulator only on one of its two output waveguides. This photodetector is used to monitor the coherent output beat signal in the electrical domain. The other output waveguide of the MMI is used to monitor the output beat signal from the output of the OPLL-PIC in the optical domain. The output waveguides are curved (7º) and their facets are anti-reflection coated in order to minimize reflections. The length of the OPLL-PIC is 6.6 mm, and the width is 0.45 mm. Fig. 2 shows a scanning electron microscope (SEM) image of the OPLL-PIC mounted on a carrier and wire-bonded. As can be seen in Fig. 2, there are four 100 µm x 100 µm G-S-G-S-G-S-G RF pads (150 µm pitch) used for direct probing of the high-speed modulators and photodetectors in both feedback and output sections of the OPLL-PIC.

Our monolithic integration platform is referred to as the "Offset Quantum Well Platform" [9]. The epitaxial structure is grown on a 2-inch S-doped InP wafer using Metalorganic Chemical Vapor Deposition (MOCVD). An "active" 119-nm-thick multiple-quantum-well (MQW) region that provides gain is grown on top of a "passive" 300-nm-thick 1.4Q layer. The passive layer is used to guide light as well as provide modulation either via carrier plasma effect, in the forward-bias operation of the modulator diodes and phase sections of the SG-DBR lasers, or via the Franz-Keldysh effect, in the reverse-bias operation of the modulator diodes. The active devices (SOAs, SG-DBR gain sections, and photodetectors) are defined by wet etching, after which the gratings in the back-side and front-side SG-DBR laser mirrors are defined by Electron Beam Lithography. Subsequently, the p-cladding regrowth is done, and surface-ridge waveguides are wet etched. The rest of the main fabrication steps include dry etching and deposition of top-side n-contacts (used for high-speed modulators and photodetectors), BCB patterning for high-speed modulators and photodetectors, p-contact metallization, proton implant isolation of passive waveguide sections between devices, wafer thinning, and back-side n-contact metallization (used for all of the low-speed devices).

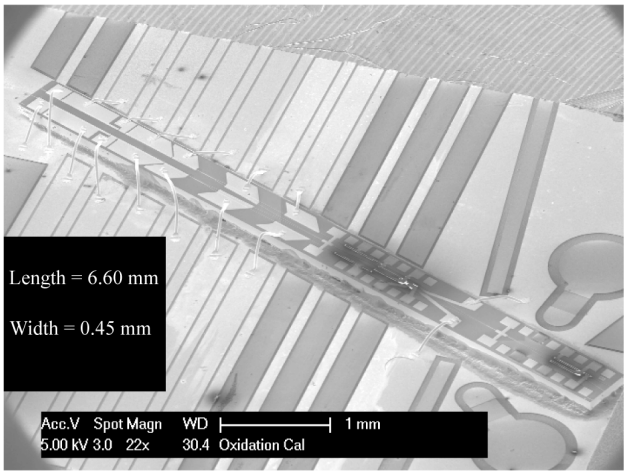


Figure 2. An SEM image of a fully fabricated OPLL-PIC after mounting on a test-carrier and wire-bonding.

## III. Heterodyne Locking Demonstration

As shown in Fig. 1, in the heterodyne locking of two SG-DBR lasers, one laser plays the role of the CCO (the slave laser), and its frequency is tuned by current injection into the phase section [10]. SG-DBR lasers offer several key advantages for OPLL applications. Their tuning sensitivities are ~20 GHz/mA, and they are an order of magnitude larger than those of the semiconductor lasers typically used in OPLL applications [5]. Their large sensitivities provide large loop gains and make OPLLs more stable. In addition, SG-DBR lasers have more than 40 nm (>5 THz) of quasi-continuous wavelength tuning range. Consequently, the OPLL-PIC can generate coherent optical beams at very high frequencies and can also provide broadband wavelength operation in homodyne applications. Fig. 3 illustrates this point, where a discrete incremental detuning of one integrated, unlocked SG-

DBR laser relative to the other is plotted. Lastly, unlike distributed feedback (DFB) lasers [5], SG-DBR lasers do not exhibit phase sign inversion when tuned via current injection into the phase section. It is hard to compensate this phase inversion using feedback electronics.

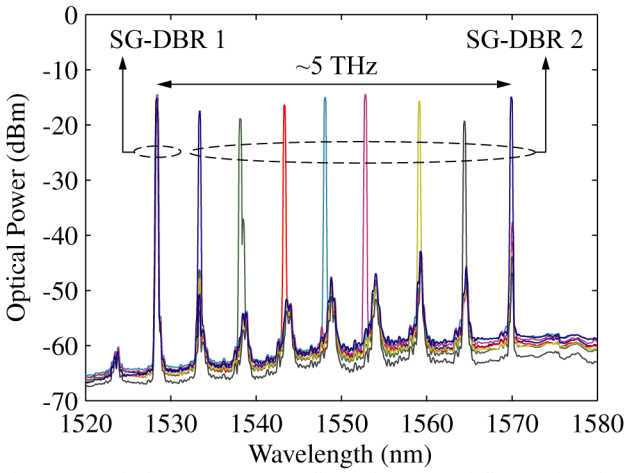


Figure 3. Optical spectra corresponding to incremental discrete detuning between the two on-chip unlocked SG-DBR lasers.

The relatively large linewidth that is characteristic of the SG-DBR laser is dominated by low-frequency jitter [11] and therefore can be well compensated by using the compact feedback loops achievable with monolithic integration. We measure linewidths of our lasers to be between 10 MHz and 50 MHz using a 30-μs-delay self-homodyne technique. Fig. 4 shows the combined linewidth of two integrated unlocked SG-DBR lasers to be ~300 MHz when measured using an external photodetector and electrical spectrum analyzer.

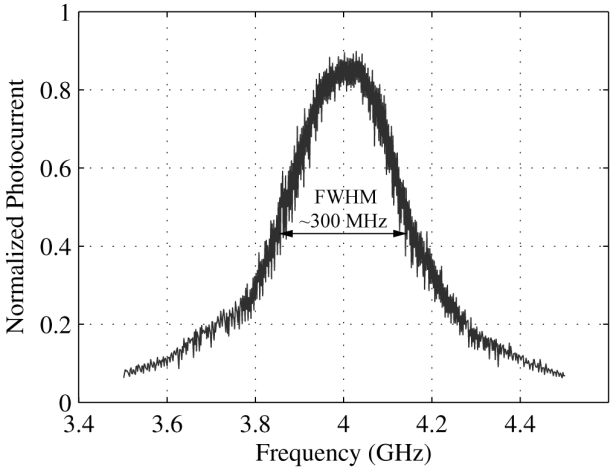


Figure 4. Combined linewidth of two unlocked integrated SG-DBR lasers.

In the heterodyne locking of the first integrated OPLL, we do not use an external mixer, which, as explained in Introduction, is a common practice [1]. Rather, for a proof-of-concept demonstration, we utilize sideband locking. In this scheme, the frequencies of the two SG-DBR lasers are detuned by the amount corresponding to the desired coherent beat frequency, *i.e.*, $\Delta f$. The combined laser outputs are then modulated with a high-speed modulator at the output of the feedback 2x2 MMI at the same frequency $\Delta f$. As shown in Fig. 1, the modulator is voltage-driven in the reverse bias regime, where the drive voltage ($V_{\text{reverse}}$) is applied using a microwave synthesizer. As the detuning frequency and the modulation frequencies are the same, a sideband of one laser occurs at the same frequency as the center frequency of the other laser, and sideband locking becomes possible. A phase error current signal is generated in the photodetector and provided as an input to the feedback electronic circuit, where it is amplified and filtered. Subsequently, the phase error current signal is applied to the phase section of the slave SG-DBR laser, adjusting its output frequency to have a fixed phase relation to the output frequency of the master SG-DBR laser.

A FET transistor in the feedback loop is used to amplify and adjust the polarity of the phase error current signal from the photodetector so that it can be used to drive the phase section of the slave laser. The total load seen by the feedback photodetector is designed to provide a second-order transfer function with lag compensation. The LR circuit is designed to have a zero at a frequency close to the pole in the FM frequency response of the slave laser, making it a more controllable device. The 3-dB point in the FM frequency response of the SG-DBR laser is ~70 MHZ. Since the laser itself acts as an integrator, the remaining RC circuit is required to provide only a single pole. This is achieved with the larger of the two resistors that dominates at low frequencies. The smaller resistor dominates at frequencies closer to the 3-dB point and provides a zero that is necessary to improve stability of the loop at the frequencies where the gain becomes unity. The resulting bandwidth of the loop is ~300 MHz, which, as we show below, is sufficient for locking an SG-DBR laser, in large part due to the fact that the phase noise of SG-DBR lasers is dominated by low-frequency jitter.

Figs. 5(a) and 5(b) show oscilloscope traces of the OPLL-PIC optical output before and after locking it with a 5 GHz microwave signal, which is also used to trigger the oscilloscope. Locking is achieved by gradually bringing the detuning frequency closer to the modulation frequency. As shown in Fig. 5(a), before locking, the phase noise is so large that only the envelope of the beat is observed. When the OPLL is locked, most of the power from the beat is in the locked state, as shown in Fig. 5(b). Occasional cycle slipping of the OPLL is evident in the jitter shown in Fig. 5(b). Fig. 6 shows the corresponding phase noise spectrum of a locked OPLL-PIC, measured using an external photodetector and an electrical spectrum analyzer. The phase noise reaches maxima at frequencies ~300 MHz below and above the 5 GHz offset frequency because the loop becomes unstable when operating at frequencies exceeding its bandwidth (~300 MHz).

There is a significant noise penalty associated with the sideband locking scheme because the power in the sidebands is a fraction of the power in the main lobes, producing an inefficient mixing in the photodetector. For the same reason, the modulation power needed for successful locking in our experiment is around 10 dBm. The noise penalty could be decreased by using an external RF mixer, which is a more complicated setup. In the future work, feedback electronics

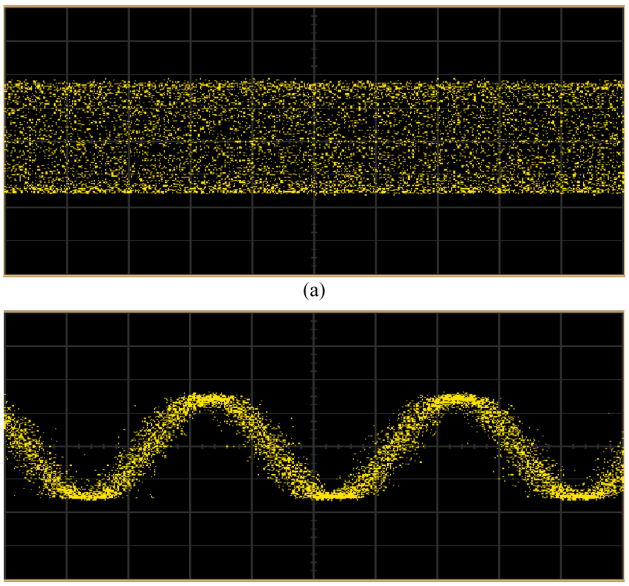

Figure 5. Oscilloscope traces of the OPLL-PIC optical output (a) before and (b) after heterodyne locking of the SG-DBR lasers at a 5GHz frequency offset. Both traces are 500 ps long.

will be integrated to further improve the loop bandwidth and decrease the phase noise. In addition, the on-chip feedback photodetectors will be used in a balanced configuration, which should decrease the phase noise penalty due to laser amplitude noise.

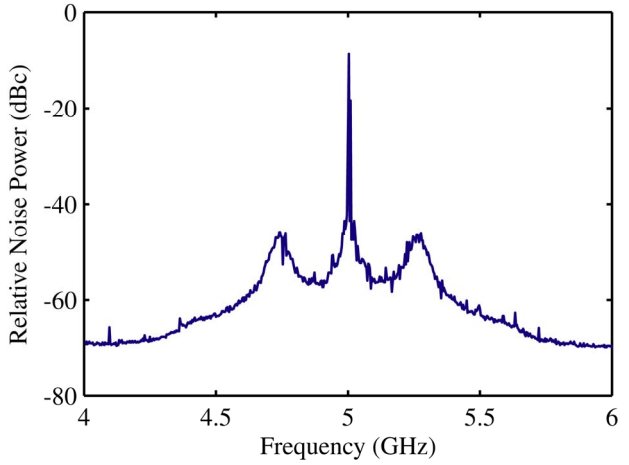


Figure 6. Phase noise spectrum of the OPLL-PIC output corresponding to heterodyne locking of the two SG-DBR lasers at a 5 GHZ frequency offset.

## IV. Conclusion

In this paper, we have demonstrated a proof-of-concept heterodyne locking of the first integrated OPLL. The OPLL-PIC contains two SG-DBR lasers monolithically integrated with SOAs, MMIs, and high-speed modulator and photodetectors. The monolithic integration enables small-latency (large-bandwidth) feedback loops, necessary to compensate for wide linewidths of SG-DBR lasers, and semiconductor lasers in general. SG-DBR lasers offer large tuning sensitivities, they are well-behaved when used as CCOs, as they do not suffer from the phase inversion problem, and they offer wide wavelength tuning ranges, *i.e.*, large coherent beat frequencies. The OPLL-PIC contains on-chip modulators that can be used for modulation of a coherent millimeter-wave beat. The technology is robust, has a small footprint, and provides for easy packaging. Future improvements of the OPLL will be achieved by using both feedback detectors as a balanced receiver pair in order to reduce laser amplitude noise, which increases the phase noise of the OPLL. In addition, more sophisticated, integrated feedback electronics will be used in order to further decrease the feedback loop latency, thereby decreasing the phase noise of the OPLL.

## Acknowledgment

A portion of this work was done in the UCSB nanofabrication facility, part of the NSF funded NNIN network.

## References

[1] R. C. Steele "Optical phase-locked loop using semiconductor laser diodes," *Electron. Lett.*, vol. 19, no. 2, pp. 69–71, Jan. 20, 1983.

[2] W. R. Leeb, H. K. Philipp, and A. L. Scholtz, "Homodyne receiver for ASK signals at 10-µm wavelength," *Appl. Opt.*, vol. 23, no. 4, pp. 523–524, Feb. 15, 1984.

[3] H. K. Philipp, A. L. Scholtz, E. Bonek, and W. R. Leeb, "Costas loop experiments for a 10.6 µm communications receiver," *IEEE Trans. Commun.*, vol. COM-31, no. 8, pp. 1000–1002, Aug. 1983.

[4] N. Satyan, W. Liang, A. Kewitsch, G. Rakuljic, and A. Yariv, "Coherent power combination of semiconductor lasers using optical phase-lock loops," IEEE *J. Sel. Top. Quant. Electron.*, vol. 15, no. 2, pp. 240–247, Mar./Apr. 2009.

[5] L. N. Langley, M. D. Elkin, C. Edge, M. J. Wale, U. Gliese, X. Huang, and A. J. Seeds, "Packaged semiconductor laser optical phase-locked loop (OPLL) for photonic generation, processing and transmission of microwave signals," *IEEE Trans. Microwave Theory Technol*., vol. 47, no. 7, pp. 1257–1264, July 1999.

[6] L. A. Johansson and A. J. Seeds, "Millimeter-wave modulated optical signal generation with high spectral purity and wide locking bandwidth using a fiber-integrated optical phase-lock loop", *IEEE Photon. Tech. Lett.*, vol. 12, no. 6, pp. 690–692, Jun. 2000.

[7] R. T. Ramos and A. J. Seeds, "Fast heterodyne optical phase-lock loop using double quantum well laser diodes," *Electron. Lett.*, vol. 28, no. 1, pp. 82–83, Jan. 1992.

[8] S. Ristic, A. Bhardwaj, M. J. Rodwell, L. A. Coldren, and L A. Johansson, "Integrated Optical Phase-Locked Loop," *Optical Fiber Communications Conf. (OFC). Postdeadline Tech. Dig. Opt. Soc. Amer.*, PDPB3, 2009.

[9] J. W. Raring *et. al.*, "Advanced integration schemes for high-functionality/high-performance photonic integrated circuits," presented at the Proc. SPIE, San Jose, CA, Jan. 23–25, 2006, Paper 61260H.

[10] L. A. Coldren, "Monolithic tunable diode lasers," *IEEE J. Select. Topics Quantum Electron.*, vol. 6, no. 6, pp. 988–999, Nov./Dec. 2000.

[11] S. Nakagawa *et. al.*, "Phase noise of widely-tunable SG-DBR laser," in *Optical Fiber Communications Conf. (OFC). (Trends in Optics and Photonics Series Vol. 86)Tech. Dig. (IEEE Cat. 03CH37403). Opt. Soc. Amer.*, vol. 2, Wash., DC, 2003, pp. 461–462.