Sub-100-nm Process Technologies For THz InP HBTs & MOSFETs

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Abstract—To obtain THz bandwidths in either bipolar or field-effect transistors, lithographic junction dimensions and epitaxial layer thicknesses must be reduced, device contact resistivities reduced, gate capacitance densities increased, and operating current densities increased. Fabrication process flows must be extensively required to fabricate devices having 10-50 nm junction dimensions and 1-3 THz cutoff frequencies.

I. INTRODUCTION

III-V transistors of ~10 to 100 nm lithographic dimensions are being developed both for THz applications and for use in large-scale digital integrated circuits. Reducing dimensions increases both IC packing density and transistor bandwidth. Increasing bandwidth of an arbitrary circuit by γ:1 requires a γ:1 reduction of transistor capacitances and transit delays while maintaining constant resistances and bias and signal voltages and currents.

For bipolar transistors [1], this requires a $\sim \gamma^1$:1 reduction in epitaxial dimensions, a γ^2:1 reduction in contact resistivities, and a γ^2:1 reduction in lithographic dimensions. For field-effect transistors [2], such scaling requires again a γ:1 reduction in epitaxial dimensions (dielectric equivalent thickness, wavefunction depth) and a γ^2:1 reduction in contact resistivities, but only requires a γ^1:1 reduction in lithographic dimensions (gate length). Required current densities scale with both transistor types; for HBTs, emitter current density ($mA/\mu m^2$) varies as γ^2, though current per unit emitter stripe length remains fixed, while for FETs, current per until gate width ($mA/\mu m$) varies as γ^1, but current per unit source and drain Ohmic contact area ($mA/\mu m^2$) varies as γ^2.

To build multi-THz HBTs and HEMTs, and to build sub-22-nm InGaAs MOSFETs, we must fabricate *self-aligned* contacts and junctions of 10-100 nm dimensions. We must develop Ohmic contacts of $\sim 1\,\Omega - \mu m^2$ contact resistivity; this resistivity must not increase when operating ~25-250 $mA/\mu m^2$ current density, nor can the contact metals diffuse under such high current and thermal stress through device junctions only ~5-10 nm below the surface. We here describe our efforts to develop such fabrication processes for both InP-based FETs and HBTs.

II. THz AND nm FET SCALING

First consider in more detail FET scaling in the constant-voltage, constant-velocity limit. Vertical dimensions (T_{well} ,

T_{eq}) must be reduced in proportion to gate length to maintain a constant g_m / G_{ds} ratio and to maintain a constant ratio of the parallel-plate (C_{g-ch}) to the fringing ($C_{gs,f}$, C_{gd}) components of the device input capacitance; in the absence of vertical scaling, drain-induced barrier lowering increases, output conductance degrades, and the input capacitance becomes dominated by gate fringing fields.

Table 1: HBT scaling laws: changes required for γ:1 increased bandwidth in an arbitrary circuit

parameter	law
emitter junction length, L_e (nm)	γ^0
emitter junction width, W_e (nm)	γ^{-2}
collector junction width (nm)	γ^{-2}
collector depletion thickness (nm)	γ^{-1}
base thickness (nm)	$\sim \gamma^{-1/2}$
contact resistivities ρ_c ($\Omega - \mu m^2$)	γ^{-2}
emitter current density ($mA/\mu m^2$)	γ^2
emitter current density ($mA/\mu m$)	γ^0
temperature rise (one device, K)	$\sim \ln(L_e / W_e)$
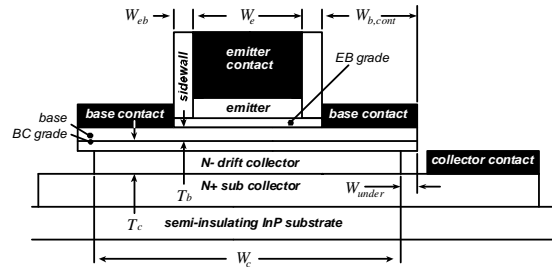
As a consequence of vertical scaling, on-state current density I_d / W_g increases as γ^1. It is well understood that difficulties in reducing T_{eq} (gate leakage by tunneling) and in increasing C_{DOS} [3] will impede constant-voltage FET scaling; note also that T_{inv} must scale as γ^{-1}, requiring thinner wells or stronger vertical fields, $(R_s + R_d)/W_g$ must scale as γ^{-1}, requiring both lower ρ_c and increased carrier concentrations in access regions, and on-state inversion charge density n_s must scale as γ^1, requiring increased gate barrier height. Further, device self-heating scales as γ^1, a serious concern for normally-on circuits such as sub-mm-wave amplifiers.

These scaling considerations apply to equally to InGaAs FETs in development for VLSI and for sub-mm-wave/THz applications; device design goals include low access resistance, high drive current density, thin wells, high sheet carrier density, and gate barriers that are both thin and high in energy. Future sub-mm-wave FETs may well use high-K gate dielectrics to permit small T_{eq} and large n_s; note that moderately high interface charge density D_{it} will not impair device gain at frequencies well above the inverse of the interface trap lifetimes.

Table 2: Constant-voltage / constant-velocity FET scaling laws: changes required for $\gamma:1$ increased bandwidth in an arbitrary circuit

| parameter	law
gate length L_g, source-drain contact lengths $L_{S/D}$ (nm)	γ^{-1}
gate width W_g (nm)	γ^{-1}
equivalent oxide thickness $T_{eq} = T_{ox}\varepsilon_{SiO_2}/\varepsilon_{oxide}$ (nm)	γ^{-1}
dielectric capacitance $C_{ox} = \varepsilon_{SiO_2}L_gW_g/T_{eq}$ (fF)	γ^{-1}
inversion thickness $T_{inv} \sim T_{well}/2$ (nm)	γ^{-1}
semiconductor capacitance $C_{semi} = \varepsilon_{semi}L_gW_g/T_{inv}$ (fF)	γ^{-1}
DOS capacitance $C_{DOS} = q^2nm^*L_gW_g/2\pi\hbar^2$ (fF)	γ^{-1}
electron density n_s (cm^{-2})	γ^1
gate-channel capacitance $C_{g-ch} = [1/C_{ox}+1/C_{semi}+1/C_{DOS}]^{-1}$ (fF)	γ^{-1}
transconductance $g_m \sim C_{g-ch}v_{injection}/L_g$ (mS)	γ^0
gate-source, gate-drain fringing capacitances $C_{gs,f} \propto \varepsilon W_g$, $C_{gd} \propto \varepsilon W_g$ (fF)	γ^{-1}
S/D access resistances R_s, R_d (Ω)	γ^0
S/D contact resistivity R_s/W_g, R_d/W_g ($\Omega-\mu$m)	γ^{-1}
S/D contact resistivity ρ_c ($\Omega-\mu$m^2)	γ^{-2}
drain current $I_d \sim g_m(V_{gs}-V_{th})$ (mA)	γ^0
drain current density (mA/μm)	γ^1
temperature rise (one device, K)	$\sim W_g^{-1}$
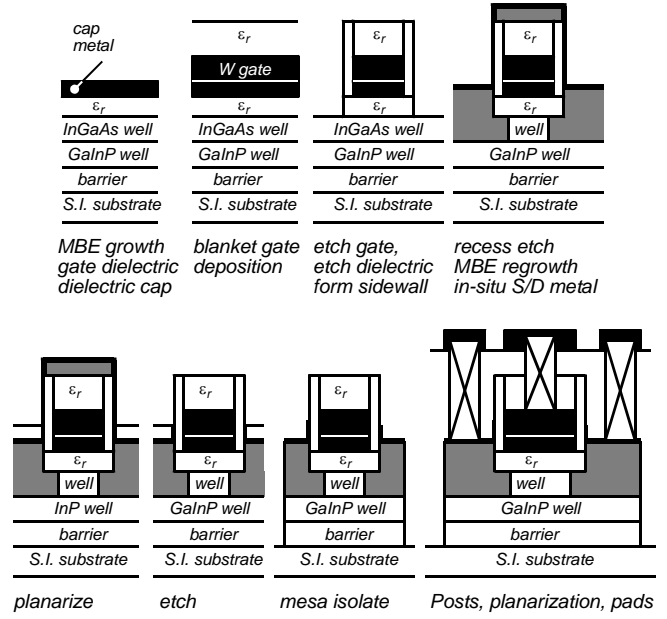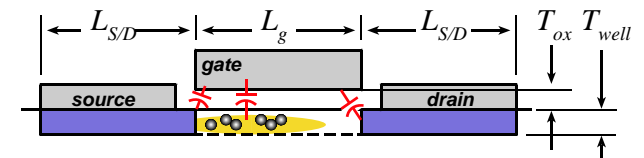
Figure 1: Process flow for III-V FETs with source/drain regrowth by MEE.

III. FABRICATION PROCESSES FOR nm III-V MOSFETs

Established III-V HEMT structures do not well address these scaling requirements. We have therefore developed a fully self-aligned InGaAs MOSFET process flow [4,5,6,7] (fig. 1). In this flow, 4.7 nm Al_2O_3 gate dielectric is deposited by ALD on a 5 nm $In_{0.53}Ga_{0.47}As$ channel, the gate is formed by blanket W/Cr/SiO_2 deposition and RIE etching, and thin ~25 nm Si_xN_y gate sidewalls formed. After etching the Al_2O_3, self-aligned S/D InAs N+ regions (50 nm thick, 8×10^{19} cm^{-3}, 23 Ω sheet resistance) are formed by migration enhanced epitaxy, and self-aligned S/D contacts formed by in-situ blanket evaporation of Mo ($3.5\,\Omega-\mu$m^2 contact resistance) and a subsequent height-selective etch [8]. Mesa isolation and back-end metal completes the process. Unlike HEMTs, no gate barrier is present in the S/D regions, the source and drain are fully self-aligned to the gate, and carrier densities in the S/D access regions are high (~1.5×10^{13}cm^{-2}). Figure 3 shows measured I_D for a 200-nm-L_g device.
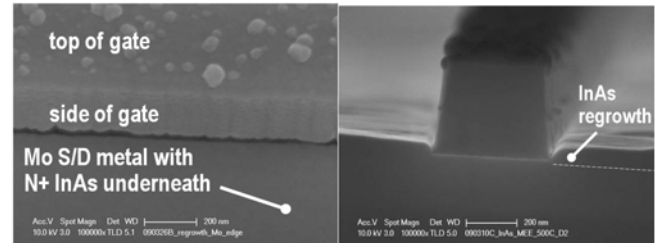

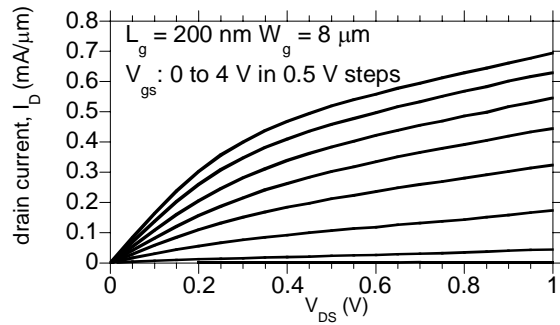Figure 2: Regrown S/D InGaAs FET, oblique view & cross-section
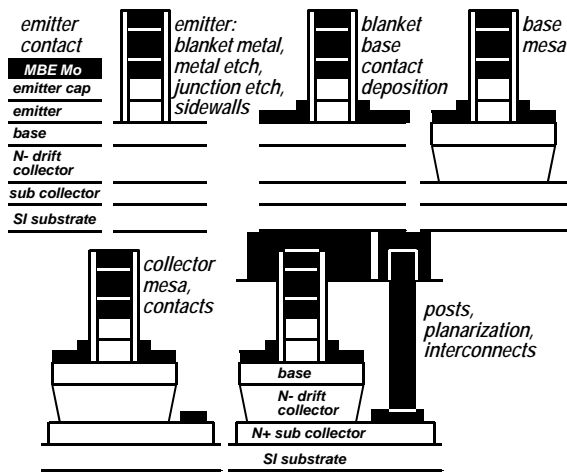
Figure 3: Common-source characteristics

Figure 4: Refractory-contact /dry-etched process flow for 128 nm /64 nm InP HBTs

IV. THZ BIPOLAR TRANSISTOR SCALING

We now review bipolar transistor scaling. Unlike FETs, the diffusion capacitances and the parallel-plate component of junction depletion capacitances dominate over edge (fringing) capacitances, hence HBTs need not be scaled to progressively increase the device operating current and transconductance per unit junction length. Unlike MOSFETs (but like THz HEMTs), the HBT is biased normally-on, and the device operating power density and the consequent junction temperature rise is a dominant consideration controlling the geometric scaling laws [9]. As noted above, each γ:1 increase in bandwidth requires a $\sim \gamma^1$:1 reduction in epitaxial dimensions, a γ^2:1 reduction in contact resistivities, and a γ^2:1 reduction in lithographic dimensions. These scaling laws arise simply because the collector thickness must be reduced γ^1:1 to reduce collector transit time, and the collector area reduced γ^2:1 to obtained the desired γ^1:1 reduction in collector capacitance. With all junction areas reduced γ^2:1, contract resistivities must be reduced in the same proportion to maintain constant access resistance, and current densities increased in the same proportion to maintain constant operating current. Because junction temperature rise varies as

$\Delta T \propto (P / K_{thermal}) \cdot \ln(L_e / W_e)$, the required γ^2:1 reduction in junction area *cannot* be obtained by reducing the device junction length; instead, the emitter (and collector) junction widths are both reduce γ^2:1. The scaling laws of table 1 are thereby obtained.

V. FABRICATION PROCESSES FOR NM III-V HBTS

For HBTs, a 1.0 THz f_τ and 2.0 THz f_{max} should be obtained with ~64 nm contact width and ~2 $\Omega - \mu m^2$ resistivity for both the emitter and base contacts. The emitter current density must be ~ 30-40 mA/μm^2, and the base must be ~20 nm thick.

There are serious challenges in building such a device. It is difficult to form tall yet narrow emitter contacts by liftoff, and target emitter current densities are close to the electromigration limits of a gold emitter electrode. We are therefore forming the emitter contact by blanket sputter deposition and subsequent dry-etching of a refractory (W or Mo) metal. To control the emitter etc undercut during emitter junction definition, the emitter semiconductor must either be very thin, or the emitter must be dry-etched. Base-emitter contact separation by liftoff is not straightforward at these junction dimensions. Figure 4 shows a simplified version of our present 128nm/64 nm process flow. n-situ Mo emitter contacts [10] provide 1.1 ± 0.4 $\Omega - \mu m^2$ contact resistivity. The emitter metal is dry-etched Mo or W to withstand high target current densities. Emitter and base contacts are separated by thin $Si_x N_y$ sidewalls, and base contacts are sputter-deposited refractory metals.

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