$In_{0.53}Ga_{0.47}As$ Channel MOSFETs With Self-Aligned InAs Source/Drain Formed by MEE Regrowth

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***Abstract*—We report $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSFETs having both self-aligned *in situ* Mo source/drain ohmic contacts and self-aligned InAs source/drain n^+ regions formed by MBE regrowth. The device epitaxial dimensions are small, as is required for 22-nm gate length MOSFETs; a 5-nm $In_{0.53}Ga_{0.47}As$ channel with an $In_{0.48}Al_{0.52}As$ back confinement layer and the n^{++} source/drain junctions do not extend below the 5-nm channel. A device with 200-nm gate length showed $I_D = 0.95$ mA/μm current density at $V_{GS} = 4.0$ V and $g_m = 0.45$ mS/μm peak transconductance at $V_{DS} = 2.0$ V.**

***Index Terms*—InAs source/drain, InGaAs MOSFET, migration-enhanced epitaxial regrowth, source/drain regrowth, III–V MOSFET.**

I. Introduction

BECAUSE of the high electron velocities observed experimentally in InGaAs-based HEMTs [1], MOSFETs with $In_xGa_{1-x}As$ $(x \geq 0.53)$ channels are being developed [2]–[6] for potential application in VLSI logic circuits at technology nodes below 22-nm gate length (L_g). There are several challenges faced in rendering these devices suitable for very large scale integrated circuits. For integration into ICs on silicon substrates, methods have to be developed to grow $In_xGa_{1-x}As$ with low defect density on Si. The semiconductor–dielectric interface state density $D_{\rm it}$ should be small ($\leq 1 \times 10^{12}$ cm^{-2}/eV), and various gate dielectrics and deposition techniques are therefore being investigated [2]–[7].

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Device structures and fabrication process flows appropriate for sub-22-nm L_g must also be developed. Vertical device dimensions should be small; in a MOSFET having n^+ source and drain regions close to the gate, for low subthreshold swing and low drain-induced barrier lowering, the gate dielectric equivalent oxide thickness (EOT) should be at most ~1 nm, and the mean depth of the electron wave function below the surface has to be at most ~3 nm [8]. Process flows have to be developed to produce n^+ source/drain regions and source/drain contacts at lithographic dimensions comparable to the gate length. Vertical source/drain n^+ region doping profiles need to be abrupt (~5 nm). Self-alignment of the source/drain contacts to the gate electrode is desirable both for decreased transistor mask layout area and for reduced source and drain access resistance, yet there is no equivalent of a self-aligned silicide process in III–V semiconductors to facilitate such self-alignment. The source and drain access resistance should be low; for a device designed for 2.5 mA of drain current I_D per micrometer of gate width W_g at 500-mV gate overdrive $(V_{\rm gs} - V_{\rm th})$, even 20 $\Omega \cdot \mu$m of normalized source resistance R_sW_g would reduce the ON-state I_D by ~10%. Because the source/drain contact lengths must be comparable with that of the gate, i.e., ~22 nm for a 22-nm L_g MOSFET, contact resistivities must be below ca. 1 $\Omega \cdot \mu$m^2.

Here, we report enhancement mode $In_{0.53}Ga_{0.47}As$ MOSFETs with self-aligned n^+ InAs source and drain formed by a low arsenic (As) flux migration-enhanced epitaxial regrowth. In these devices, metal contacts to the source and drain n^+ regions are also self-aligned to the gate. These are formed by depositing Mo contact metal *in situ* immediately after regrowth, followed by patterning by height-selective etching [9]. In contrast to earlier results [10] reported using $In_{0.53}Ga_{0.47}As$ regrown source/drain regions, the InAs n^+ regions employed here are less prone to electron depletion from defects or surface states in comparison to $In_{0.53}Ga_{0.47}As$ because the intrinsic Fermi level pinning is above the conduction band edge [11]. The devices show a transconductance (g_m) peak of 0.45 mS/μm for $L_g = 200$ nm.

II. Device Structure and Fabrication

The devices were fabricated following the process flow in [9]. A 1×10^{17} cm^{-3} Be-doped (P-type) $In_{0.48}Al_{0.52}As$ buffer layer, an $In_{0.48}Al_{0.52}As$ bottom confinement layer and a 5-nm-thick $In_{0.53}Ga_{0.47}As$ channel were grown by MBE upon a p^+ InP substrate. The upper 3.3 nm of $In_{0.48}Al_{0.52}As$ confinement layer was $[Si] = 2.0 \times 10^{19}$ $(n = 1.8 \times 10^{19}$ cm$^{-3})$ doped; this

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will modulation dope the $In_{0.53}Ga_{0.47}As$ channel in regions both beneath the gate dielectric sidewalls and under the gate. The modulation doping was provided to ensure sufficient electrons in the portions of the channel under the sidewall, given the possible carrier depletion from traps at the high-k/channel interface. The wafer was then cooled to 50 °C, and an 80 nm of arsenic was deposited in order to prevent oxidation during transfer to dielectric deposition system. Next, the wafer was loaded into an atomic layer deposition tool, the arsenic cap layer desorbed at 480 °C, and 4.7-nm (∼2.5-nm EOT)-thick Al_2O_3 was deposited.

W (50 nm)/Cr (50 nm)/SiO_2 (350 nm) gates were then defined by optical lithography at gate lengths varying from 200 nm to 10 μm and were patterned using a selective dry etch process [9]. The 20–25-nm-thick SiN_x sidewalls were then defined by blanket PECVD deposition and low-power anisotropic RIE etch. The Al_2O_3 high-k dielectric was then wet etched in dilute KOH, stopping selectively on the 5-nm $In_{0.53}Ga_{0.47}As$ channel. The wafer was then cleaned by exposure to UV ozone, followed by a 1-min dilute HCl treatment and a DI rinse. Following the cleaning, the wafer was immediately loaded into the MBE chamber and cleaned with atomic H at 400 °C for 30 min. The wafer was then heated to 560 °C under arsenic overpressure to thermally desorb any native oxide on the channel. A c(4 × 2) reconstruction was seen in reflection high electron energy diffraction before regrowth, indicating an epiready surface. A 50 nm of $[\mathrm{Si}] = 8 \times 10^{19}$ cm^{-3} $(n = 4 \times 10^{19}$ $\mathrm{cm}^{-3})$-doped InAs was grown at 500 °C by migration-enhanced epitaxy [12]. After the growth, the wafer was transferred under ultrahigh vacuum to an electron beam evaporator connected to the MBE, and a 20 nm of molybdenum (Mo) was deposited. As deposited, the Mo film covered the entire wafer surface, bridging over the dielectric-encapsulated gate, and therefore short circuited the source and drain electrodes. This source/drain contact metal covering the gate electrode was therefore removed with height-selective etch [9]. Source/drain pads were then deposited, and devices are mesa isolated. To contact the gates, the silicon dioxide covering the gate pads was removed by etching in buffered HF.

III. Results and Discussion

Fig. 1(b) shows a cross-sectional Scanning Electron Microscopy (SEM) of a gate after InAs regrowth on a coprocessed wafer having no gate dielectric. Fig. 1(c) shows an angled view SEM of the MOSFET after regrowth and *in situ* Mo deposition. No gaps are seen between the n^+ InAs regrowth and the gate edge, and there is no InAs growth on the gate sidewall. Unlike the $In_{0.53}Ga_{0.47}As$ regrowth on our previously reported FETs [10], there is no significant reduction in the thickness of InAs near the gate edge. The common-source output characteristics of a 200-nm L_g MOSFET are shown in Fig. 2(a), while Fig. 2(b) shows the variation I_D of with V_{GS}. The device shows 0.95-mA/μm I_D at $V_{\mathrm{GS}} = 4.0$ V and shows 0.45-mS/μm peak g_m at $V_{\mathrm{DS}} = 2.0$ V. The zero-bias drain–source resistance is 710 $\Omega \cdot \mu$m. The measured threshold voltage differs considerably from the −0.75 V calculated from the layer structure and the tungsten vacuum work function [13]; this may indicate

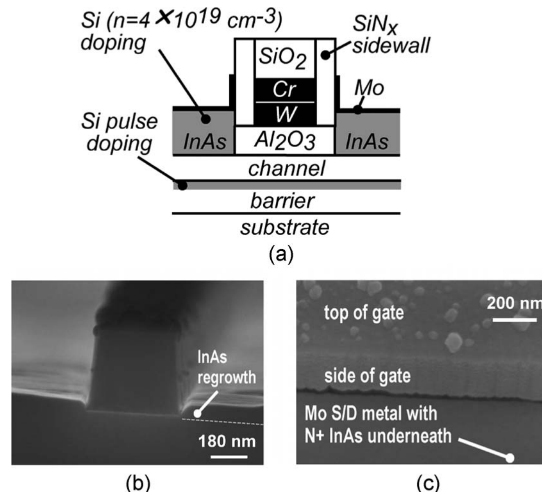

Fig. 1 (a) Device cross-sectional schematic (not to scale). (b) Cross-sectional SEM of the gate after InAs regrowth on a coprocessed wafer with no high-k dielectric. (c) Oblique view SEM of MOSFET after InAs regrowth and Mo deposition. No gaps are observed between the semiconductor regrowth and the gate edge, and no InAs growth is observed on the sidewall.

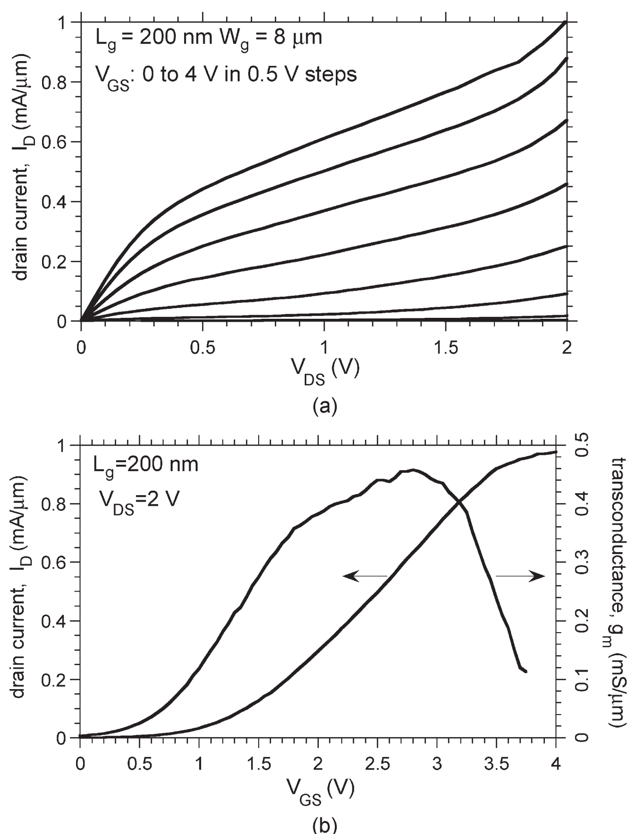

Fig. 2 (a) Common-source characteristics and (b) variation of drain current with a gate–source voltage of a 200-nm gate length MOSFET. The g_m plot is obtained by differentiating the smoothened I_d–V_{gs} plot to minimize noise in the plot. Note that, at $V_{\mathrm{DS}} = 2.0$ V, there is a 20% enhancement of I_d and g_m arising from impact ionization.

a fixed charge at the dielectric–semiconductor interface. The peak drive current and transconductance are more than an order of magnitude larger than the enhancement mode source/drain regrown MOSFETs reported in [10]. Transmission line measurements indicate a 3.5-$\Omega \cdot \mu\mathrm{m}^2$ Mo/InAs contact resistance, an 8.5-$\Omega \cdot \mu$m lateral ohmic contact access resistance, and a

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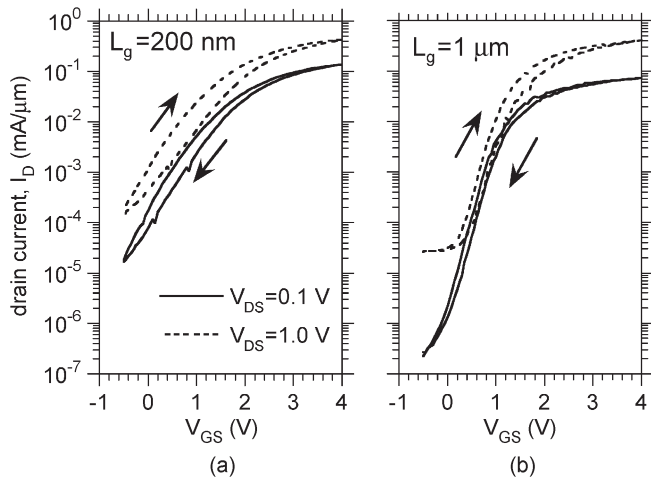

Fig. 3 Subthreshold I_D–$V_{\rm gs}$ plot of (a) the 200-nm gate length device and (b) a 1-μm gate length device.

23-Ω sheet resistance for the lattice-mismatched (relaxed) InAs layer. This sheet resistance is comparable to that of the lattice-matched n^+ $In_{0.53}Ga_{0.47}As$ regrowths reported earlier [10]. The n^{++} InAs/n^{++} InGaAs interface resistance is observed to be less than $2.0\ \Omega\cdot\mu m^2$ [14]. The $\log(I_D)-V_{\rm GS}$ characteristics on 200-nm L_g MOSFETs (Fig. 3) show 500 mV/dec subthreshold swing and 250-mV hysteresis; devices with $L_g = 1\ \mu$m show a subthreshold swing of 280 mV/dec. The hysteresis observed in the subthreshold operation may be due to charge traps in the gate oxide or at the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface.

Several limitations are evident in these dc characteristics. The variation in subthreshold swing with L_g is at least partly a consequence of poor control of short-channel effects. The electron density N_s in the $In_{0.53}Ga_{0.47}As$ channel below the N+ source/drain regrowths is $\sim 1.0 \times 10^{13}$ to 2×10^{13} cm^{-2}; hence, the Fermi level $E_{\rm fn}$ calculated including nonparabolicity is ~440 meV to 610 mV above the $In_{0.53}Ga_{0.47}As$ conduction band edge E_c. This is very close to the 500-meV $In_{0.53}Ga_{0.47}As$–$In_{0.48}Al_{0.52}As$ conduction band offset, leading to poor vertical electron confinement and, hence, poor short-channel effects; increased p^+ back barrier doping or increased bottom barrier energy (an AlAsSb bottom barrier) would improve the confinement. Note that, in $In_xGa_{1-x}As$ HEMTs [1], the N_s in the source/drain regions is $\sim 5 \times 10^{12}$ cm^{-2} in a 10-nm-thick channel, and $(E_{\rm fn} - E_c)$ is ~350 meV; hence, an $In_{0.48}Al_{0.52}As$ bottom barrier is sufficient for confinement. Furthermore, although comparable to other reported $In_xGa_{1-x}As$-channel MOSFETs [2]–[6], the dc transconductance and drive current here observed also remain well below the $In_xGa_{1-x}As$ HEMTs of comparable gate-channel vertical separation and comparable L_g. The possible causes of this discrepancy include the screening of the channel charge from the gate-imposed field by dielectric–semiconductor interface traps and the depletion of channel charge in regions under the silicon nitride gate dielectric sidewall. The channel region under the sidewalls is not modulated by the gate voltage; the electron supply to this region is from the electrostatic spillover from the n^{++} source/drain regions. The sidewalls must therefore be thin in order to reduce the resulting added contribution to the source access resistance. Building on this successful demonstration of a self-aligned device process flow, future performance enhancements will require new substrate designs for improved vertical confinement, characterization of devices with short (~35 nm) gate lengths, and detailed characterization of access resistivity in the source/drain regions.

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