A 1.1V 150GHz Amplifier with 8dB Gain and +6dBm Saturated Output Power in Standard Digital 65nm CMOS Using Dummy-Prefilled Microstrip Lines

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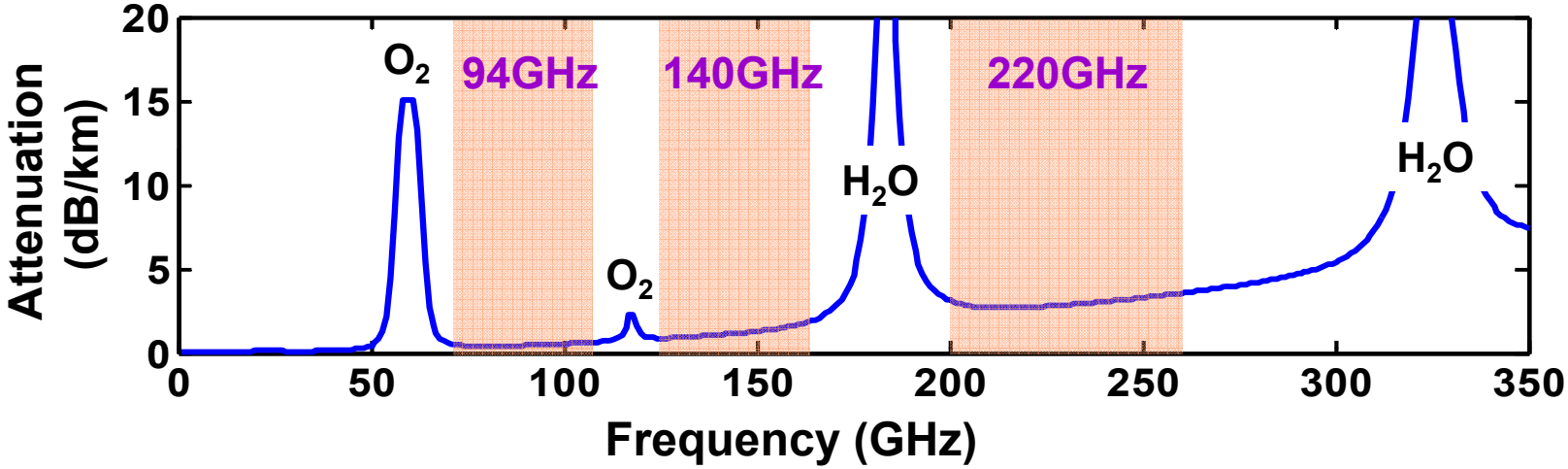
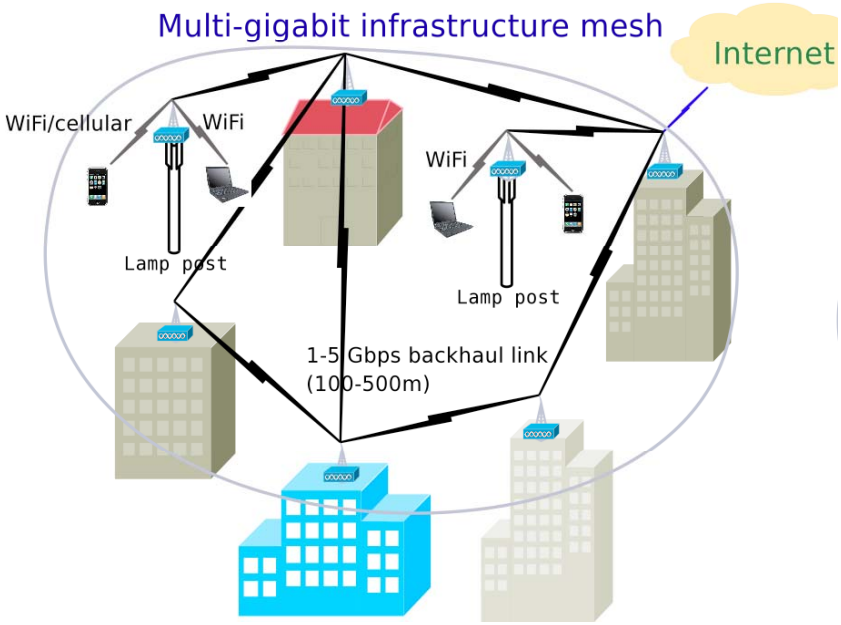
Outline

- **Introduction**
- **“Dummy-Prefilled” Microstrip Line**
  - Structure and Modeling
- **Design and Simulation**
- **Measurement Results**

Beyond 100GHz: What Applications?

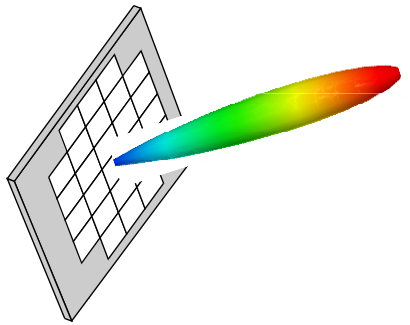




- **Communication**
  - Outdoor, indoor
- **Imaging (Passive, active)**
  - Security
  - All-weather radar
  - Medical

Beyond 100GHz: Why CMOS?

- **Low-cost**
- **Low-power**
- **Large-scale Integration → Parallelism**
  - Large monolithic phased array, imager.

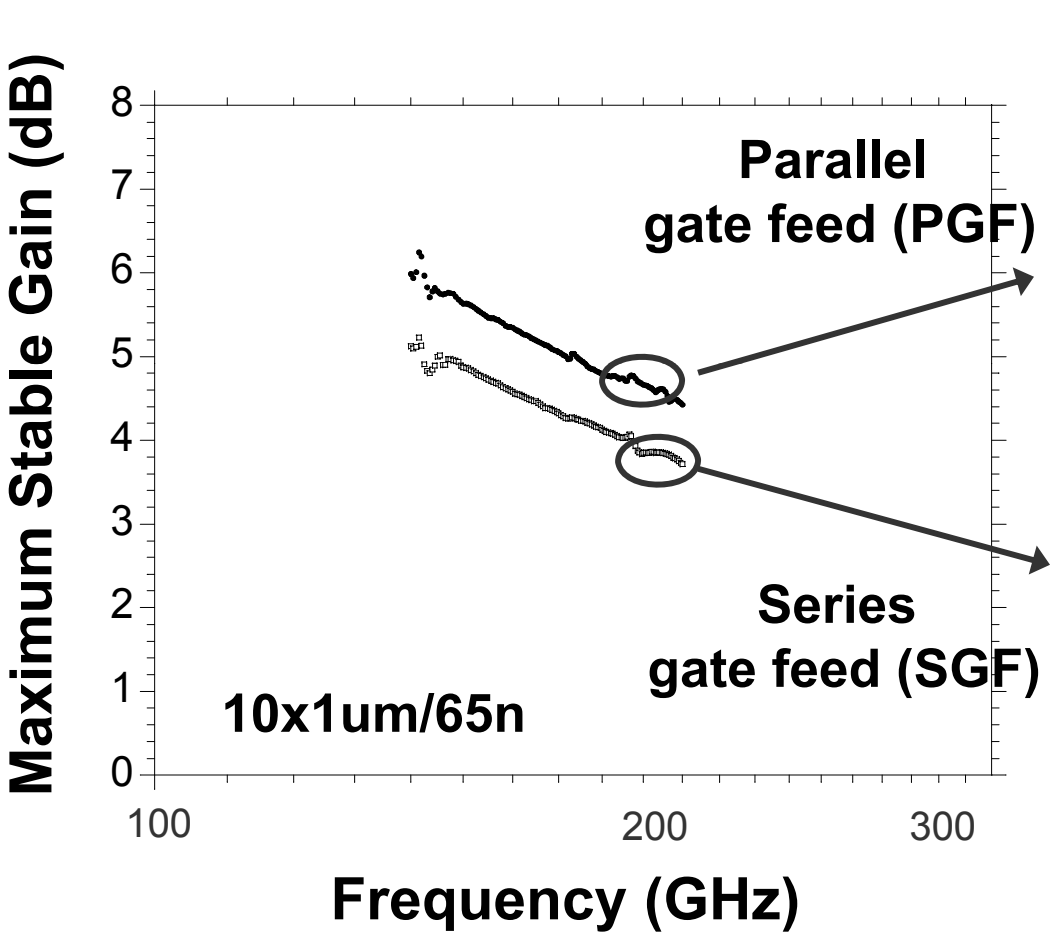


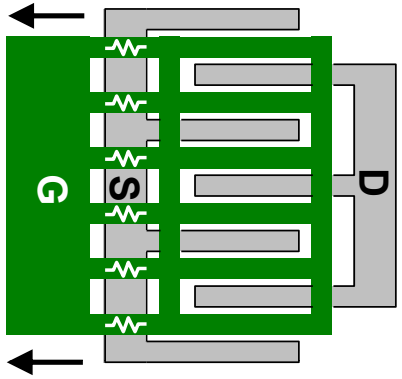
- **RF/mm-wave, IF/analog, DSP on a same die.**
  - System-on-chip
  - Digital calibration of RF/analog circuit imperfections, process variations.
  - Reconfigurability and adaptability

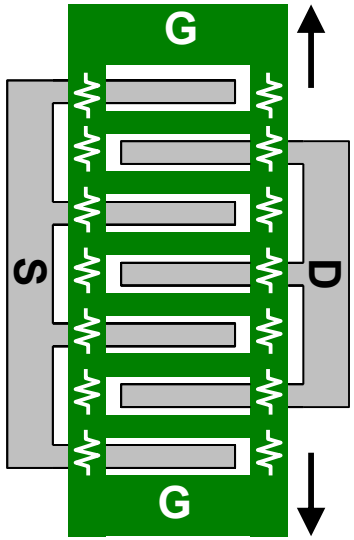
What Challenges in 150GHz CMOS Amp?

- **Low available FET gain, Low Supply Voltage**
  - Careful FET layout & sizing
  - Multi-stage Common-Source
- **Modeling uncertainties**
  - Simple matching topology with microstrip (MS) lines
- **Automatic "dummies" alter MS-line characteristics**
  - Propose "**Dummy-prefilled**" MS-line
- **Characterization**
  - Full 2-port on-wafer TRL calibration

FET Layout

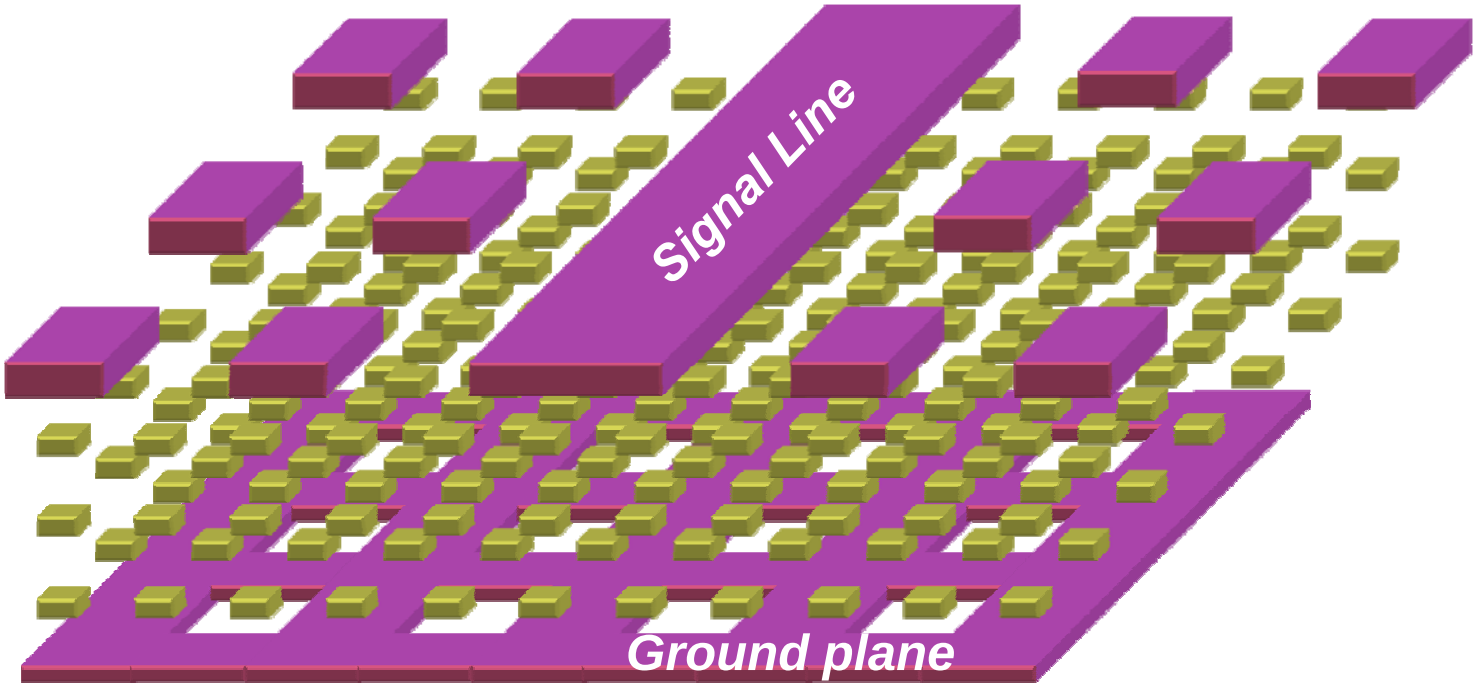






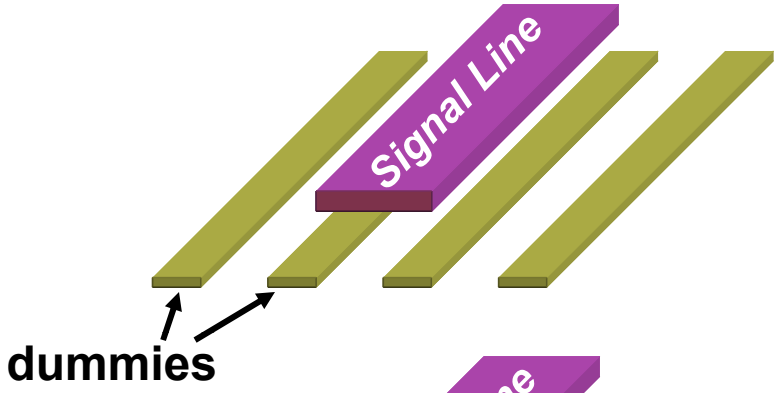
- Finger design: Reduce $R_{g,ext}$ and C_{gd} (W_F=1um)
- Wiring multiple fingers: Parallel versus Series

“Microstrip Line” in Nanoscale CMOS

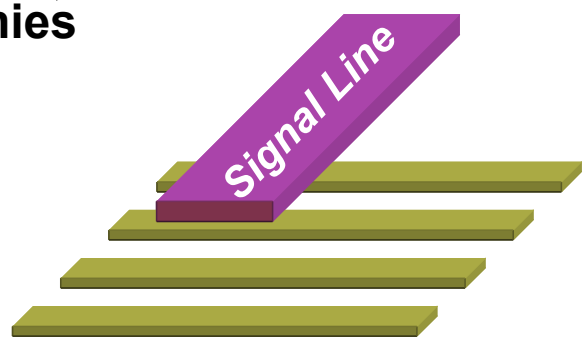


- **“Automatic” dummies/holes to meet metal density rules.**
- **Line capacitance increases**
  - ΔC depends on E-field orientation → Anisotropic
- **Direct E/M simulation nearly impossible**

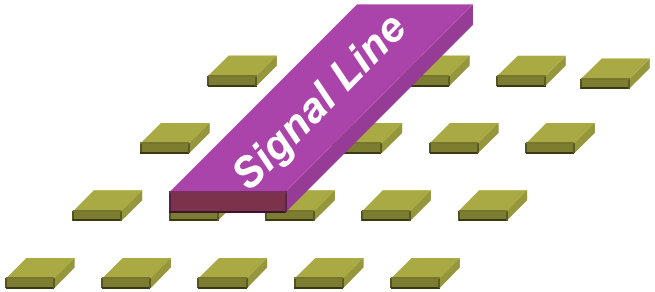
Possible Shapes of Dummy Pre-fillers



- "LINE" dummies
- Parallel to current flow

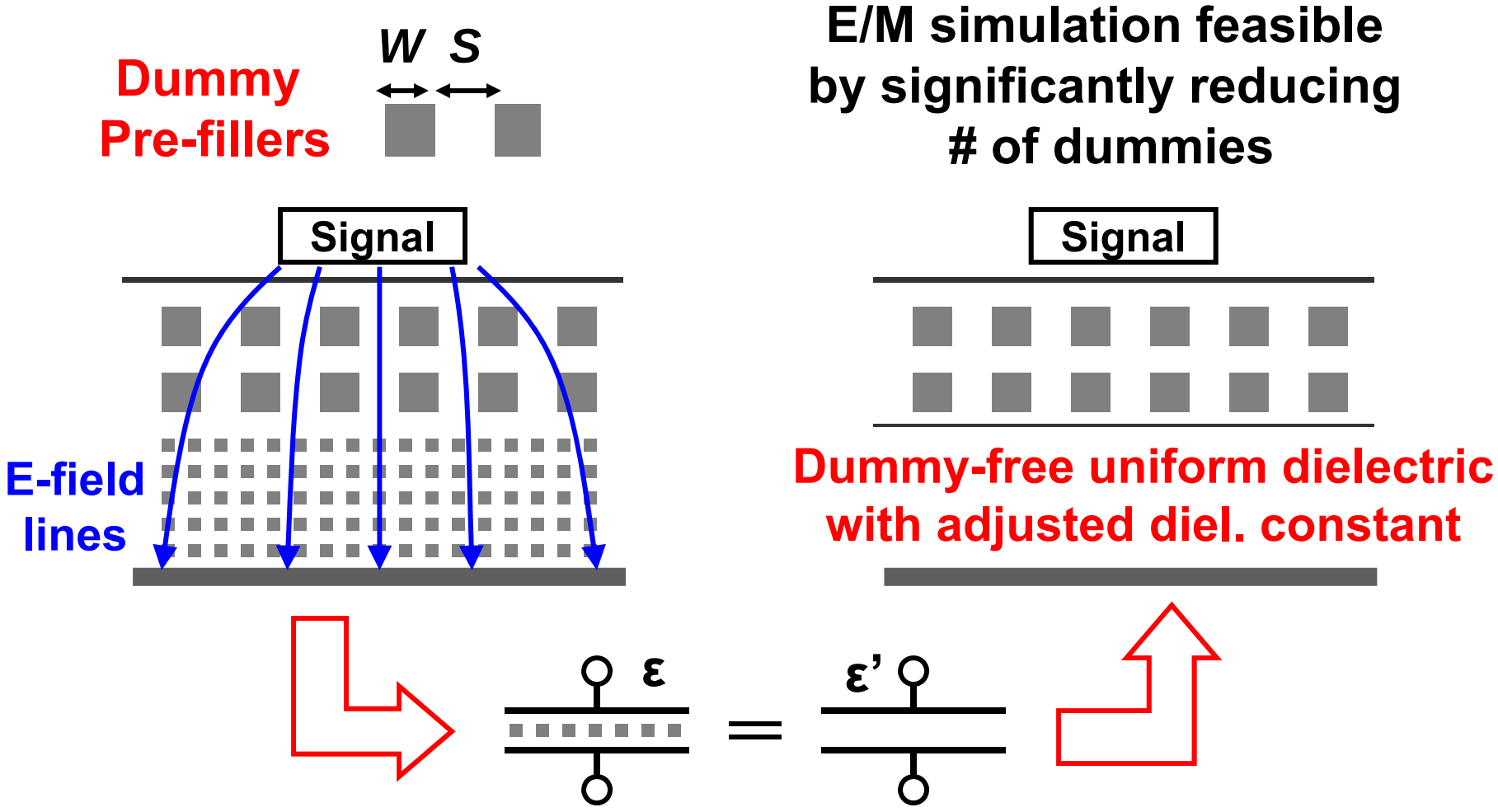


- "LINE" dummies
- Perpendicular to current flow



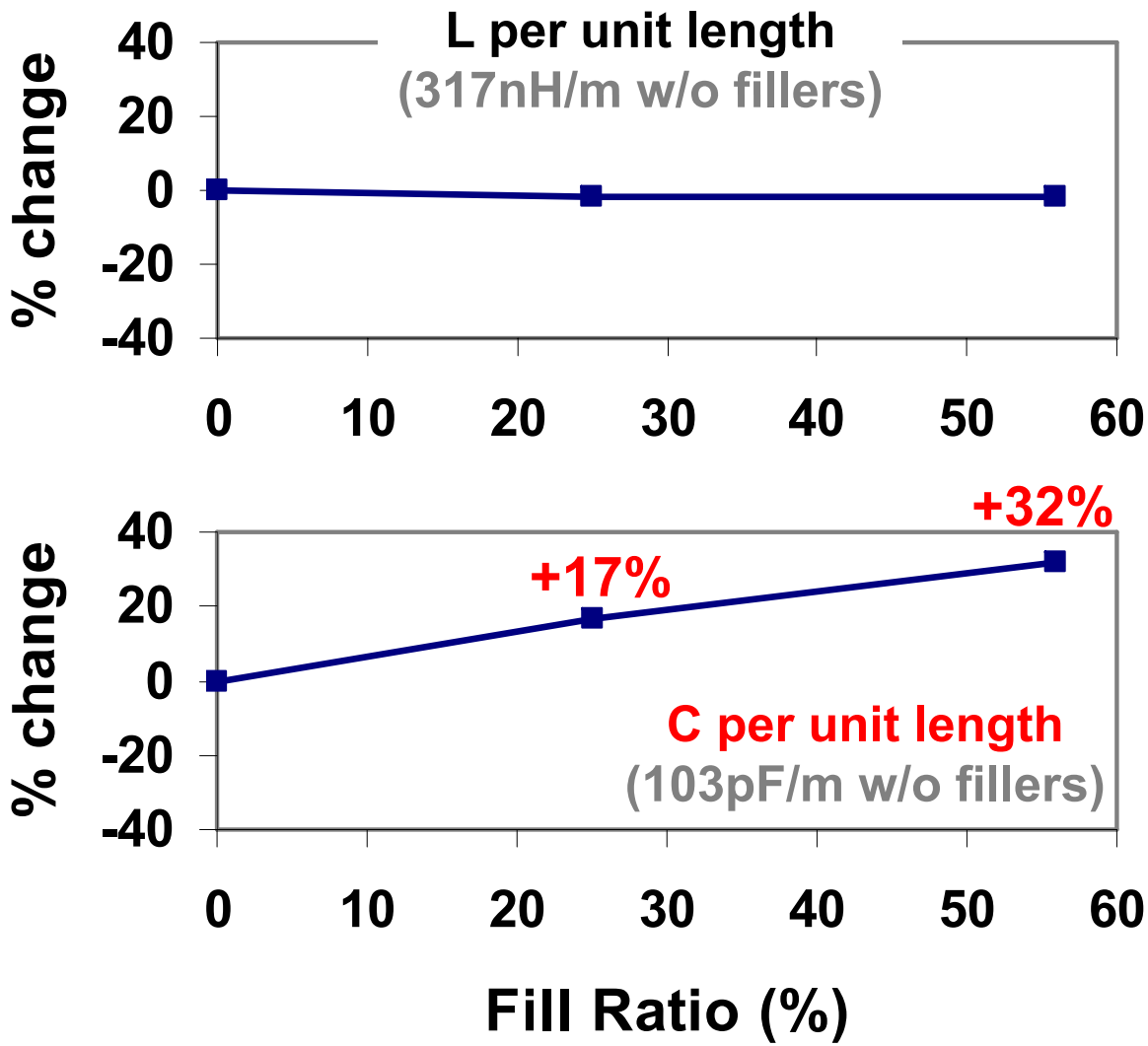
- "SQUARE" dummies
- No preferred direction of current flow

Reducing Complexity in E/M Sim

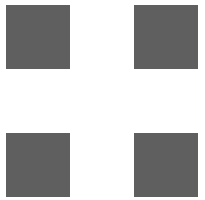


Successive dummy-layer substitution
by parallel-plate capacitor simulation

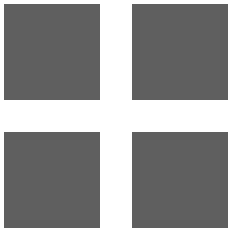
Line Inductance/Capacitance vs Fill Ratio



25% Fill
W:S = 1:1

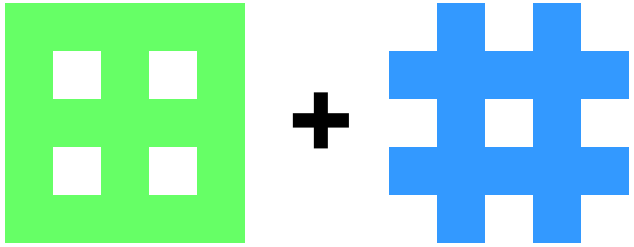


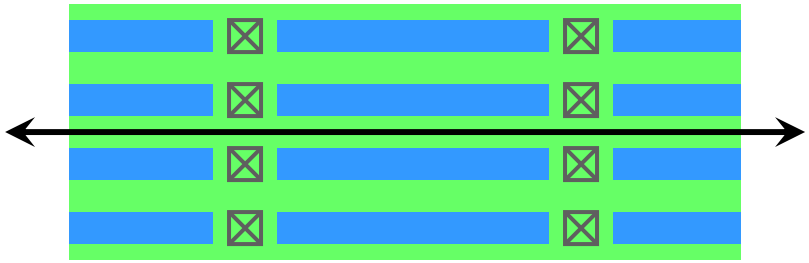
56% Fill
W:S = 3:1



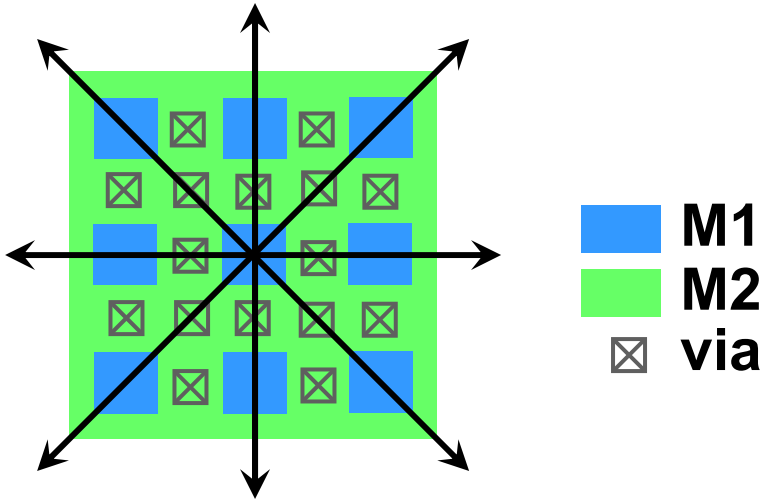
Ground Plane Construction

- Solid GND plane not allowed
- Put holes, and strap M1 & M2



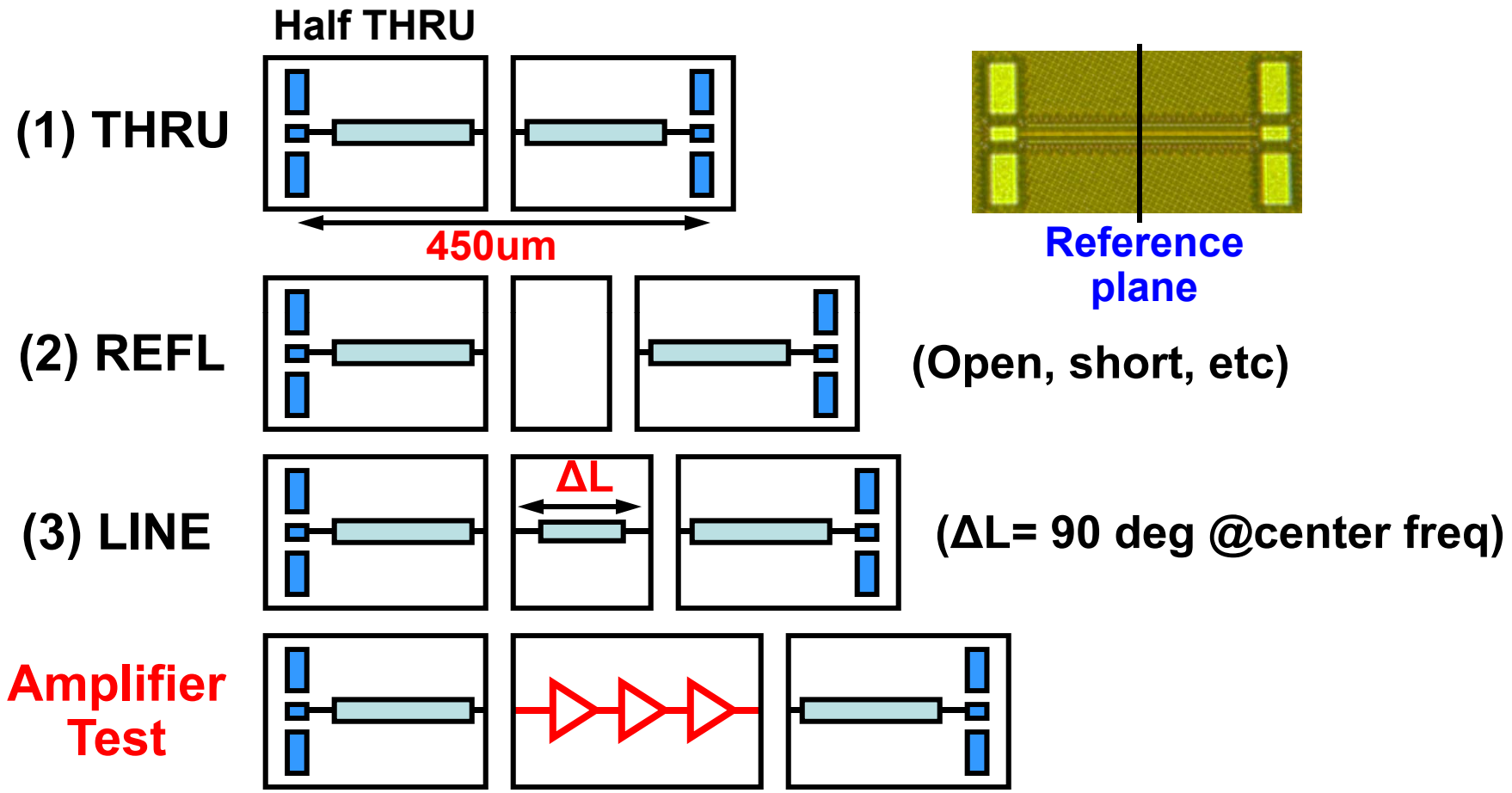


Where current flow is uniform
(e.g. under MS-line)



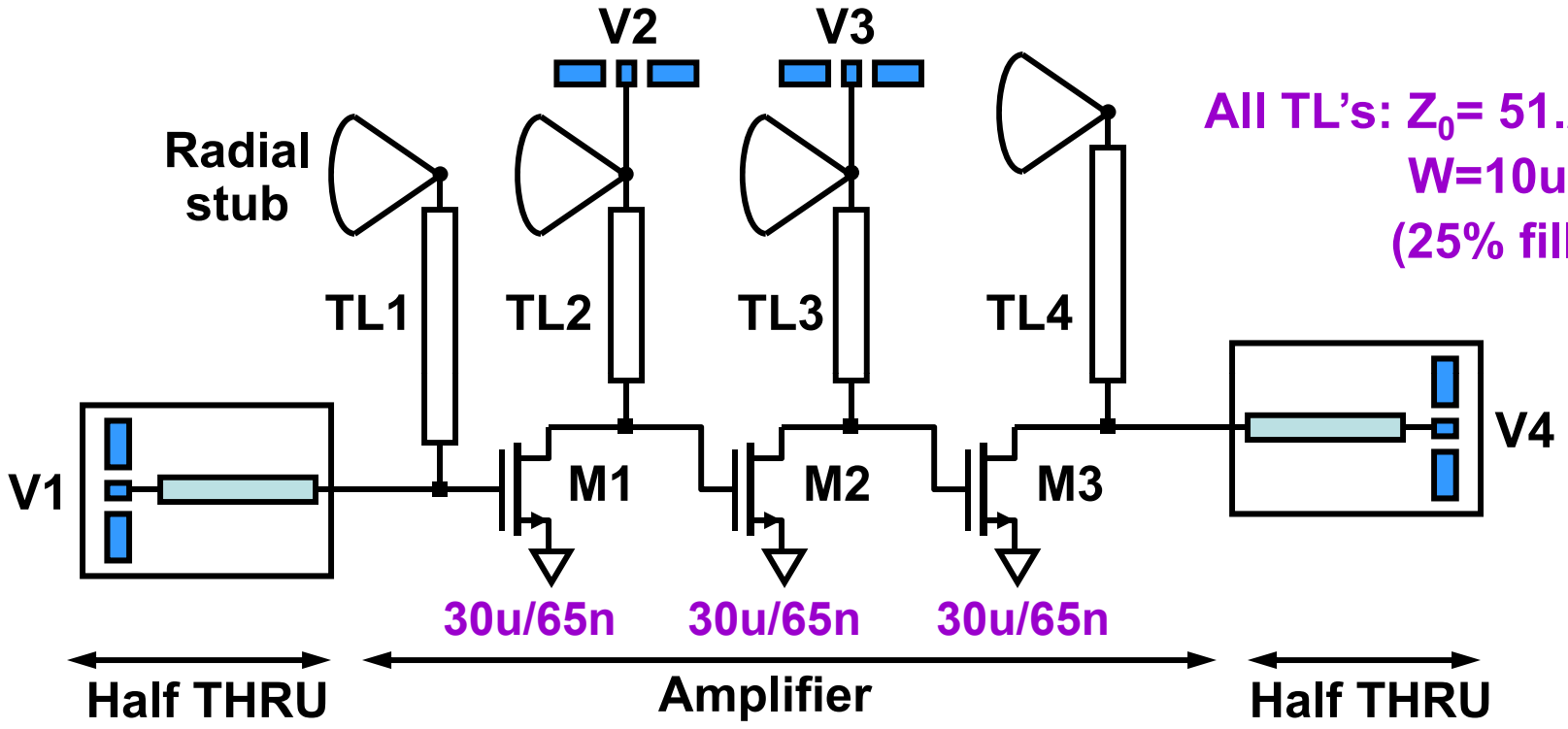
Where current flow is not uniform
(e.g. under bends, T-junction,
radial stubs)

THRU-REFL-LINE (TRL) Calibration



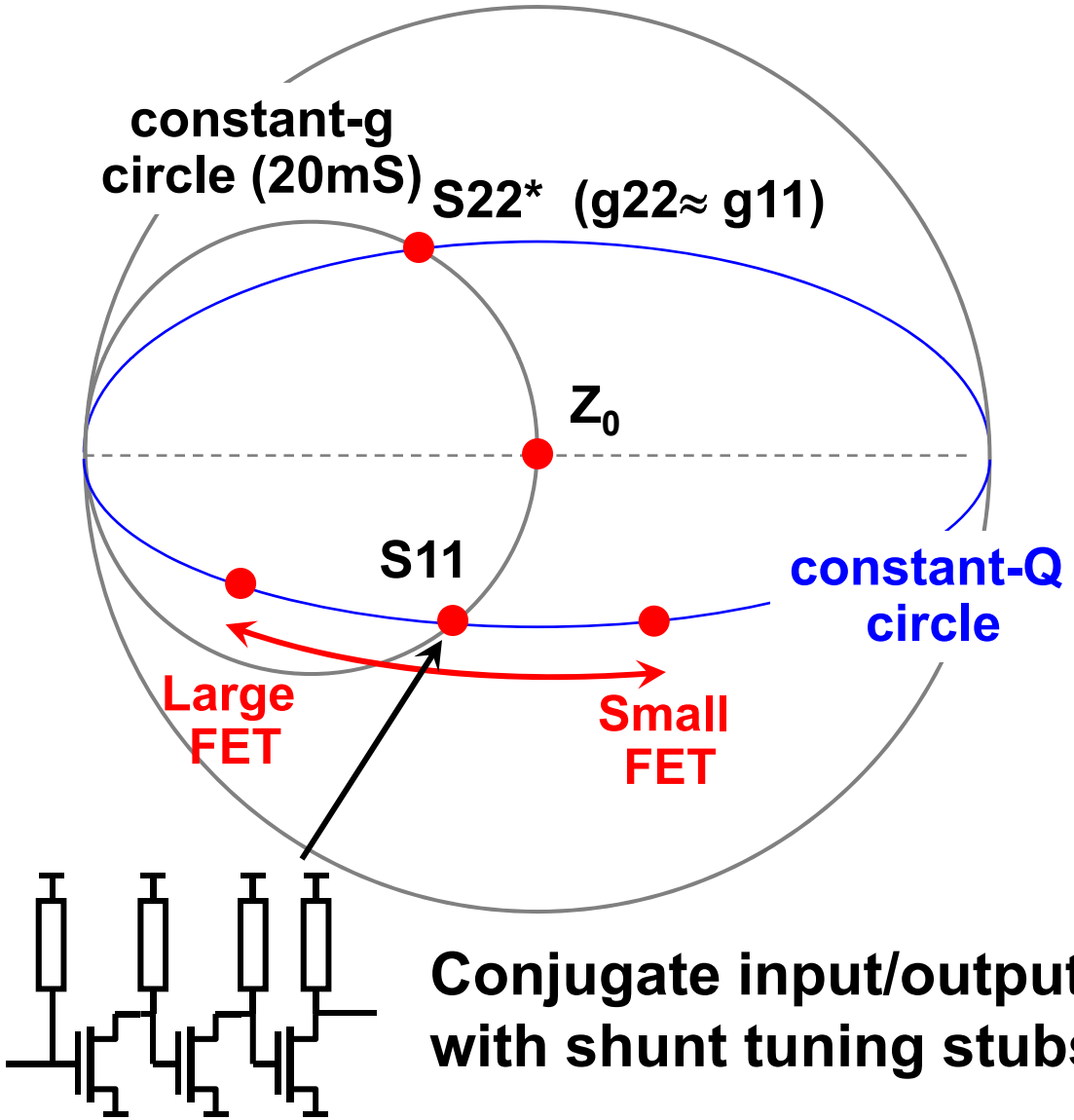
- REFL & LINE need not be accurately known
- Measurements normalized to the line impedance

3-Stage 150GHz Amplifier: Schematic



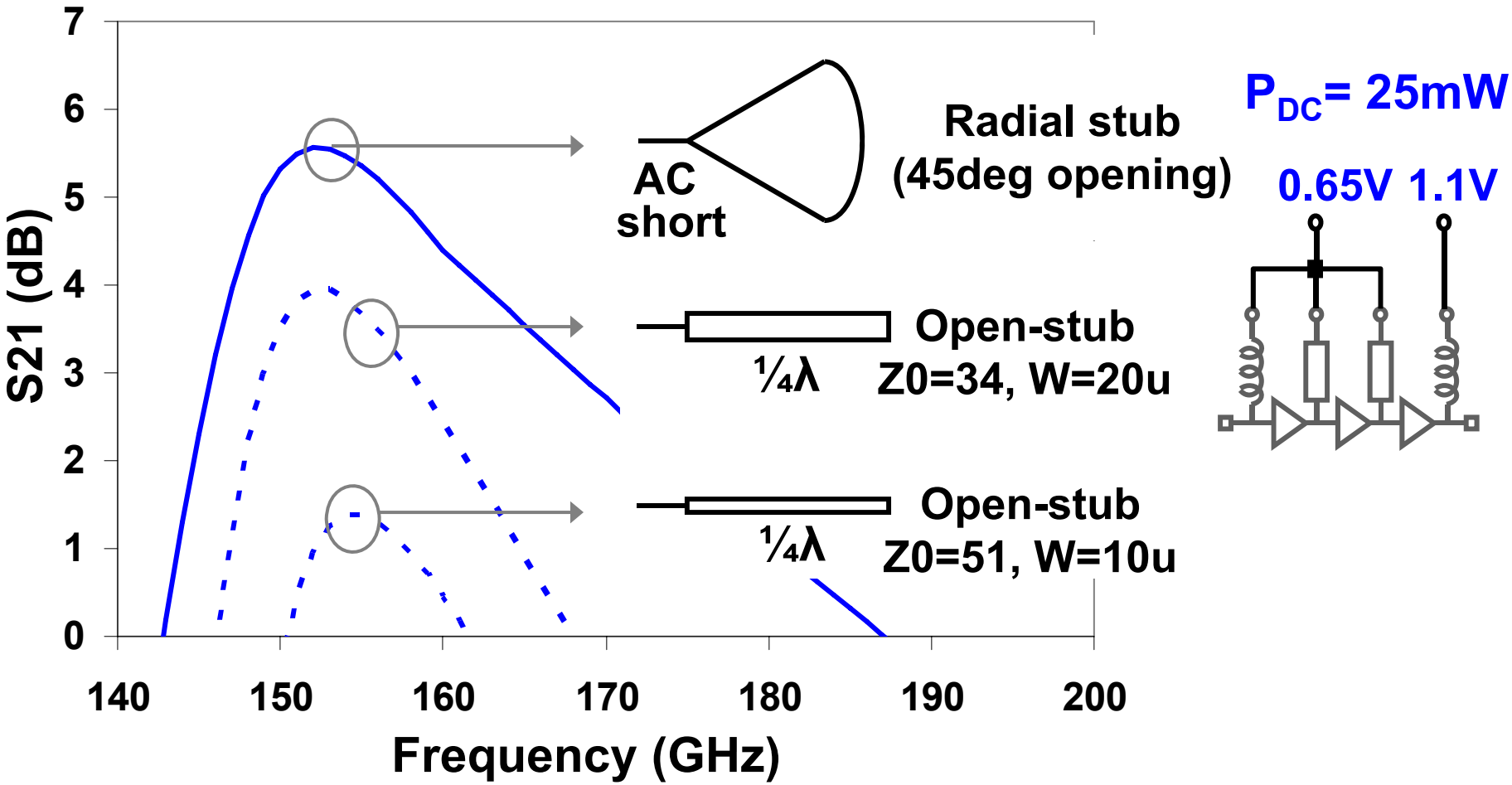
- No DC block: Forces V_{GS}=V_{DS} for M1 & M2, but eliminates loss and modeling uncertainties associated with DC-block cap
- FET size is chosen for low matching loss
- Radial stub for lower loss than quarter-wave TL

FET Sizing

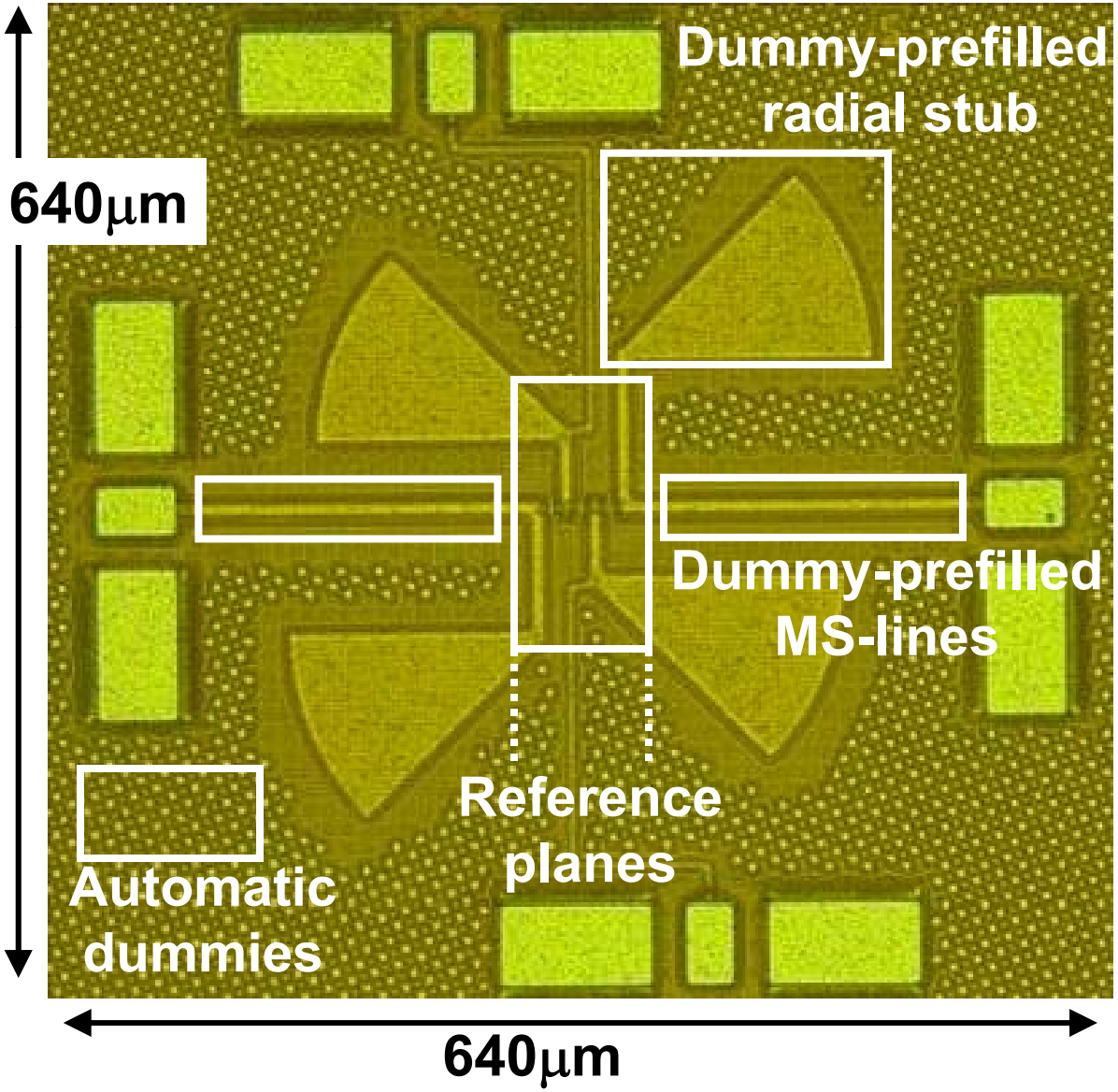


Conjugate input/output/inter-stage match with shunt tuning stubs only.

Simulated 150-GHz Amplifier Gain

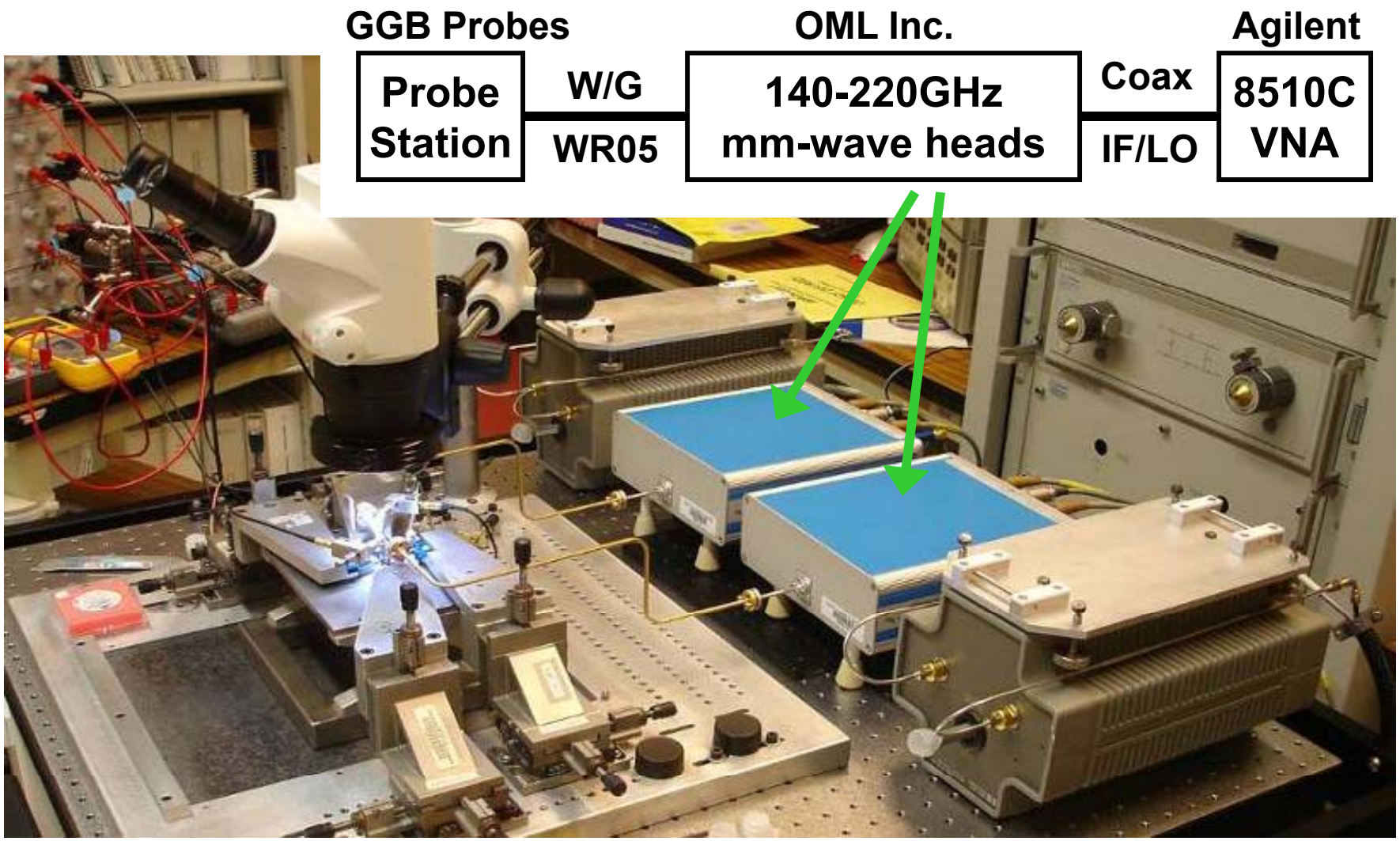


Die Photograph

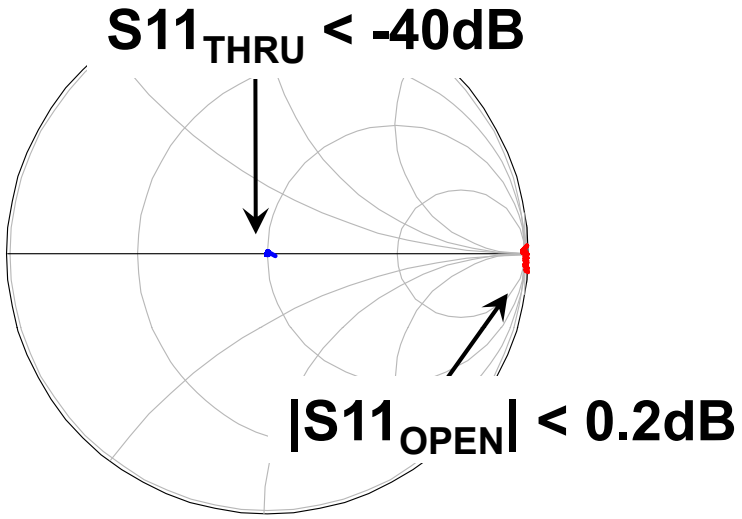


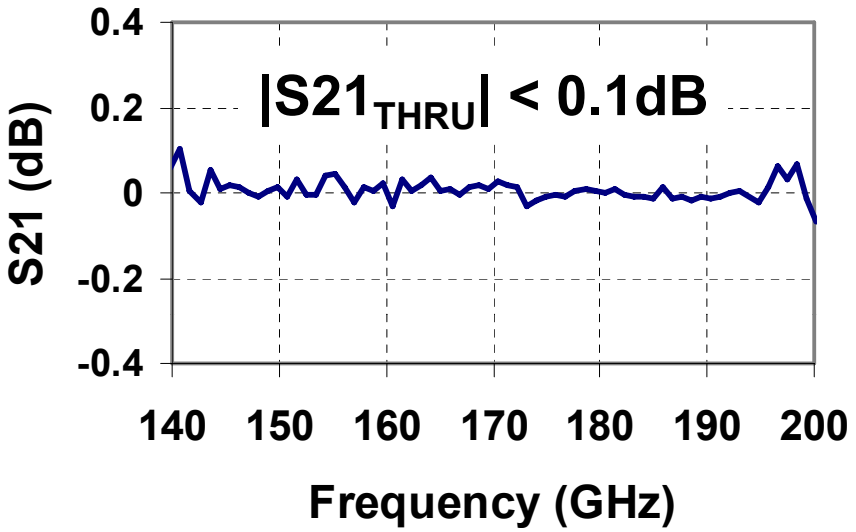
- Area
  = 0.4mm² (w pads)
  = 0.16mm² (w/o pads)
- Stack: 9 Cu + 1 Al

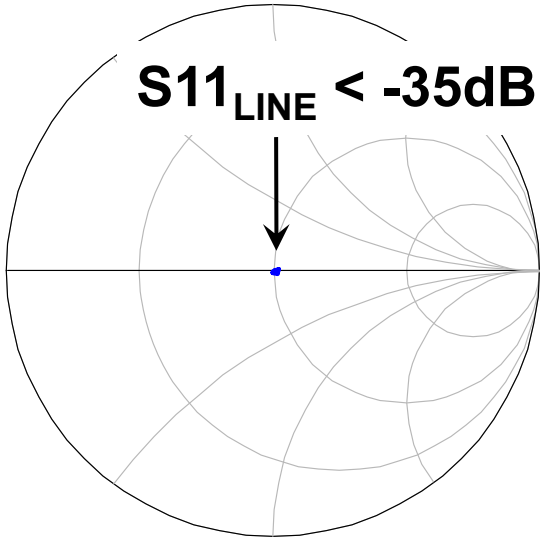
S-parameter Measurement Setup



Can we trust the calibration?

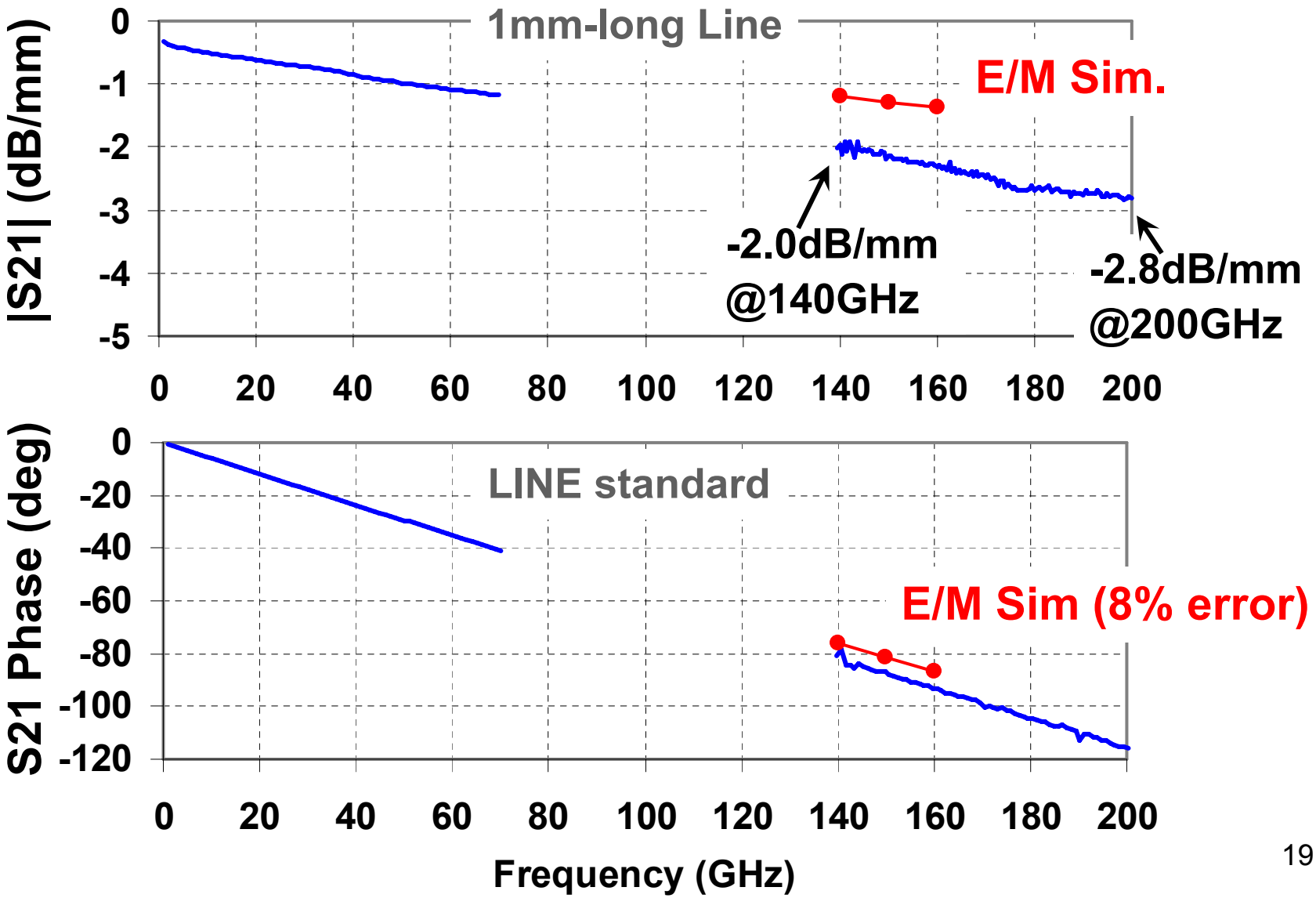




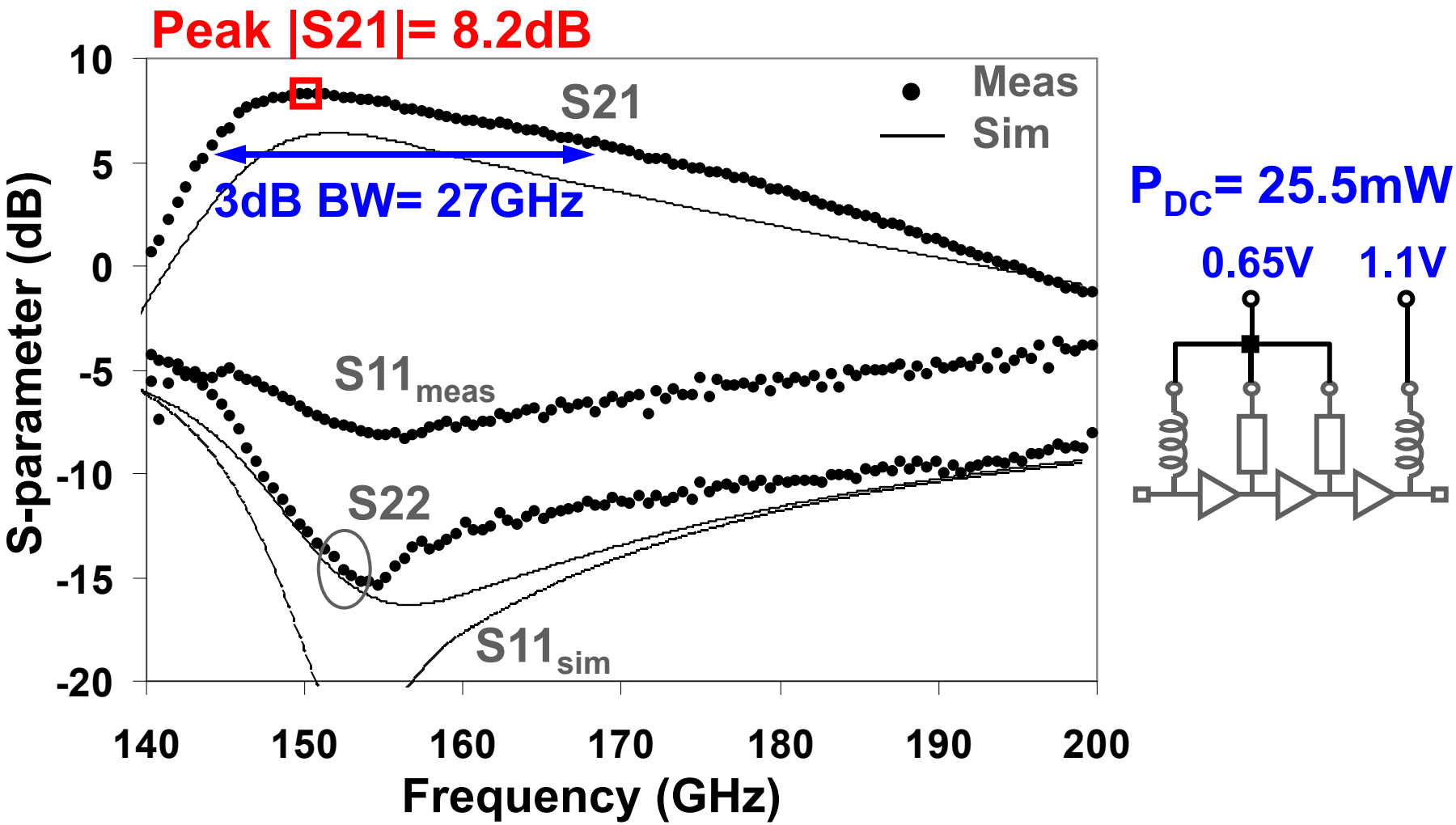


- **Probe coupling < -40dB**
- **Repeatability issues**
  - Probe placement
  - Probe contact resistance

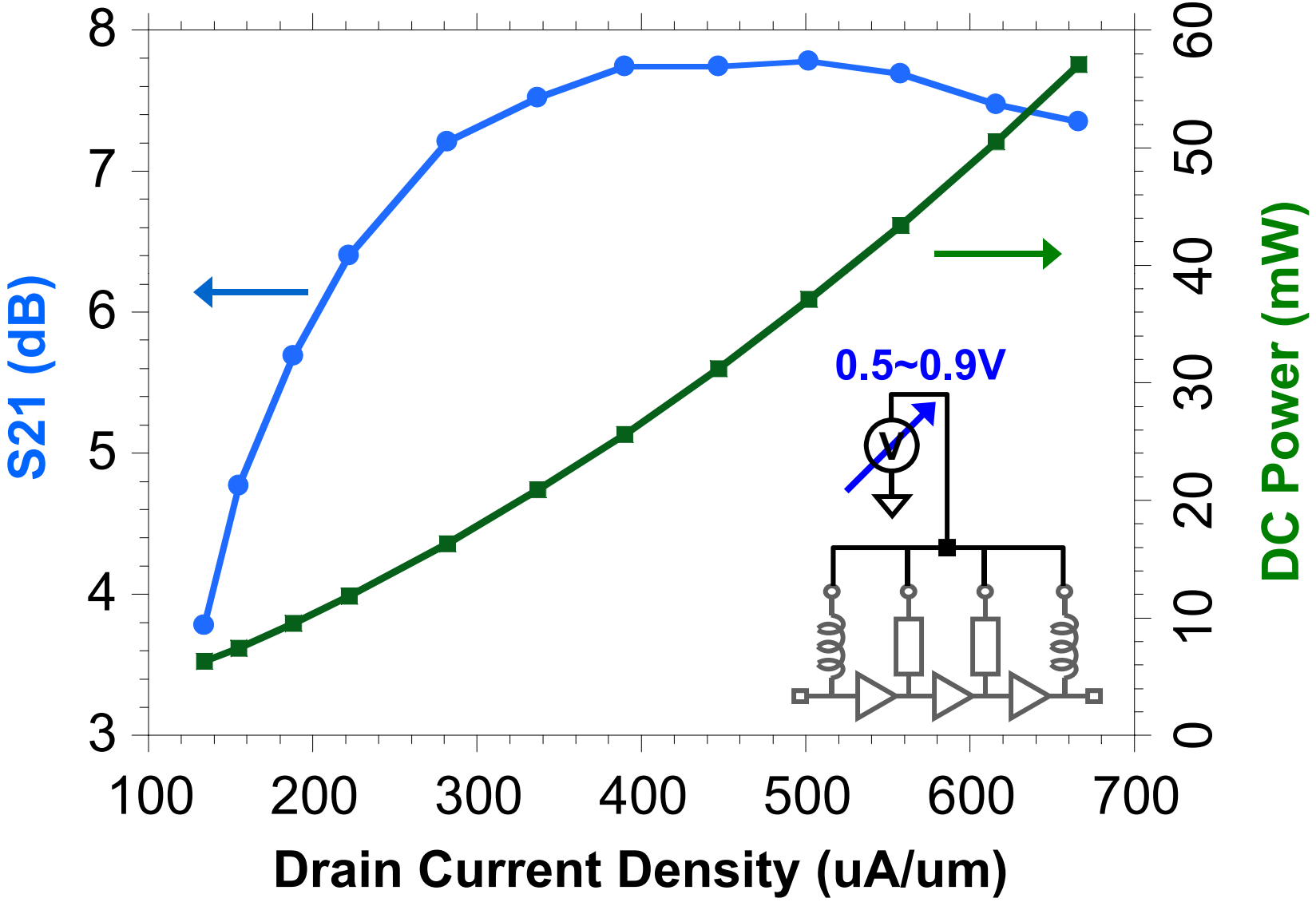
Prefilled MS-Line: Measurement



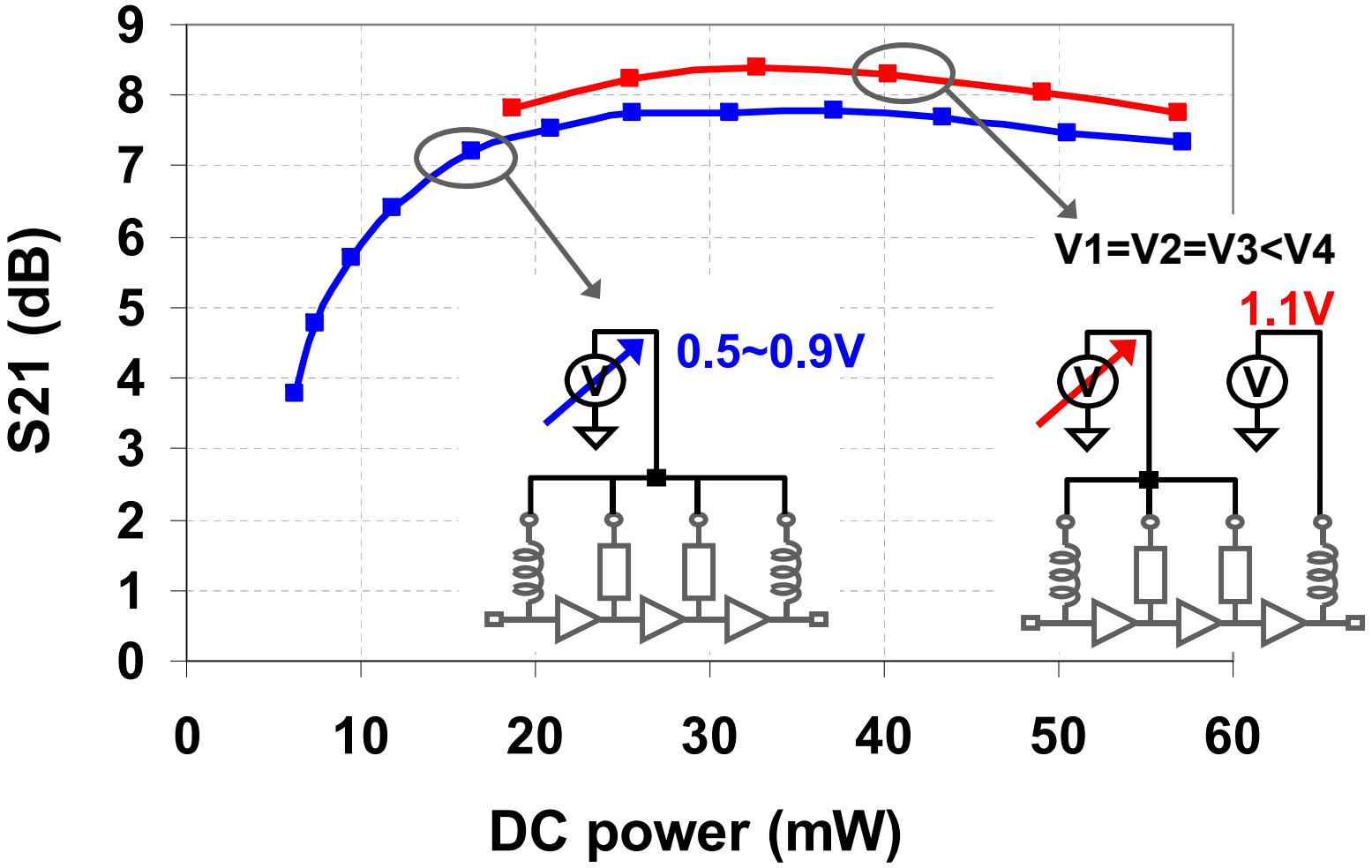
Measured Amp. S-Parameters



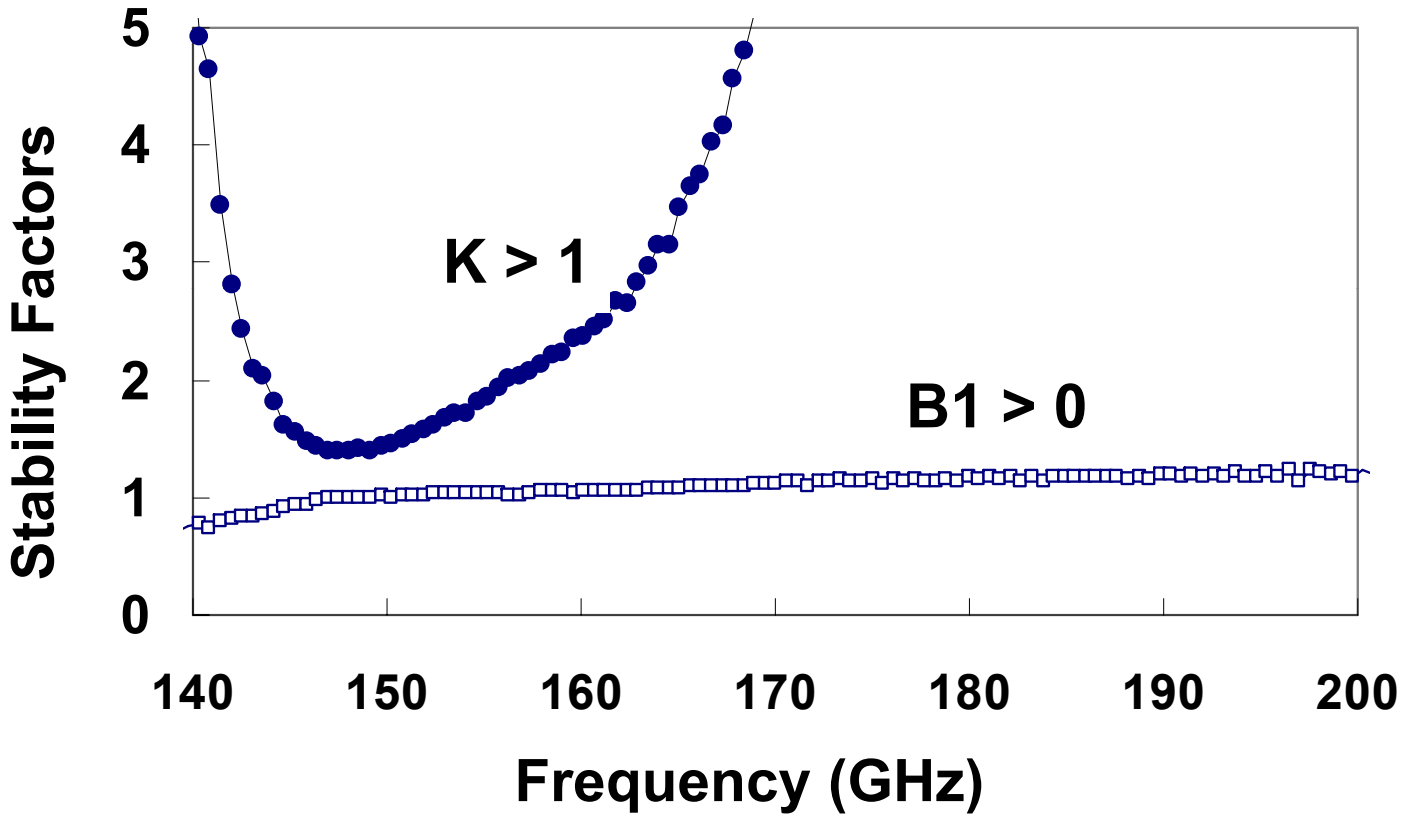
S21 versus Current Density



S21 @Higher Drain Bias (M3)

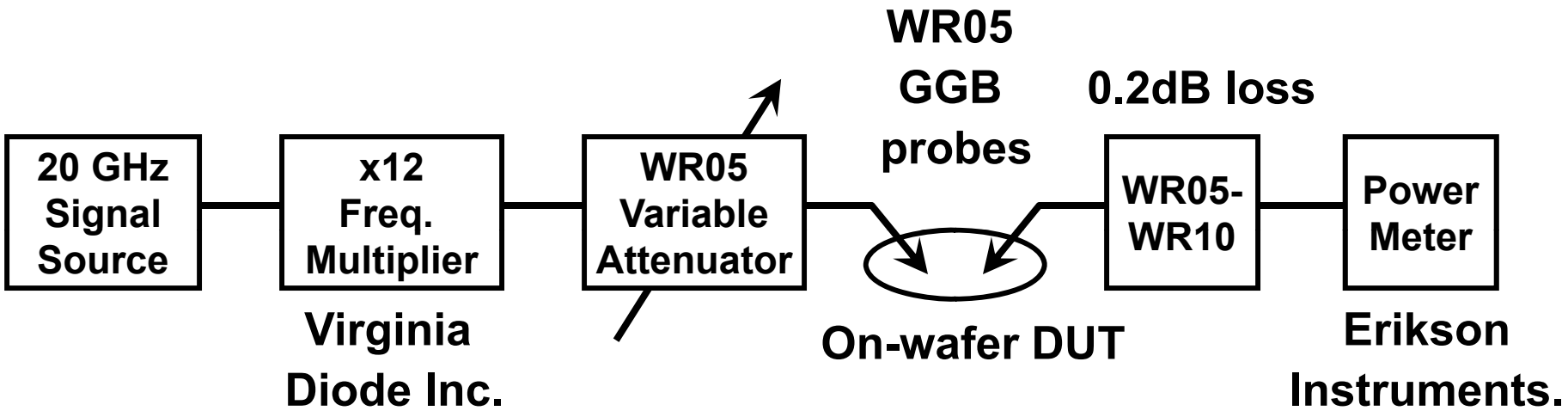


Amplifier Stability Factor



- **Unconditionally stable over 140-200GHz.**

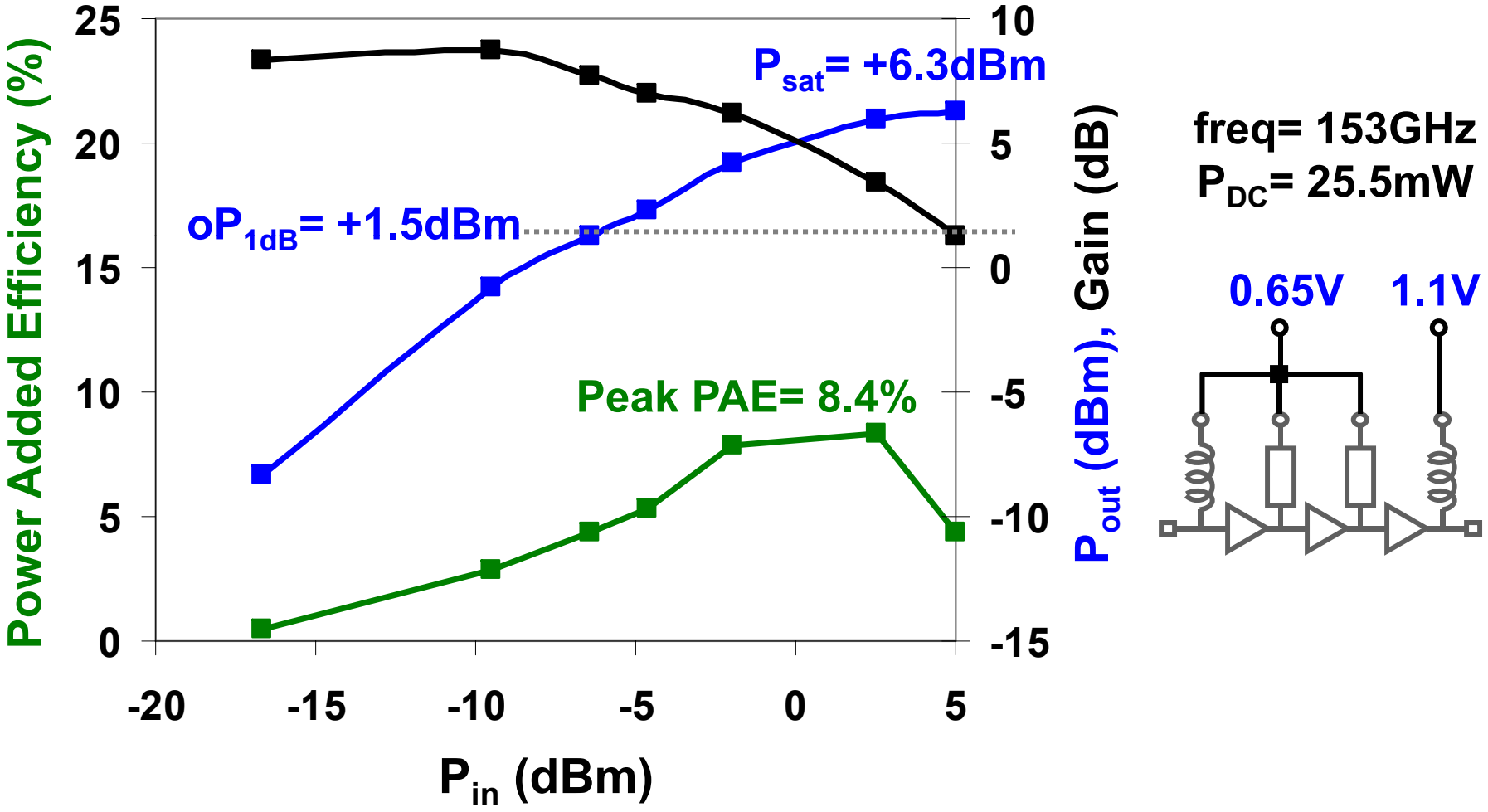
Large-Signal Setup



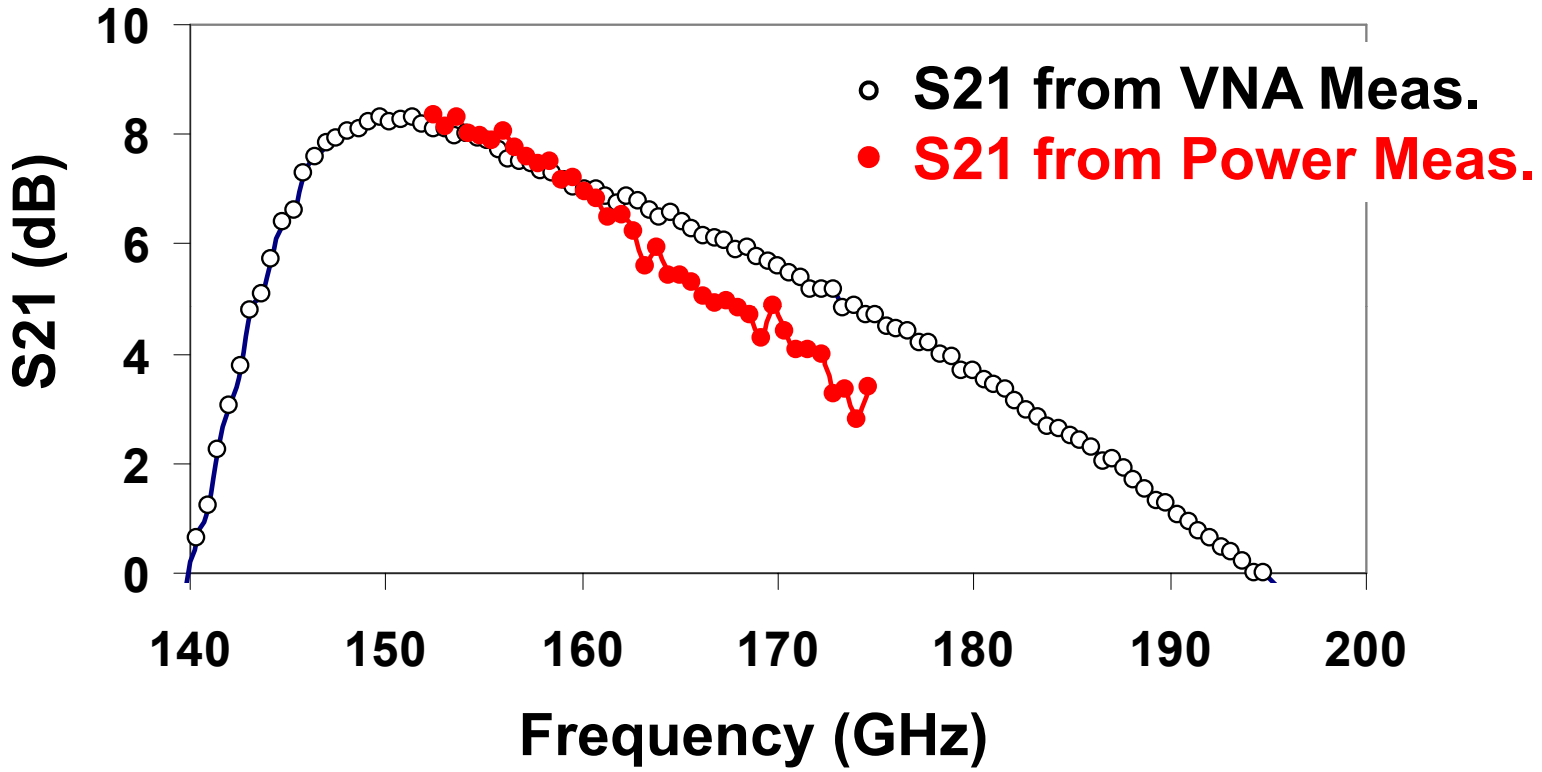
P_{IN}= -20dBm ~ +15dBm
Freq= 153GHz ~175GHz

- Power correction: Insertion calibration using W/G THRU & On-wafer THRU

Large-Signal Characteristics



Comparison of Measured S21



- VNA Measurement: Full 2-port TRL calibration
- Power Measurement: Insertion calibration

Performance Summary

Technology	65nm digital CMOS
Topology	3-stage Common-source
Center freq	150GHz
3dB BW	27GHz
Peak Gain	8.2dB
Input RL	-7.4dB
Output RL	-13.6dB
DC Power	25.5mW
P_{1dB}	+1.5dBm
P_{sat}	+6.3dBm

Conclusion

- **Minimalistic Circuit Design Strategy**
- **“Design-rule Compliant” Transmission Line Structure and Modeling**
- **Linear/Power measurement up to 200GHz**
- **Highest frequency CMOS amplifier reported to date**

Acknowledgement

- IBM for chip fabrication and support
- OML Inc.
- This work was supported by the NSF under grants CNS-0520335 and ECS-0636621