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29.1 A 1.1V 150GHz Amplifier with 8dB Gain and +6dBm Saturated Output Power in Standard Digital 65nm CMOS Using Dummy-Prefilled Microstrip Lines

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Radio applications beyond 100GHz that will benefit from silicon technologies [1-5] include high-rate communication links, medical imaging systems, and chemical sensors. Challenges in CMOS mm-wave front-ends include low available transistor gain and strict metal density rules which alter passive element characteristics [1, 2, 5, 6].

This paper presents the first 150GHz amplifier in a digital 65nm CMOS technology. Design techniques to preserve raw transistor gain near f_{max} include layout optimization, dummy-prefilled microstrip lines (MSL) for design-rule compliance, and matching topologies which minimize passive element losses. To the authors' knowledge, the measured 8.3dB gain, 6.3dBm saturated output power (P_{sat}), 1.5dBm P_{1dB}, 25.5mW DC dissipation (P_{DC}), and 27GHz 3dB BW are among the best in either CMOS or SiGe beyond 110GHz.

The design kit transistor layout was slightly modified to reduce external gate resistance and gate-drain inter-finger capacitance. Examination of design rules suggested gate-drain inter-finger capacitance can be reduced at similar access resistance by modifying the contact structures. Double-sided gate contacts were chosen with W=1μm unit finger. Figure 29.1.1 illustrates two representative gate wiring styles. The external gate resistance ($R_{g,ext}$) of a parallel gate feed (PGF) and a series gate feed (SGF) scale as $1/N_{finger}$ and N_{finger}, respectively, to first order. PGF was chosen for its lower $R_{g,ext}$ despite its increased overlap C_{gs}. Gate feed resistance arises mostly from within the fingers, and therefore external wiring capacitances do not significantly reduce Mason's Unilateral gain (U). Measurement in Fig. 29.1.1 shows that PGF yields 4.8dB of maximum stable gain (MSG) at 150GHz, 1dB higher than SFG.

Impedance matching based on lumped elements has been demonstrated beyond 100GHz [1-3,6,7], enabling compact IC layout. This approach requires accurate modeling of MIM capacitors and spiral inductors, including their resonance frequency. Microstrip line (MSL) matching networks [5,8] have more predictable parameters, but consume more die area. Furthermore, the automatic addition of metal dummies to meet density requirements complicates transmission-line modeling. In this work, MSL-based matching is chosen. At 150GHz, an MSL loaded quarter wavelength is only ~240μm, resulting in ×2.5 area reduction over similar 60GHz designs. To accurately control the line characteristics while meeting metal density rules, an array of dummies is prefilled around MSL (Fig. 29.1.2). The size (W_D) and spacing (S_D) of prefillers are chosen to prevent automatic cheesing on prefillers or dummy filling under the controlled area.

The most notable effect of dummies is increased line capacitance. Dummies are typically too small to support image current, and thus do not change the line inductance. Electromagnetic simulation of a full dummy-filled structure is not feasible with present computers. Furthermore, because of the anisotropic dummy shape, the effective dielectric constant (ε_r) depends on field orientation, further complicating modeling. Modeling is simplified because (Fig. 29.1.2) the MSL E-field is nearly vertical in the bottom dielectric region. By simulating a parallel-plate capacitor (with vertical E-field), an adjusted ε_r of an equivalent dummy-free layer can be obtained for the same capacitance per unit area. Similar substitutions are subsequently applied to intermediate filling layers. For the uppermost filling layers, the E-field is no longer vertical, hence such substitutions cannot be applied; the lines are modeled including these uppermost fillers.

Figure 29.1.3 shows the 3-stage 150GHz amplifier schematic. All MSL's are 50Ω after 25% dummy prefilling. The signal line uses 1.2μm-thick top-layer metal, and two bottom metal layers constitute the ground plane. The stages are DC-coupled, which forces equal V_{gs} and V_{ds} (both 0.65V for I_d=330μA/μm). While this reduces the FET MSG by 0.4dB relative to peak-gain DC bias, DC coupling eliminates both losses and potential model errors associated with decoupling capacitors and their parasitic inductances, thereby easing design. Higher circuit gain is therefore obtained. Saturated output power is, however, not sacrificed since M_3 can have full drain bias up to 1.1V. Series tuning elements are also eliminated so as to reduce associated line losses; instead devices sizes (W=30μm for M_1, M_2, M_3) are chosen so that low return loss is obtained in a 50Ω environment without series tuning. Shunt tuning elements resonate with the FET capacitances at the design frequency; these are terminated by quarter-wave radial stubs. These provide ~1.4dB less matching loss than would 50Ω quarter-wave MSL bias decoupling lines. The final layout is 0.64×0.64mm^2 including pads.

On-wafer calibration is performed using on-wafer thru-reflect-line (TRL) calibration standards (Fig. 29.1.3) with the probe pads placed 200μm distant from the reference planes. The amplifier S-parameters were measured from 140GHz to 200GHz using HP8510C and G-band OML mm-wave heads (Fig. 29.1.4). The measured S_{21} is 8.3dB at 150GHz and remains above 0dB until 190GHz, validating the design. The amplifier consumes 25.5mW of P_{DC} at V_1=V_2=V_3=0.65V and V_4=1.1V. An equivalent FET circuit model is obtained by fitting to design kit FET models up to 60GHz, and is subsequently used in simulation. The amplifier remains unconditionally stable over the entire band. Measured loss of a 1mm-long MSL is 2.2dB and 2.8dB at 150GHz and 200GHz, respectively, suggesting that prefilled MSL can be used at even higher frequencies. Probe-tip calibration at lower frequencies (from 1 to 67GHz) confirmed Z_0 of the prefilled line closely matches the design value.

Figure 29.1.5 shows measured large-signal characteristics of the 150GHz amplifier. A multiplier diode module from Virginia Diodes, Inc. generates RF power from 153GHz and above, and a calorimeter from Erikson Instruments measures the output power. All power measurements are calibrated to the reference planes in Fig. 29.1.3 by separately measuring the THRU standard. Measured P_{sat} is 6.3dBm and 6.7dBm, and P_{1dB} is 1.5dBm and 2dBm, at 153GHz and 158.4GHz, respectively, at V_1=V_2=V_3=0.65V and V_4=1.1V. P_{sat} and P_{1dB} increase by +0.7dB at V_4=1.3V. Peak power-added efficiency (PAE) was measured to be 8.4% and 9.5%, at 153GHz and 158.4GHz, respectively. Sweeping the frequency from 153GHz to 175GHz at –10dBm input power produced a gain curve similar to VNA measurement (Fig. 29.1.4).

Figure 29.1.6 compares this work with previously published state-of-the-art mm-wave amplifiers in silicon. Beyond 100GHz, use of simple matching topologies is key to preserving device gain and output power. These matching networks have low Q, hence extend circuit bandwidth. These circuit techniques, combined with optimized transistor layout and systematic modeling of design-rule compliant MSL, will push the frequency limit of 65nm digital CMOS to even beyond 150GHz.

Acknowledgements:
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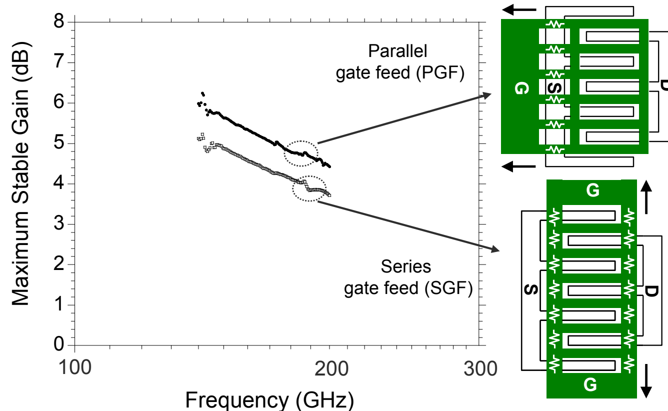

Figure 29.1.1: Measured MSG of 65nm W=10μm FET at V_{gs}=V_{ds}=0.65V.

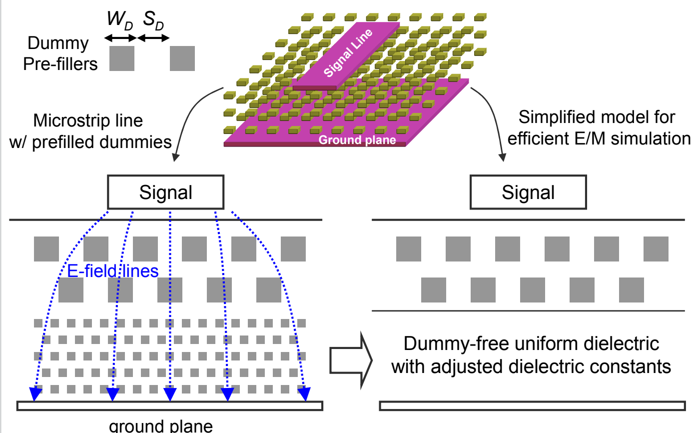

Figure 29.1.2: Dummy-prefilled microstrip line and its simplified equivalent model.

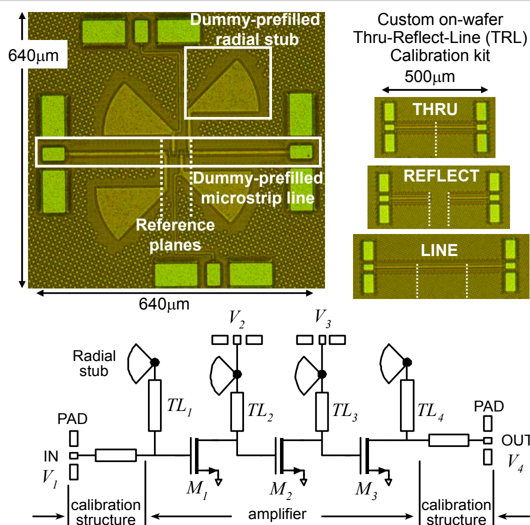

Figure 29.1.3: Schematic and die micrograph of the 3-stage 150GHz amplifier and on-wafer TRL calibration kit.

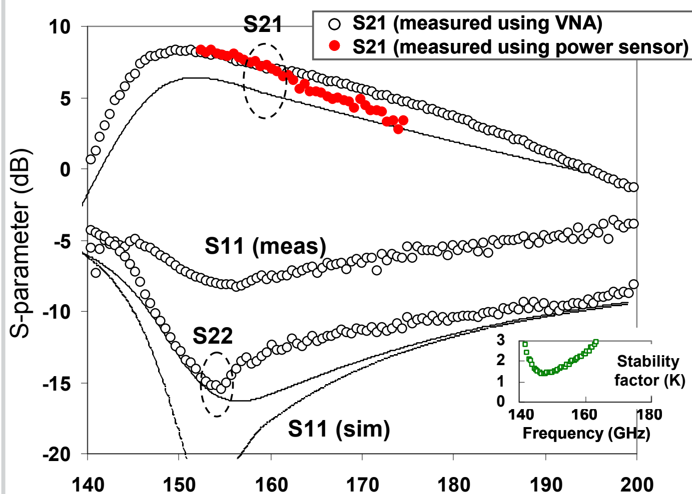

Figure 29.1.4: Measured (circles) and simulated (solid lines) S-parameters at V_1=V_2=V_3=0.65V and V_4=1.1V (P_{DC}=25.5mW).

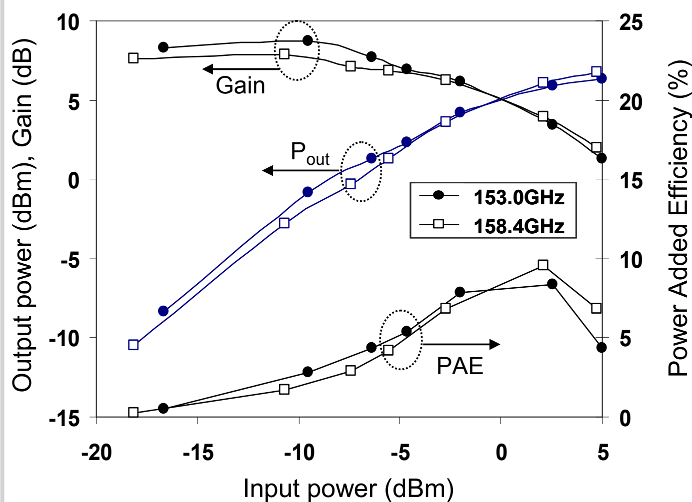

Figure 29.1.5: Measured large-signal characteristics at V_1=V_2=V_3=0.65V and V_4=1.1V.

	This work	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]
Technology	65nm CMOS	SiGe HBT	65nm CMOS	SiGe HBT	90nm CMOS	90nm CMOS	65nm CMOS	65nm CMOS	90nm CMOS
f center [GHz]	150	170	140	140	103.8	97	95	80	77
3dB BW [GHz]	27	14	10	18	5#	22	> 19	20	17.5
Gain [dB]	8.2	15	8	18	9.34	17.4	13	13.5	8.5
No. of stages	3	5	6	5	3	3	3	3	4
S_{11} [dB]	-7.4	N/A	N/A	-12*	-9.8	< -15	-15	-20	N/A
S_{22} [dB]	-13.6	N/A	N/A	-19*	-5.5	< -15	N/A	N/A	N/A
V_{DD} [V]	1.1	3	1.2	3	1	2.5	1.5	1.5	1.2
P_{DC} [mW]	25.5	135	63	112	22	54	35	36.3	142.2
P_{sat} [dBm]	6.3	> 0	> -1.8	N/A	N/A	4	N/A	4	6.3
P_{1dB} [dBm]	1.5	0	-5	-1	N/A	2	> -6	-1.6	4.7
Area [mm^2]	0.4 ×0.4	0.29 ×0.15	0.3 ×0.2#	0.4 ×0.2	0.64 ×0.38#	0.57 ×0.52#	0.12 ×0.12#	0.16 ×0.1#	0.94 ×0.36#

* Simulation
# Estimate from either plots or chip micrographs (not including pads)

Figure 29.1.6: Comparison of mm-wave amplifiers in silicon at or beyond 77GHz.

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