Technology Development for InGaAs/InP-channel MOSFETs

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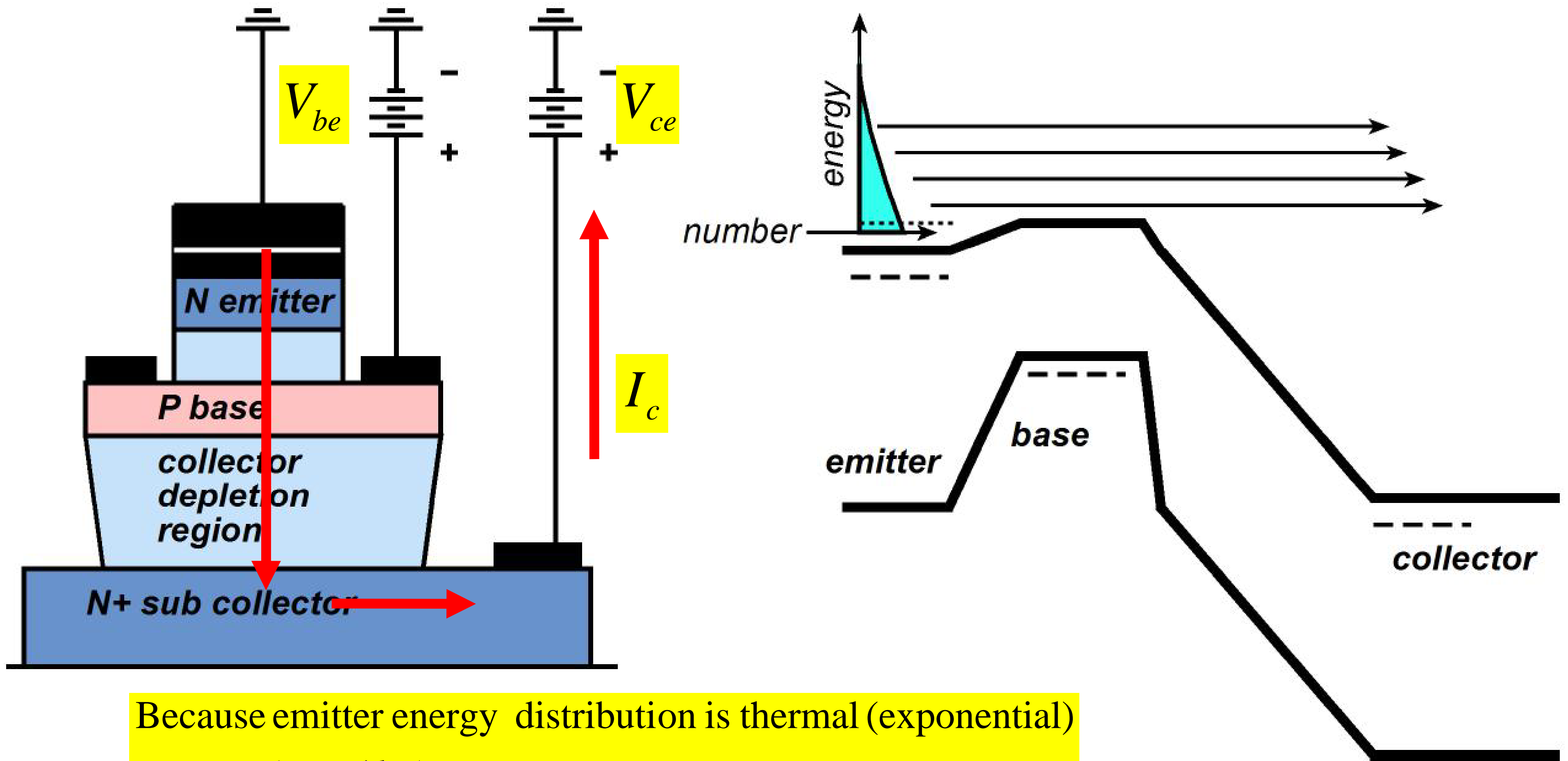
Scope of Presentation

Topic of discussion is channel materials for CMOS
...the potential use of III-V materials
...and their advantages and limitations

To understand this,
we must examine in some detail
MOSFET scaling limits

Zeroth-Order MOSFET Operation

Bipolar Transistor ~ MOSFET Below Threshold



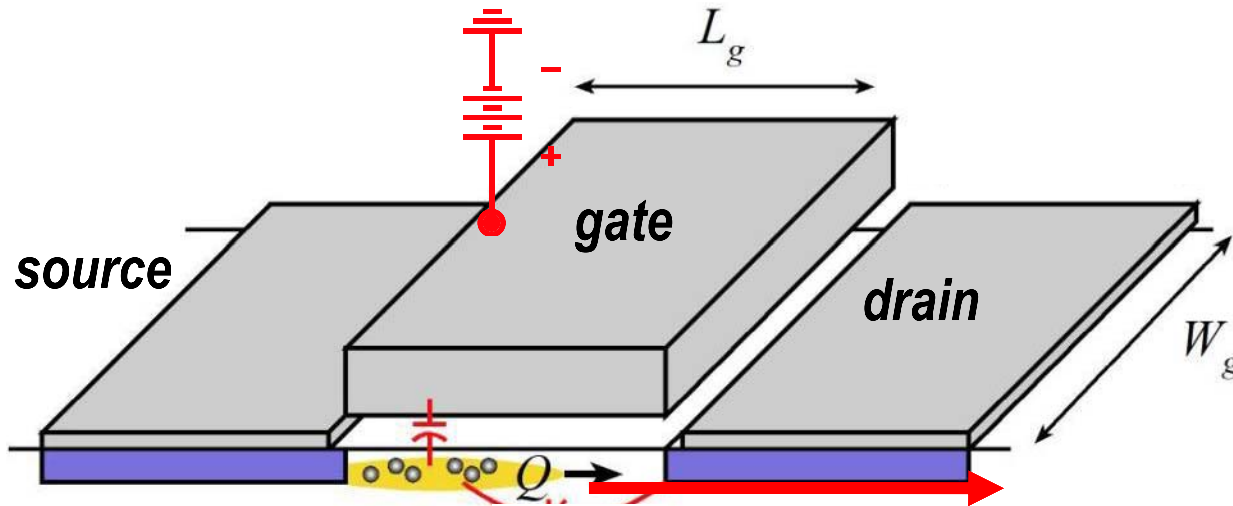
Because emitter energy distribution is thermal (exponential)

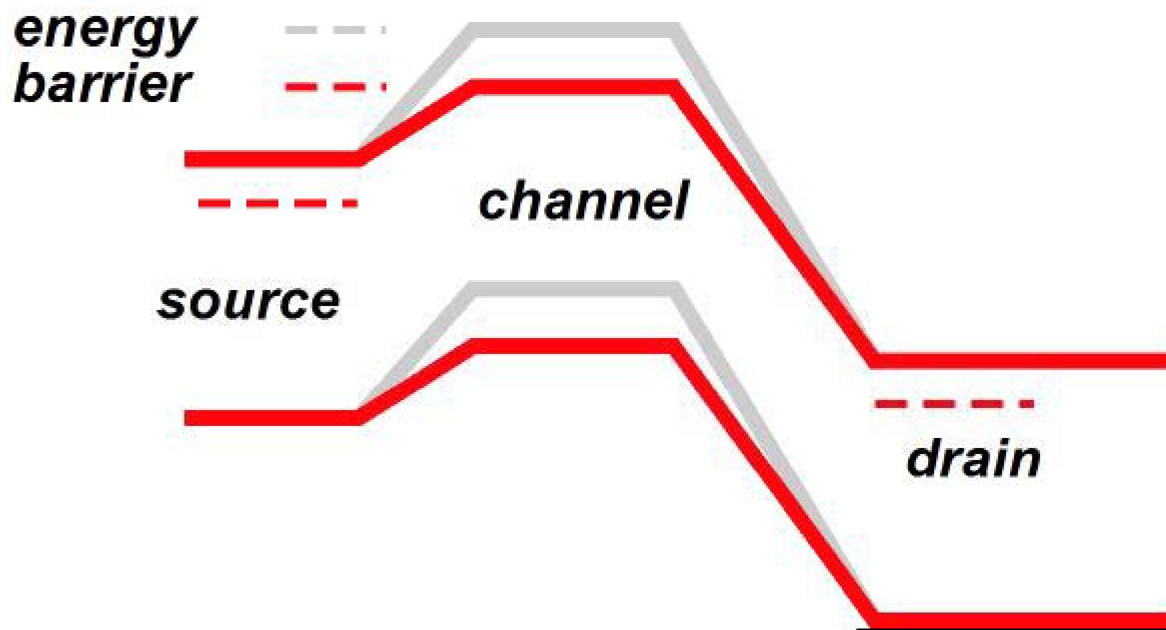
$I_c \propto \exp(qV_{be}/kT)$

Almost all electrons reaching base pass through it

$\rightarrow I_c$ varies little with collector voltage

Field-Effect Transistor Operation



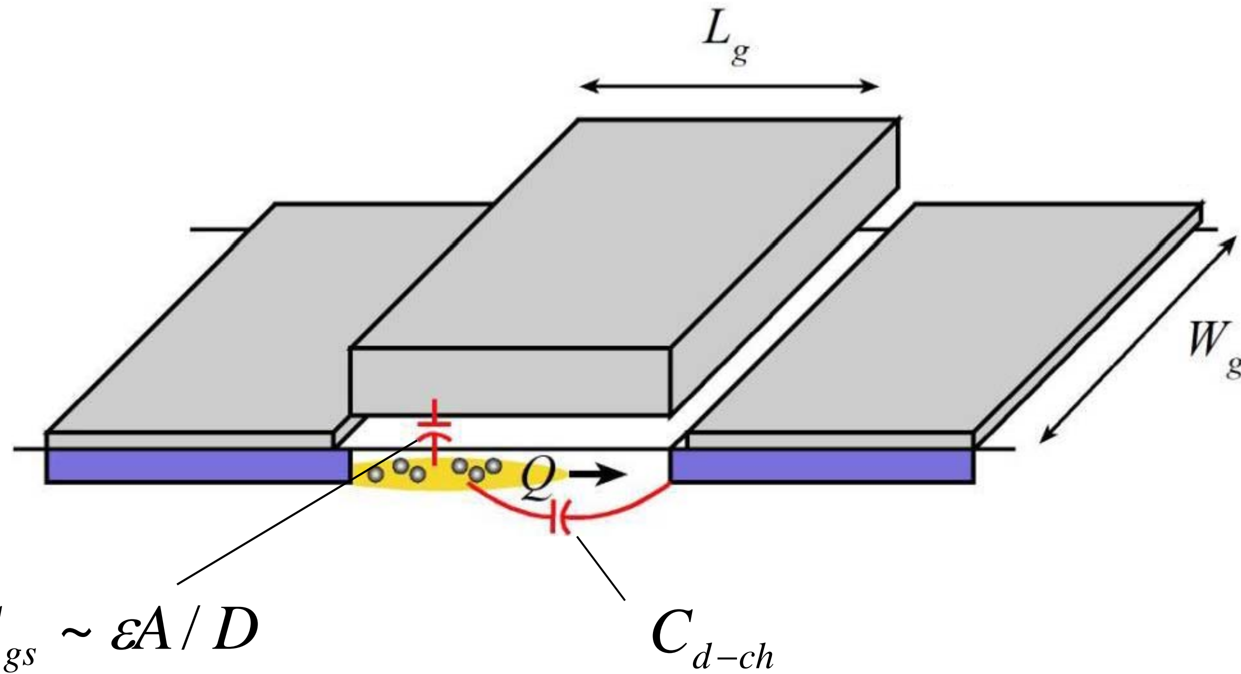


Positive Gate Voltage

→ **reduced energy barrier**

→ **increased drain current**

FETs: Computing Their Characteristics



$$I_d = Q / \tau \quad \text{where} \quad \tau = L_g / v_{electron}$$

$$\delta Q = C_{gs} \delta V_{gs} + C_{d-ch} \delta V_{ds}$$

$$\delta I_d = g_m \cdot \delta V_{gs} + G_{ds} \cdot \delta V_{ds} \quad \text{where} \quad g_m = C_{gs} / \tau \text{ and } G_{gd} = C_{d-ch} / \tau$$

FET Characteristics

L_g

W_g

Q

$C_{gs} \sim \varepsilon A / D$

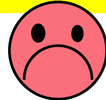
C_{d-ch}

I_D

increasing V_{GS}

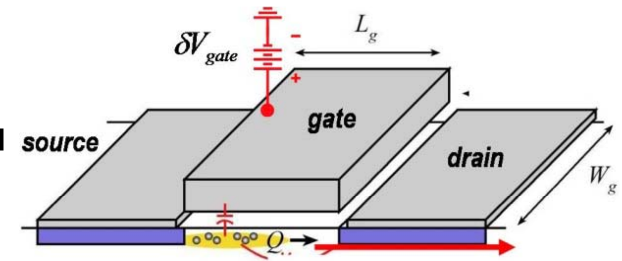
V_{DS}

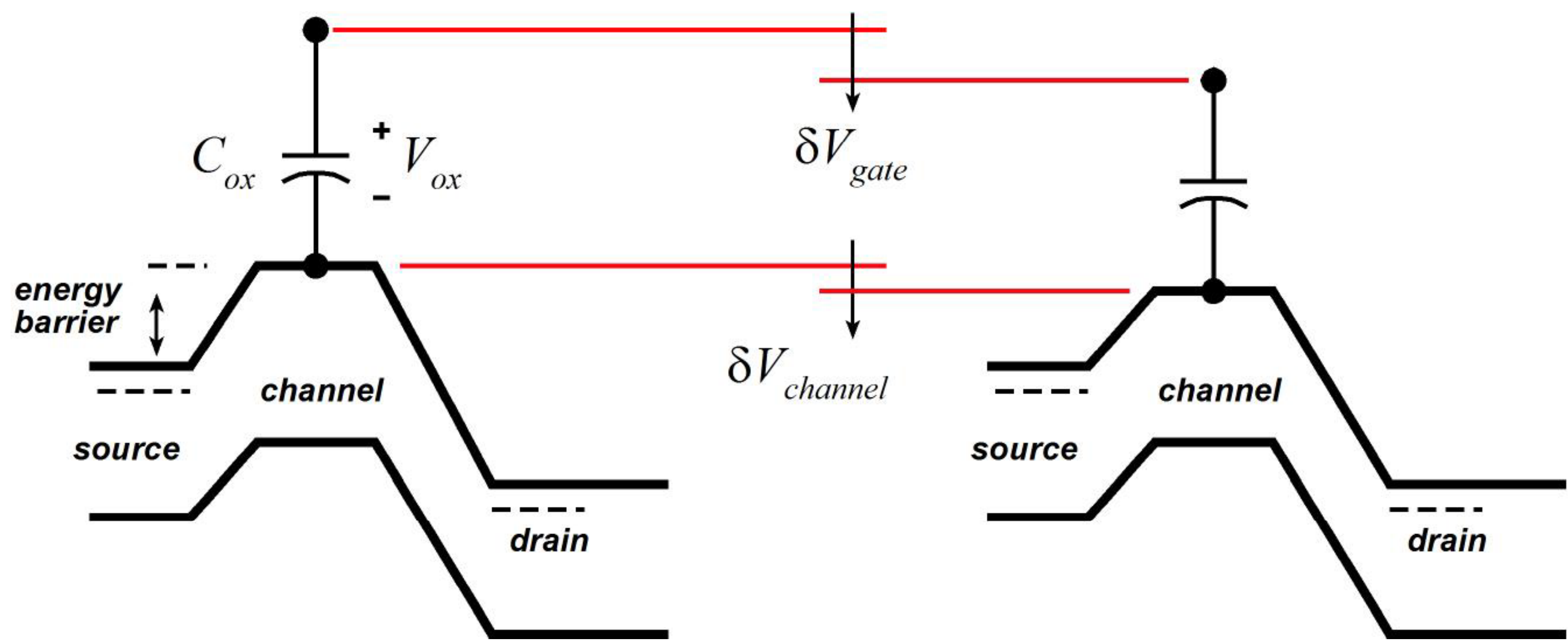
$$\delta I_d = g_m \cdot \delta V_{gs} + G_{ds} \cdot \delta V_{ds}$$



$$g_m = C_{gs} / \tau \quad G_{gd} = C_{d-ch} / \tau \qquad \tau = L_g / v_{electron}$$

FET Subthreshold Characteristics



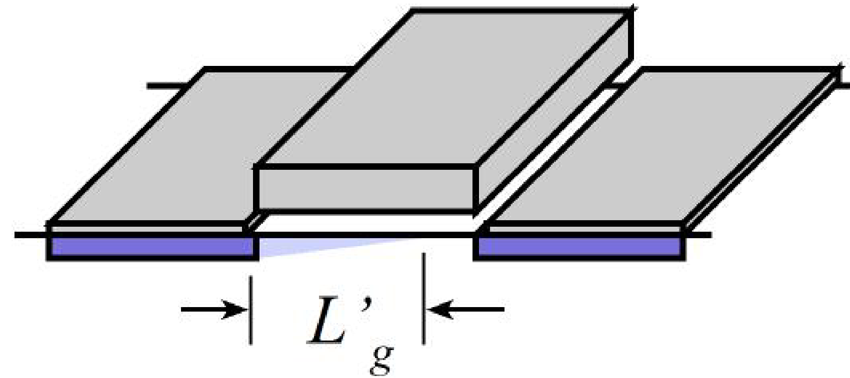


$$\delta V_{gate} = \delta V_{ox} + \delta V_{channel} = \frac{\delta(qn_s)}{C_{ox}} + \frac{\delta(qn_s)}{qn_s} \cdot \frac{kT}{q}$$

Strong gate drive : channel charge varies linearly with V_{gs}

Weak gate drive : channel charge varies exponentially with V_{gs}

Classical Long-Channel MOSFET Theory



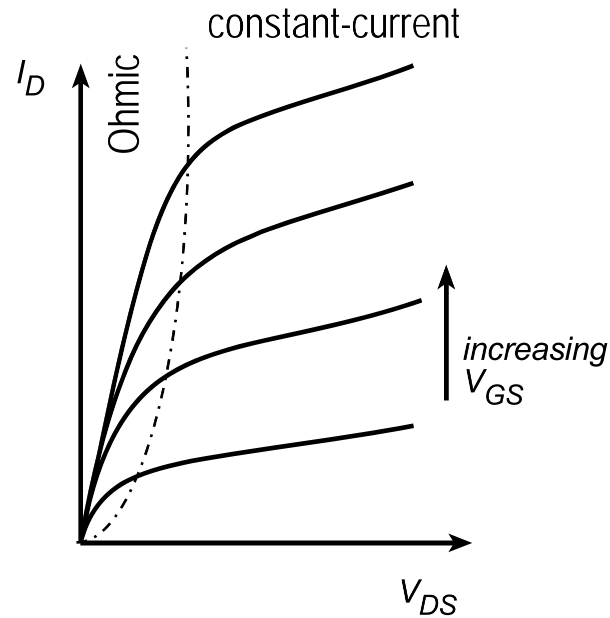
Assumptions :

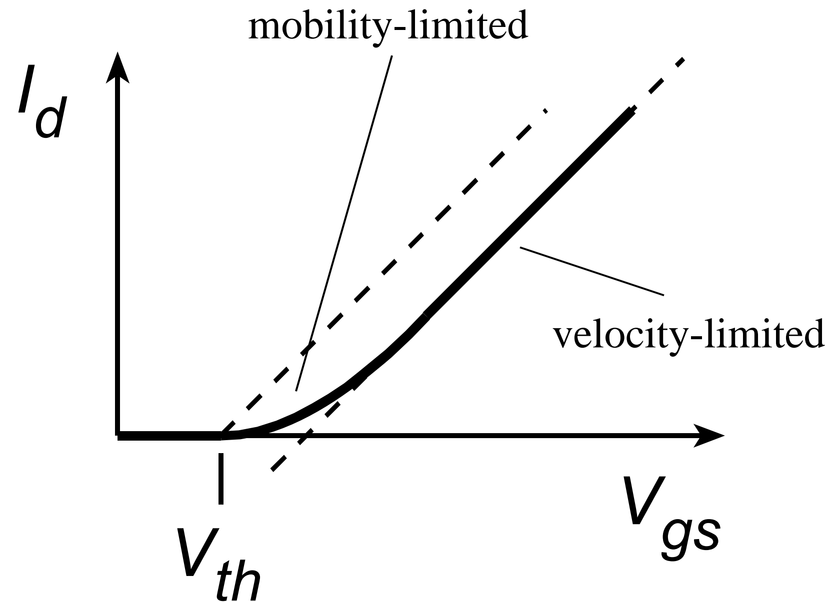
1) Moderate lateral field E in channel.

2) Transport modeled by drift/diffusion $J = q\mu_n n(x)E + qD_n \frac{\partial n(x)}{\partial x}$

3) Exit velocity at end of pinched - off channel : $v_{exit} = v_{thermal} = \sqrt{kT / m^*}$

Classic Long-Channel MOSFET Theory





For drain voltages larger than saturation :

mobility – limited current

$$I_{D,\mu} = \mu c_{ox} W_g (V_{gs} - V_{th})^2 / 2L_g$$

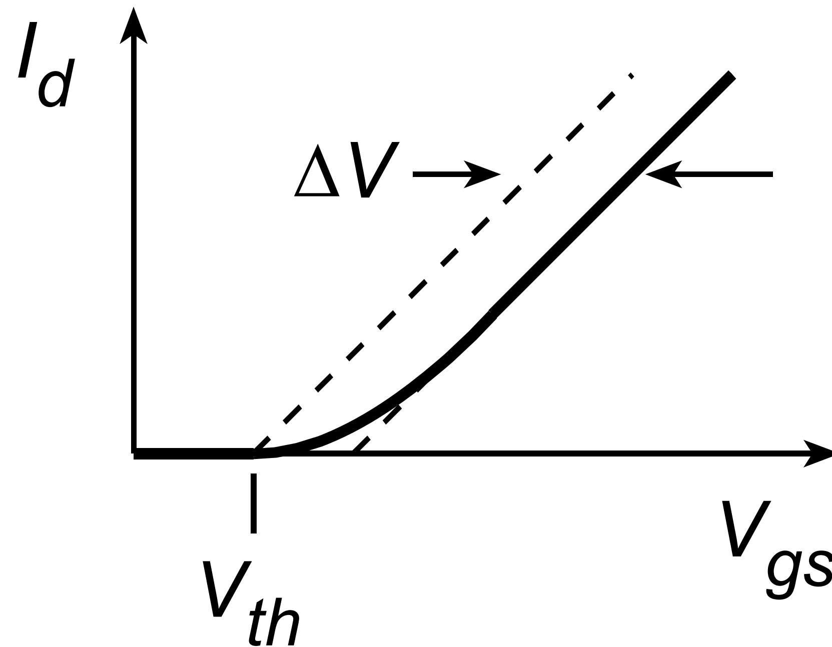
velocity – limited current

$$I_{D,v} = c_{ox} W_g v_{exit} (V_{gs} - V_{th})$$

Generalized Expression

$$\left(\frac{I_D}{I_{D,v}}\right)^2 + \left(\frac{I_D}{I_{D,\mu}}\right) = 1$$

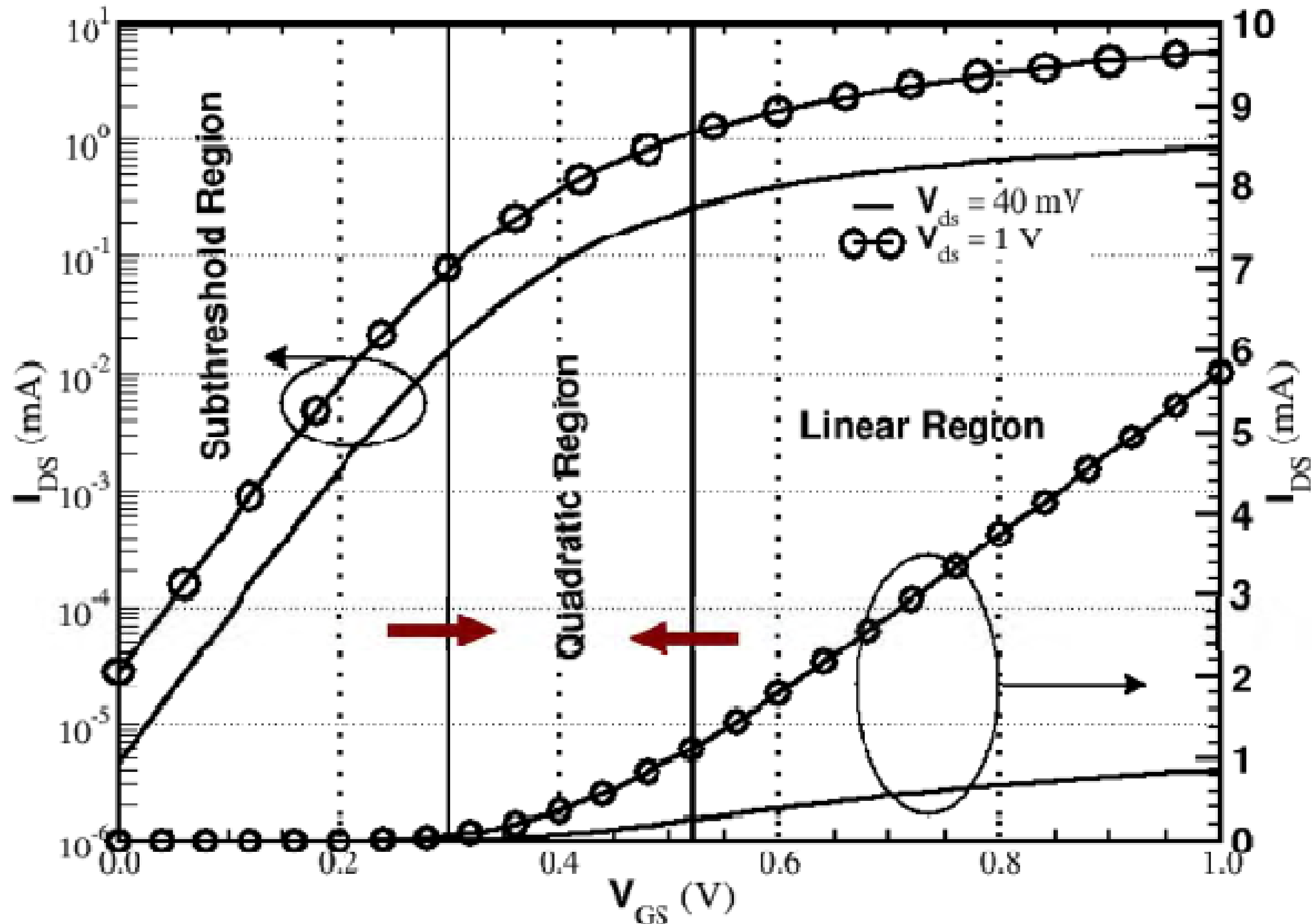
Classic Long-Channel FET : Far Above Threshold



$$I_D \approx c_{ox} W_g v_{exit} (V_{gs} - V_{th} - \Delta V) \text{ for } (V_{gs} - V_{th}) / \Delta V >> 1$$

where $\Delta V = v_{exit} L_g / \mu$

Exponential, Square-Law, Linear FET Characteristics



Relevance of DC Parameters

Digital circuit speed largely controlled by on-state current

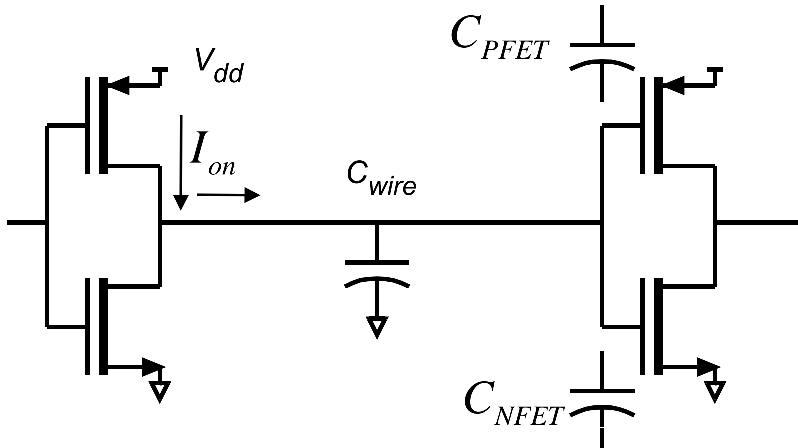
Standby power consumption controlled by off-state current

Dynamic power consumption controlled by supply Voltage

→ *Examine VLSI Power & Delay Relationships*

Zeroth-Order VLSI Performance Analysis

CMOS Power Dissipation & Gate Delay



Gate delay

$$\tau_{gate} \approx C_{total} V_{dd} / 2I_{on} = (C_{wire} + C_{NFET} + C_{PFET}) V_{dd} / 2I_{on}$$

wiring capacitance usually dominates

Dynamic dower dissipation :

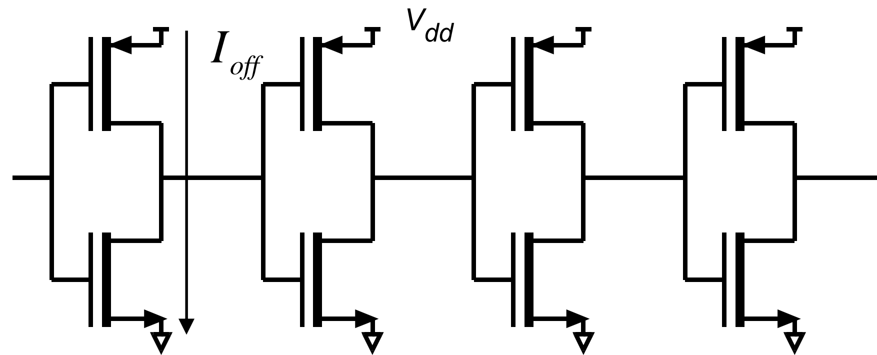
$$P_{dynamic} = \frac{C_{total} V_{dd}^2}{2} \cdot \text{frequency} \cdot (\text{switching probability})$$

Off state current

$$I_{off} / I_{on} > \exp(-qV_{th} / nkT)$$

Static Dissipation

$$P_{static} > I_{off} \cdot V_{dd}$$

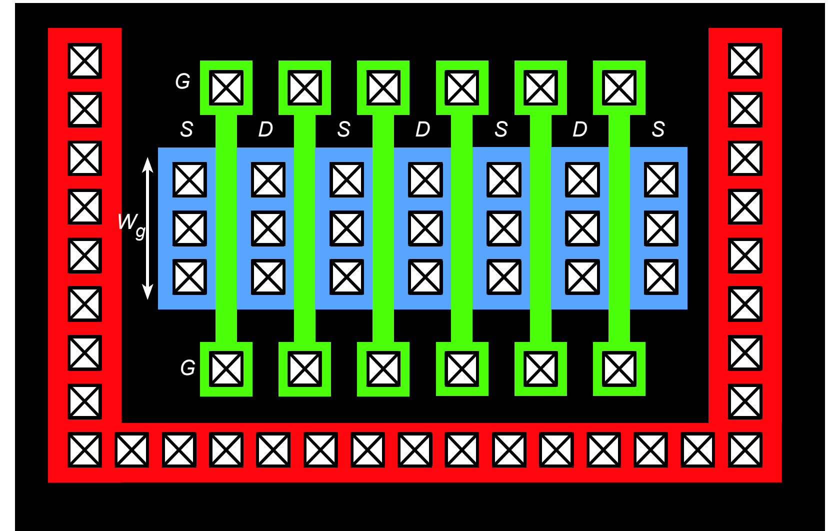


Tradeoff between static and dynamic dissipation : $P_{dynamic} \sim C_{wire} V_{dd}^2 f \cdot p \quad P_{static} \sim V_{dd} I_{on} e^{-qV_{th}/kT}$

Why Large Current Density is Needed

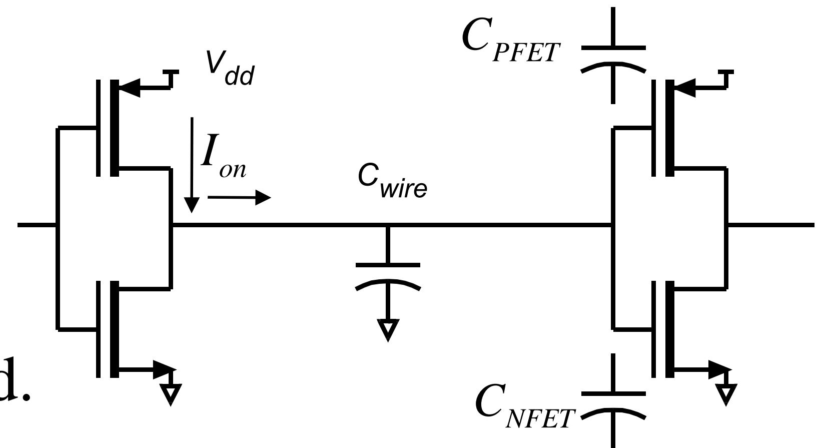
FET with $n = 6$ fingers,

each of width $W_g \rightarrow$ total width $= nW_g$



To drive C_{wire} at delay τ,

requires current $I_d = C_{wire} V_{dd} / 2\tau$.



If I_d / W_g is small, large FETs are needed.

Large FETs $\rightarrow$ long wires $\rightarrow$ large C_{wire}.

Device Requirements

High on-state current per unit gate width

Low off-state current→ subthreshold slope

Low device capacitance;
but only to point where wires dominate

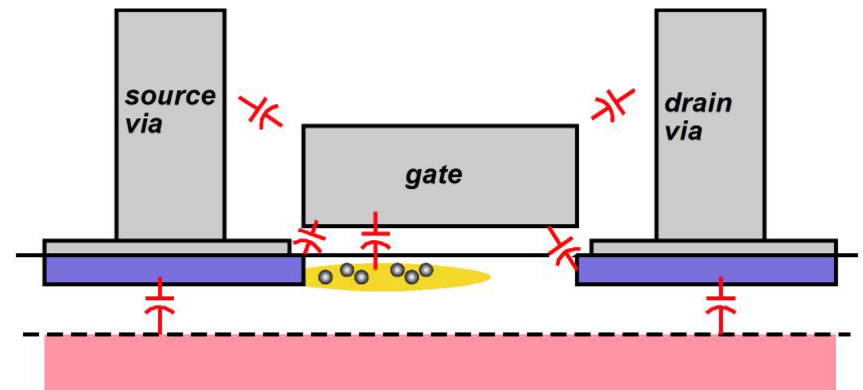
Low supply voltage: probably 0.5 to 0.7 V

What Are Our Goals ?

Low off-state current (10 nA/μm) for low static dissipation
→ good subthreshold slope → minimum L_g / T_{ox}
low gate tunneling, low band-band tunneling

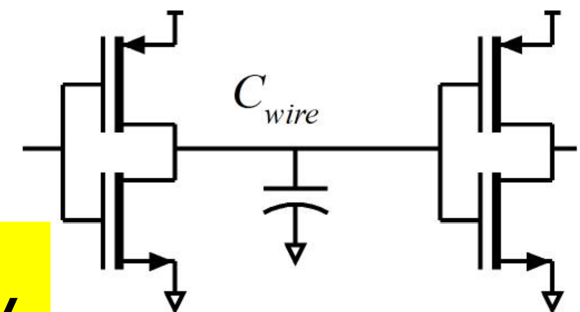
Low delay C_{FET} $\Delta V/I_d$ in gates where transistor capacitances dominate.

~1 fF/μm parasitic capacitances
→ low C_{gs} is desirable,
but high I_d is imperative



Low delay C_{wire} $\Delta V/I_d$ in gates where wiring capacitances dominate.

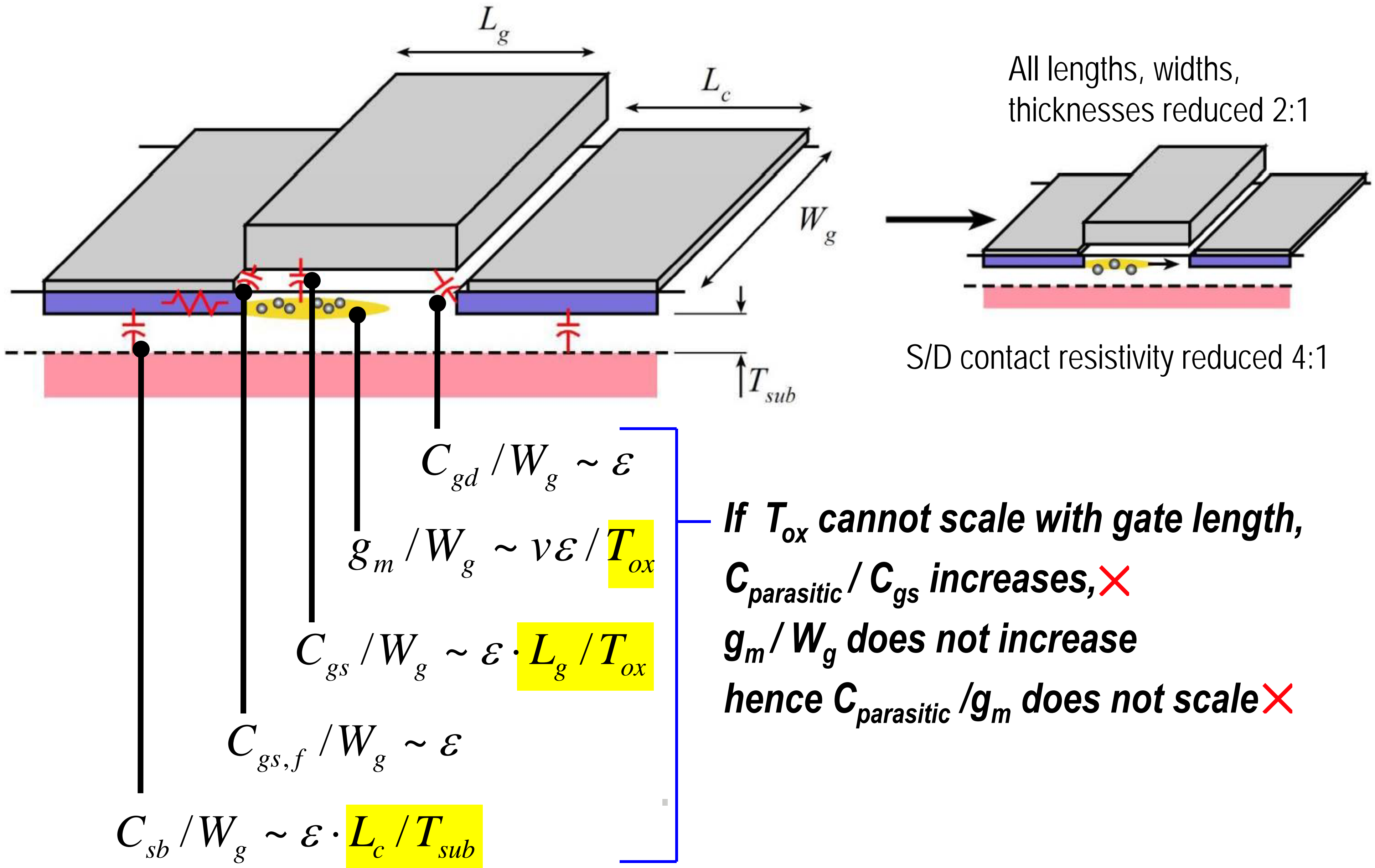
large FET footprint → long wires between gates
→ need high I_d / W_g ; target ~5 mA/μm @ ΔV= 0.7V
target ~ 3 mA/μm @ ΔV= 0.5V



Improving FETs
by Scaling

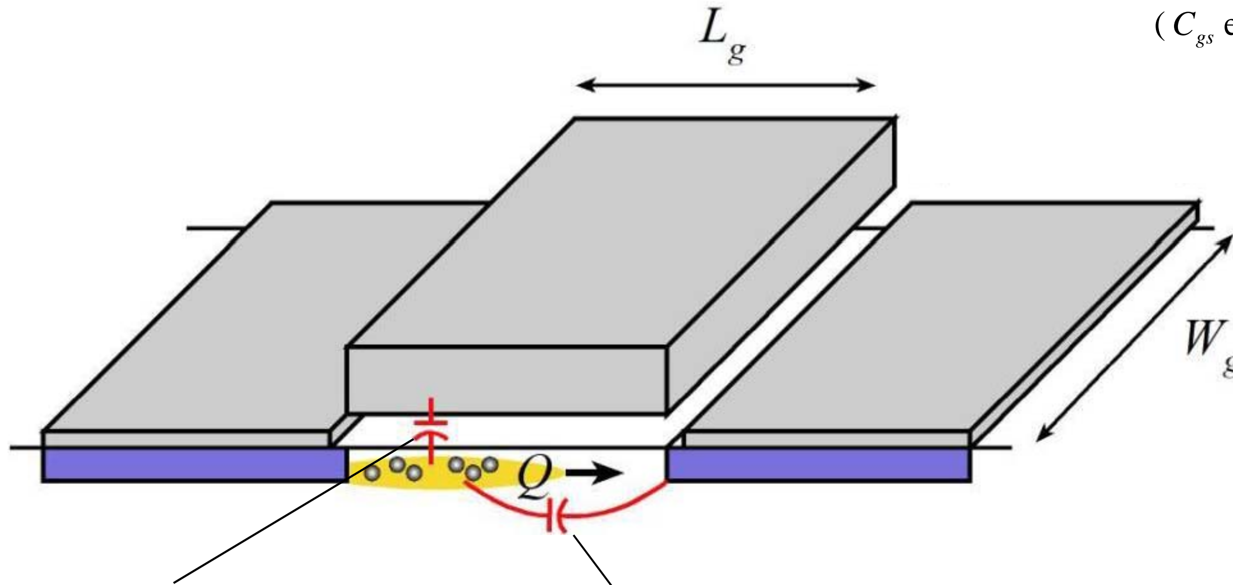
Simple FET Scaling

Goal double transistor bandwidth when used in any circuit
→ reduce 2:1 all capacitances and all transport delays
→ keep constant all resistances, voltages, currents



FET scaling: Output Conductance & DIBL

(C_{gs} expression neglects D.O.S. effects)



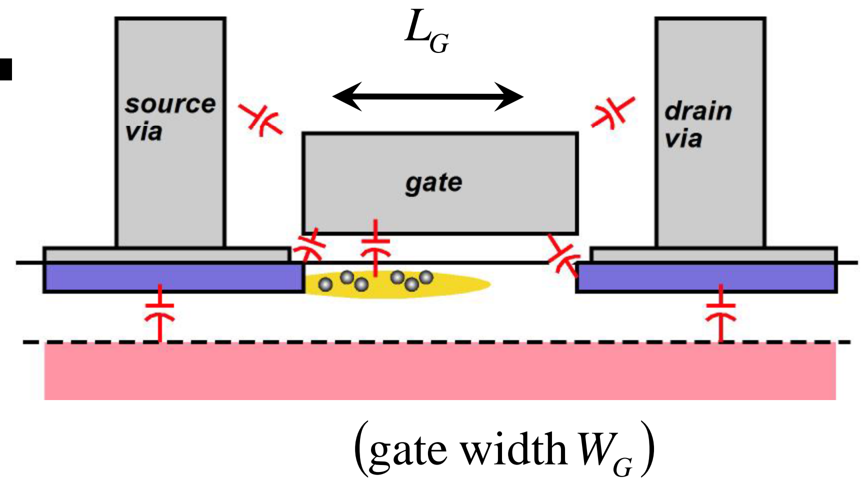
$$C_{gs} \sim \varepsilon W_g L_g / T_{ox} \qquad C_{d-ch} \sim \varepsilon W_g$$

$$I_d = Q / \tau \quad \text{where} \quad \delta Q = C_{gs}\delta V_{gs} + C_{d-ch}\delta V_{ds}$$

transconductance (from $C_{gs}\delta V_{gs}$) *output conductance* (from $C_{d-ch}\delta V_{ds}$)

→ ***Keep L_g / T_{ox} constant as we scale L_g***

FET Scaling Laws



Changes required to double transistor bandwidth:

parameter	change
gate length	decrease 2:1
gate dielectric capacitance density	increase 2:1
gate dielectric equivalent thickness	decrease 2:1
channel electron density	increase 2:1
source & drain contact resistance	decrease 4:1
current density (mA/μm)	increase 2:1

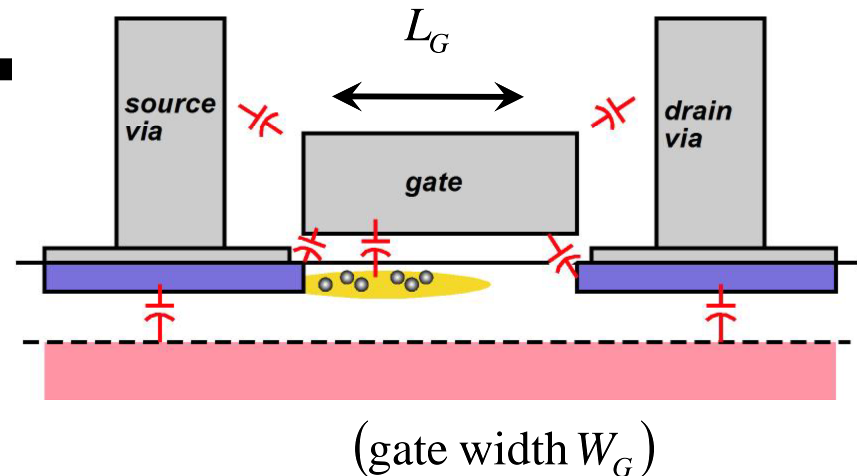
nm Transistors: it's all about the interfaces

Metal-semiconductor interfaces (Ohmic contacts):
<u>very low resistivity</u>

Dielectric-semiconductor interfaces (Gate dielectrics):
<u>very high capacitance density</u>

Transistor & IC thermal resistivity.

FET Scaling Laws



(gate width W_G)

Changes required to double transistor bandwidth:

parameter	change
gate length	decrease 2:1
gate dielectric capacitance density	increase 2:1
gate dielectric equivalent thickness	decrease 2:1
channel electron density	increase 2:1
source & drain contact resistance	decrease 4:1
current density (mA/μm)	increase 2:1

What do we do if gate dielectric cannot be further scaled ?

Why Consider MOSFETs with III-V Channels ?

If FETs cannot be further scaled,
instead increase electron velocity:

$$I_d / W_g = qn_s v \qquad I_d / Q_{transit} = v / L_g$$

III-V materials → lower m* → higher velocity
(need > 1000 cm^2/V-s mobility)

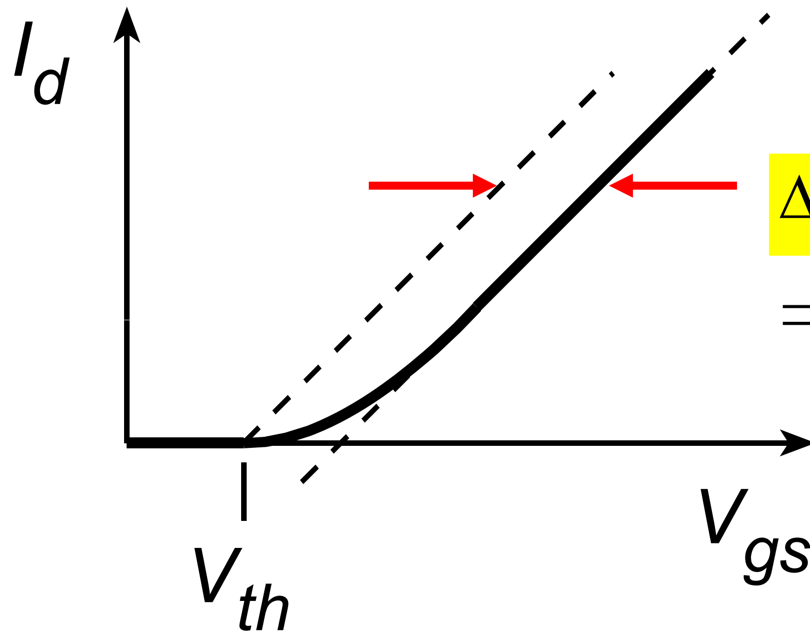
Candidate materials (?) $In_xGa_{1-x}As$, InP, InAs (InSb, GaAs)

Difficulties:
- High-K dielectrics
- III-V growth on Si
- building MOSFETs
- low m* constrains vertical scaling, reduces drive current

III-V CMOS: The Benefit Is Low Mass, Not High Mobility

Simple drift - diffusion theory, nondegenerate, far above threshold :

$I_D \approx c_{ox} W_g v_{injection} (V_{gs} - V_{th} - \Delta V)$ where $v_{injection} \sim v_{thermal} = (kT / m^*)^{1/2}$



$\Delta V = v_{injection} L_g / \mu$

$\Rightarrow$ Ensure that $\Delta V << (V_{gs} - V_{th})$

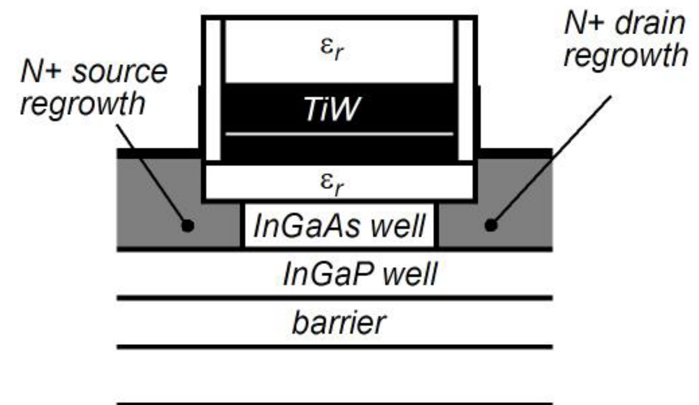
~ 700 mV

low effective mass → high currents

mobilities above ~ 1000 cm²/V-s of little benefit at 22 nm Lg

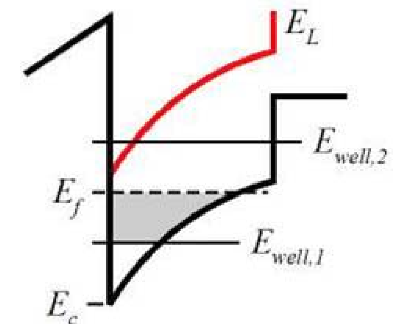
III-V MOSFETs for VLSI

What is it ?
MOSFET with an InGaAs channel



Why do it ?
low electron effective mass→ higher electron velocity
more current, less charge at a given insulator thickness & gate length
very low access resistance

What are the problems ?
low electron effective mass→ constraints on scaling !
must grow high-K on InGaAs, must grow InGaAs on Si



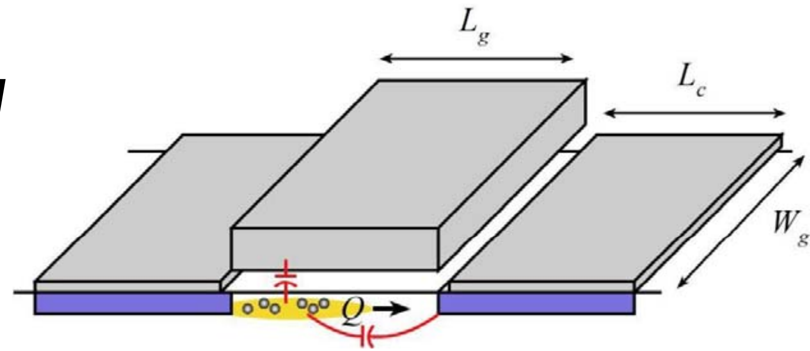
Device characteristics must be considered in more detail

III-V MOSFET

Characteristics

Low Effective Mass Impairs Vertical Scaling

Shallow electron distribution needed for high g_m / G_{ds} ratio, low drain-induced barrier lowering.



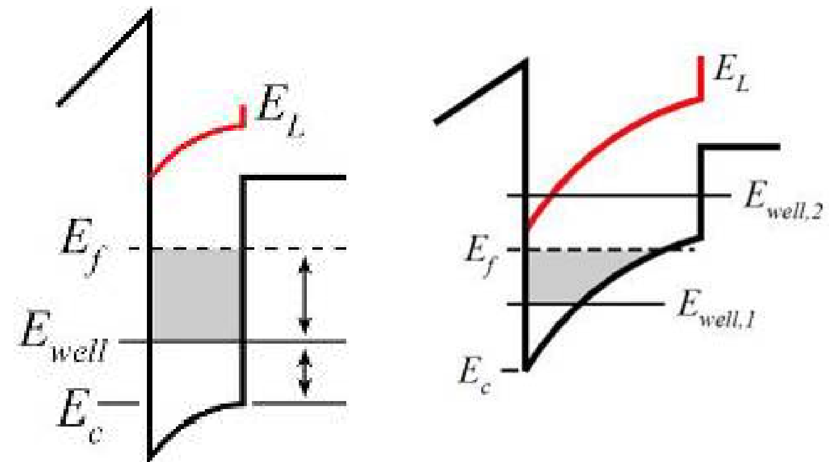
Energy of Lth well state $\propto L^2 / m^* T_{well}^2$.

For thin wells,

only 1st state can be populated.

For very thin wells,

1st state approaches L-valley.

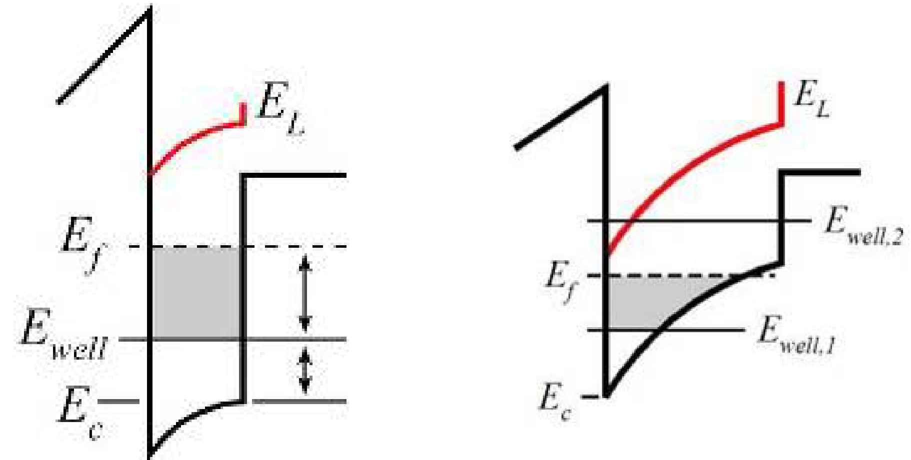


Only one vertical state in well.
Minimum ~ 5 nm well thickness.
→ Hard to scale below 22 nm L_g.

Semiconductor (Wavefunction Depth) Capacitance

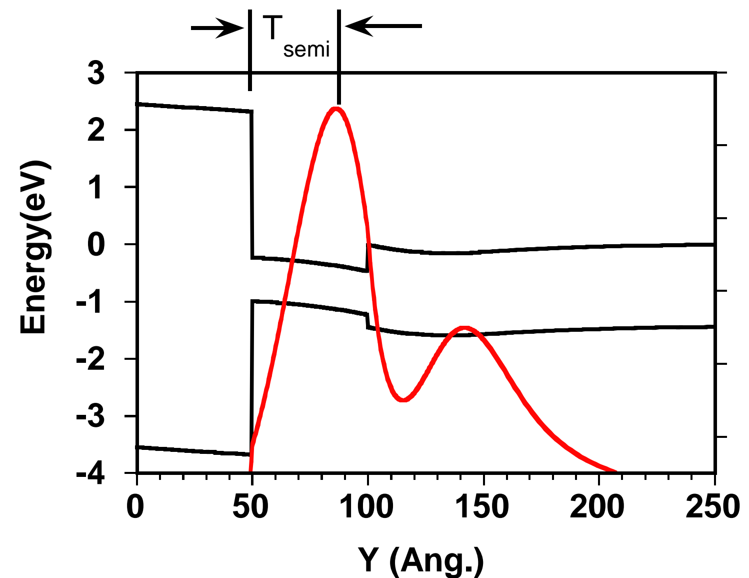
Bound state energy

$$E_{well} \propto L^2 / m^* T_{well}^2.$$



Semiconductor capacitance

$$c_{\text{semiconductor}} = \varepsilon / T_{semi}$$



Density-Of-States Capacitance

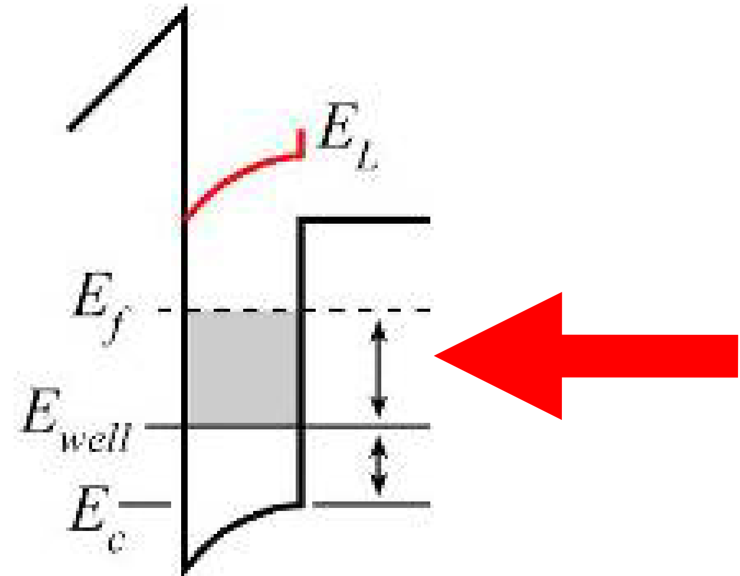
$$E_f - E_{well} = n_s / (nm^* / \pi\hbar^2)$$

(bidirectional motion)

$$V_f - V_{well} = \rho_s / c_{dos}$$

where $c_{dos} = q^2 nm^* / \pi\hbar^2$

and n is the # of band minima



Two implications:

- With N_s >$10^{13}/cm^2$, electrons populate satellite valleys

Fischetti et al, IEDM2007

- Transconductance dominated by finite state density

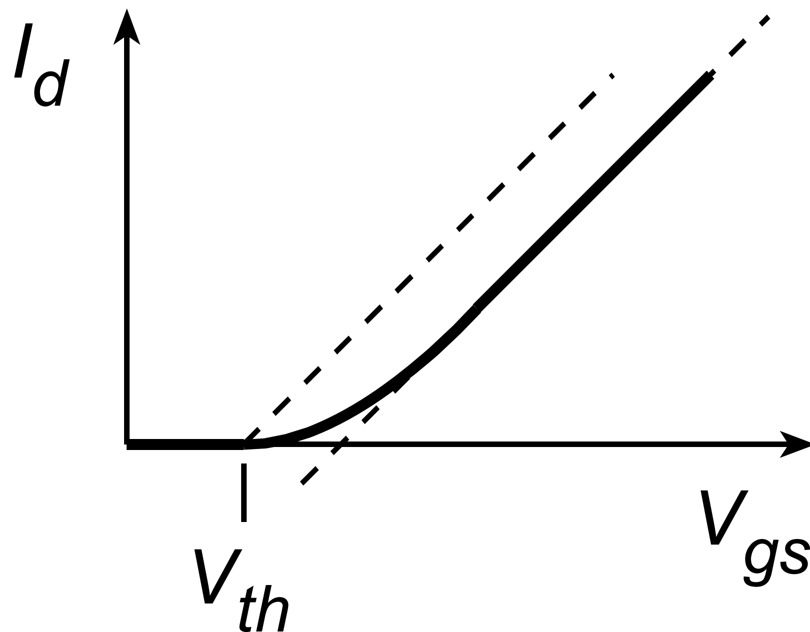
Solomon & Laux , IEDM2001

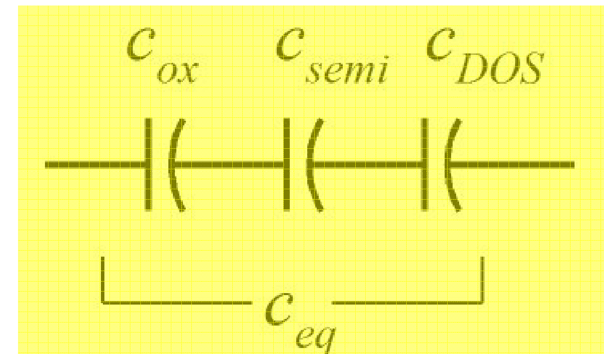
Current Including Density of States, Wavefunction Depth

Simple drift - diffusion theory, nondegenerate, far above threshold :

$$I_D \approx c_{eq} W_g v_{thermal} (V_{gs} - V_{th} - \Delta V)$$

where $1/c_{eq} = 1/c_{ox} + 1/c_{\text{semiconductor}} + 1/c_{DOS}$





...but with III-V materials,
we must also consider degenerate carrier concentrations.

Current of Degenerate & Ballistic FET

(Lundstrom, Natori, Laux, Solomon, Fischetti, Asbeck, ...)

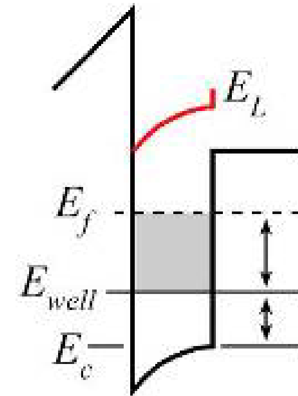
Density of states : $dN_s / dE_f = n \cdot m^* / 2\pi\hbar^2$ (unidirectional motion)

Highly degenerate :

electron density : $n_s = n \cdot (m^* / 2\pi\hbar^2)(E_f - E_c)$,

Fermi velocity : $v_f = \left(2(E_f - E_c) / m^*\right)^{1/2}$,

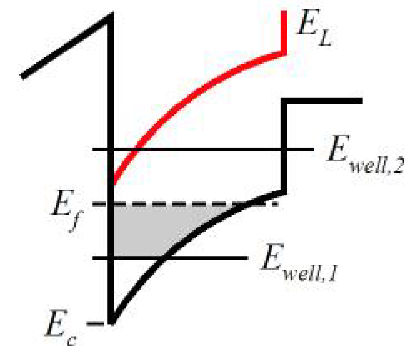
Mean electron velocity : $\bar{v} = (4 / 3\pi) v_f$.



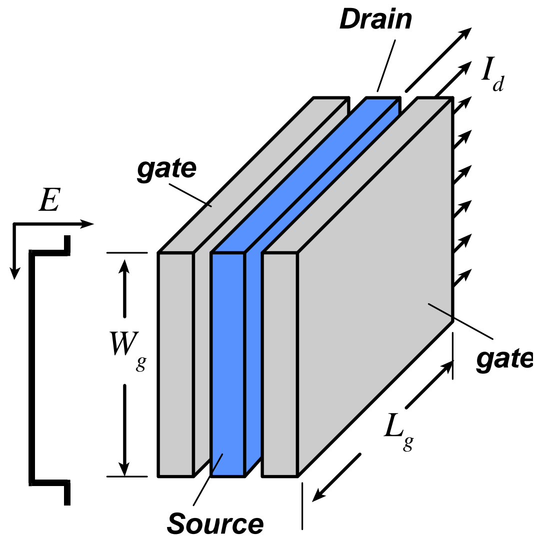
Current density :

$$J = qn_s\bar{v} = \left(\frac{2^{3/2}}{3\pi^2}\right)\frac{q^{5/2} n \cdot \left(m^*\right)^{1/2}\left((E_f - E_c)/q\right)^{3/2}}{\hbar^2}$$

$$= n \cdot \left(84\frac{\text{mA}}{\mu\text{m}}\right)\left(\frac{m^*}{m_0}\right)^{1/2}\left(\frac{E_f - E_c}{1\,\text{eV}}\right)^{3/2}$$



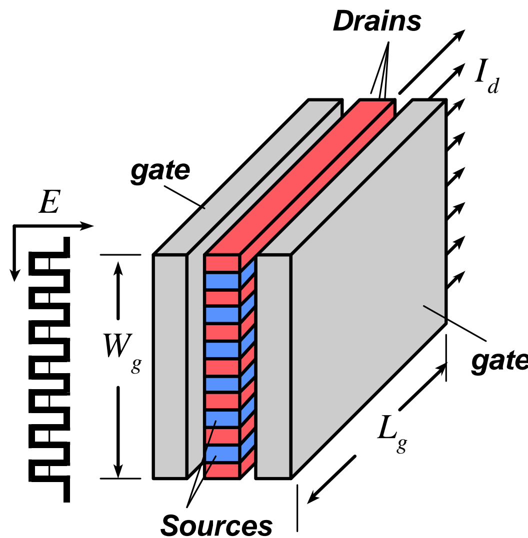
2D vs. 1D Field-Effect Transistors in Ballistic Limit



2D - FET; InGaAs channel ($m^*/m_0 = 0.04$)

$$J \cong \left(84\frac{\text{mA}}{\mu\text{m}}\right)\left(\frac{m^*}{m_0}\right)^{1/2}\left(\frac{E_f - E_c}{1\,\text{eV}}\right)^{3/2} = \left(17\frac{\text{mA}}{\mu\text{m}}\right)\left(\frac{E_f - E_c}{1\,\text{eV}}\right)^{3/2} = 2.8\frac{\text{mA}}{\mu\text{m}}$$

for 0.3 eV Fermi level shift in semiconductor.



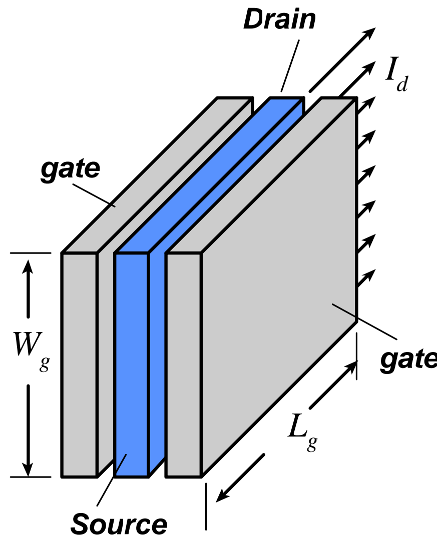
Array of 1D - FETs; 5 nm InGaAs wells @ 6 nm pitch

$$E_{well} = \frac{\hbar^2\pi^2}{2m^* T_{well}^2} = 0.37\,\text{eV}, \quad g_{m,well} = 2q^2/h = 78\,\mu\text{S}$$

$$J = \left(\frac{78\,\mu\text{A}}{6\,\text{nm}}\right)\left(\frac{E_f - E_c}{1\,\text{eV}}\right) = \left(13\frac{\text{mA}}{\mu\text{m}}\right)\left(\frac{E_f - E_c}{1\,\text{eV}}\right) = 3.9\frac{\text{mA}}{\mu\text{m}}$$

for 0.3 eV Fermi level shift in semiconductor

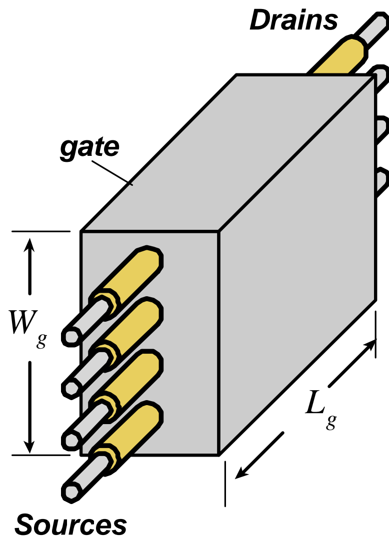
2D FET vs. Carbon Nanotube FET



2D - FET; InGaAs channel ($m^*/m_0 = 0.04$)

$$J \cong \left(17\,\frac{\text{mA}}{\mu\text{m}}\right)\left(\frac{E_f - E_c}{1\,\text{eV}}\right)^{3/2} = 2.8\,\frac{\text{mA}}{\mu\text{m}} \quad ,$$

for 0.3 eV Fermi level shift in semiconductor.



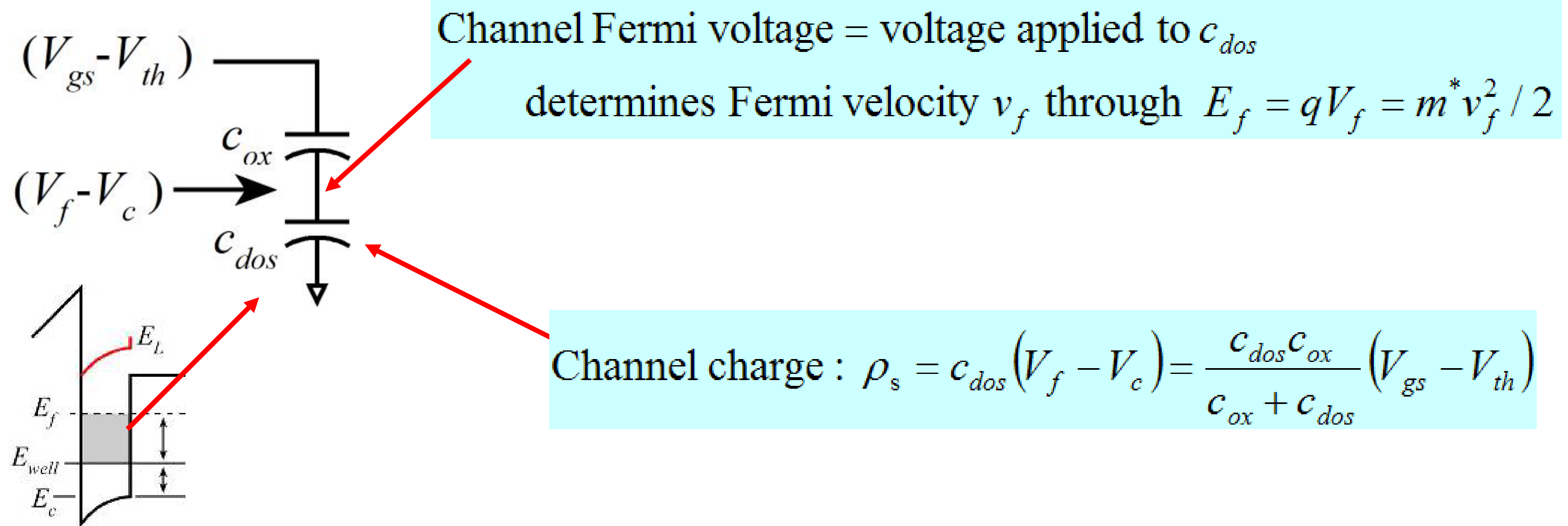
Array of carbon nanotubes, 5 nm pitch

$$g_{m,tube} = 2q^2/h = 78\,\mu\text{S}$$

$$J = \left(\frac{78\,\mu\text{A}}{5\,\text{nm}}\right)\left(\frac{E_f - E_c}{1\,\text{eV}}\right) = \left(15.5\,\frac{\text{mA}}{\mu\text{m}}\right)\left(\frac{E_f - E_c}{1\,\text{eV}}\right) = 4.7\,\frac{\text{mA}}{\mu\text{m}}$$

for 0.3 eV Fermi level shift in semiconductor

Ballistic/Degenerate Drive Current vs. Gate Voltage



$c_{dos} = q^2 n m^* / 2\pi\hbar^2 = c_{dos,o} \cdot n \cdot (m^* / m_o)$, where n is the # of band minima

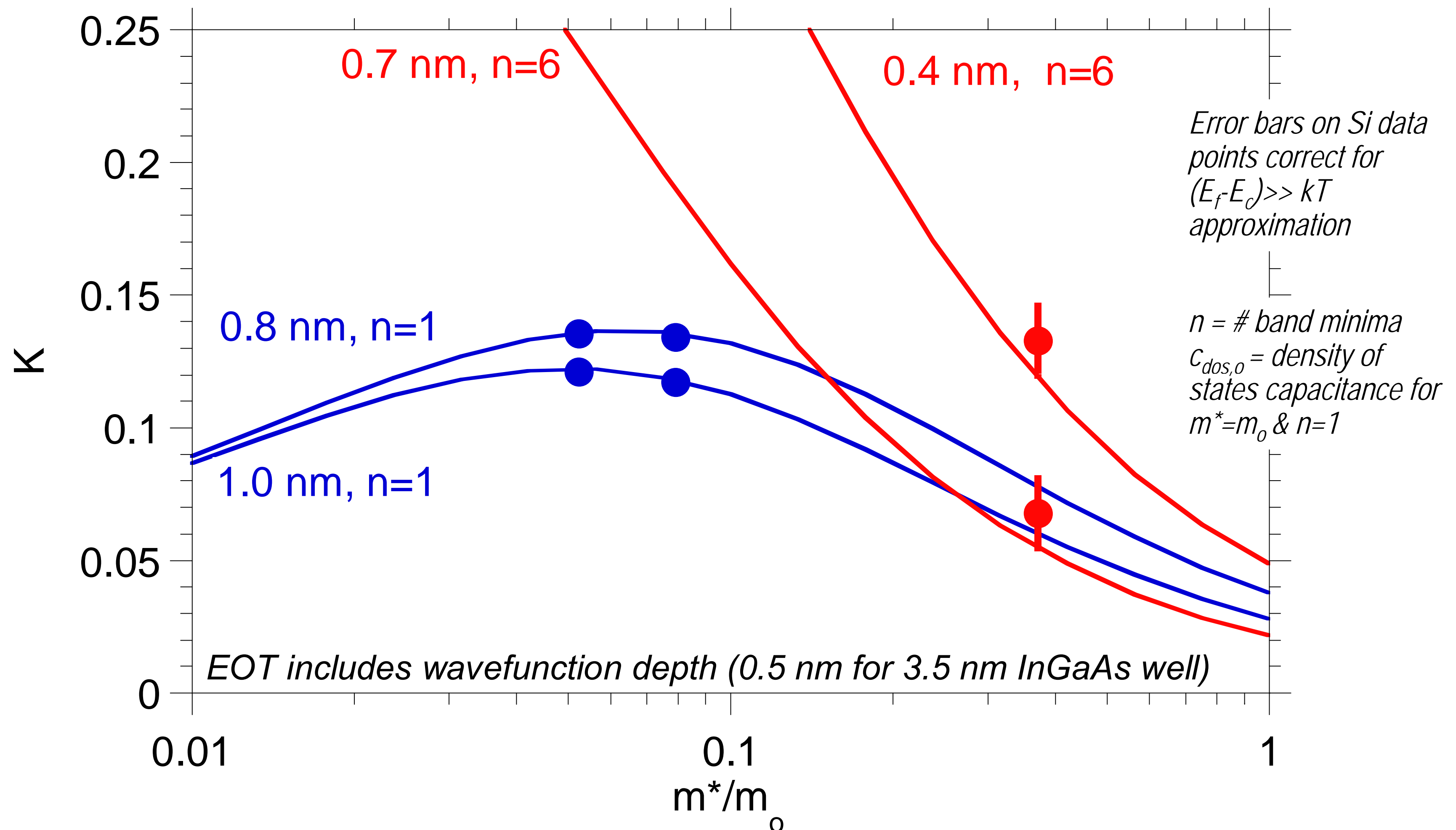
$$\Rightarrow \quad J = \left(84 \frac{\text{mA}}{\mu\text{m}}\right) \cdot \left(\frac{V_{gs} - V_{th}}{1\text{V}}\right)^{3/2} \cdot \frac{n \cdot \left(m^* / m_o\right)^{1/2}}{\left(1 + (c_{dos,o} / c_{ox}) \cdot n \cdot (m^* / m_o)\right)^{3/2}}$$

Ballistic but nondegenerate case : $J \approx \left(kT / m^*\right)^{1/2} c_{ox} \left(V_{gs} - V_{th}\right)$

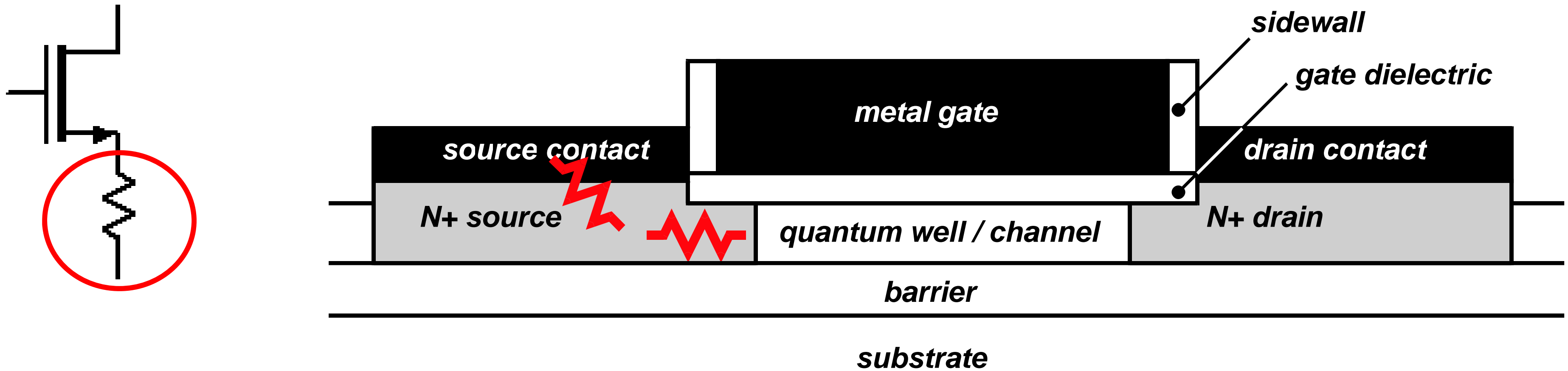
More careful analyses by Taur & Asbeck Groups, UCSD; Fischetti Group: U-Mass: IEDM2007

Drive Current in the Ballistic & Degenerate Limits

$$J = \underline{K} \cdot \left(84\,\frac{\text{mA}}{\mu\text{m}}\right) \cdot \left(\frac{V_{gs} - V_{th}}{1\,\text{V}}\right)^{3/2} \quad , \quad \text{where } \underline{K} = \frac{n \cdot \left(m^*/m_o\right)^{1/2}}{\left(1 + (c_{dos,o}/c_{ox}) \cdot n \cdot (m^*/m_o)\right)^{3/2}}$$



High Drive Current Requires Low Access Resistance



For < 10% impact on drive current,

$$I_D R_S / (V_{DD} - V_{th}) < 0.1$$

$$\text{Target } I_D / W_g \sim 1.5 \text{ mA}/\mu\text{m @ } (V_{DD} - V_{th}) = 0.3 \text{ V}$$

$$\text{Target } I_D / W_g \sim 3 \text{ mA}/\mu\text{m @ } (V_{DD} - V_{th}) = 0.5 \text{ V}$$

$$\rightarrow R_s W_g < 15 - 20\, \Omega - \mu\text{m}$$

Materials Selection;

What channel material should we use ?

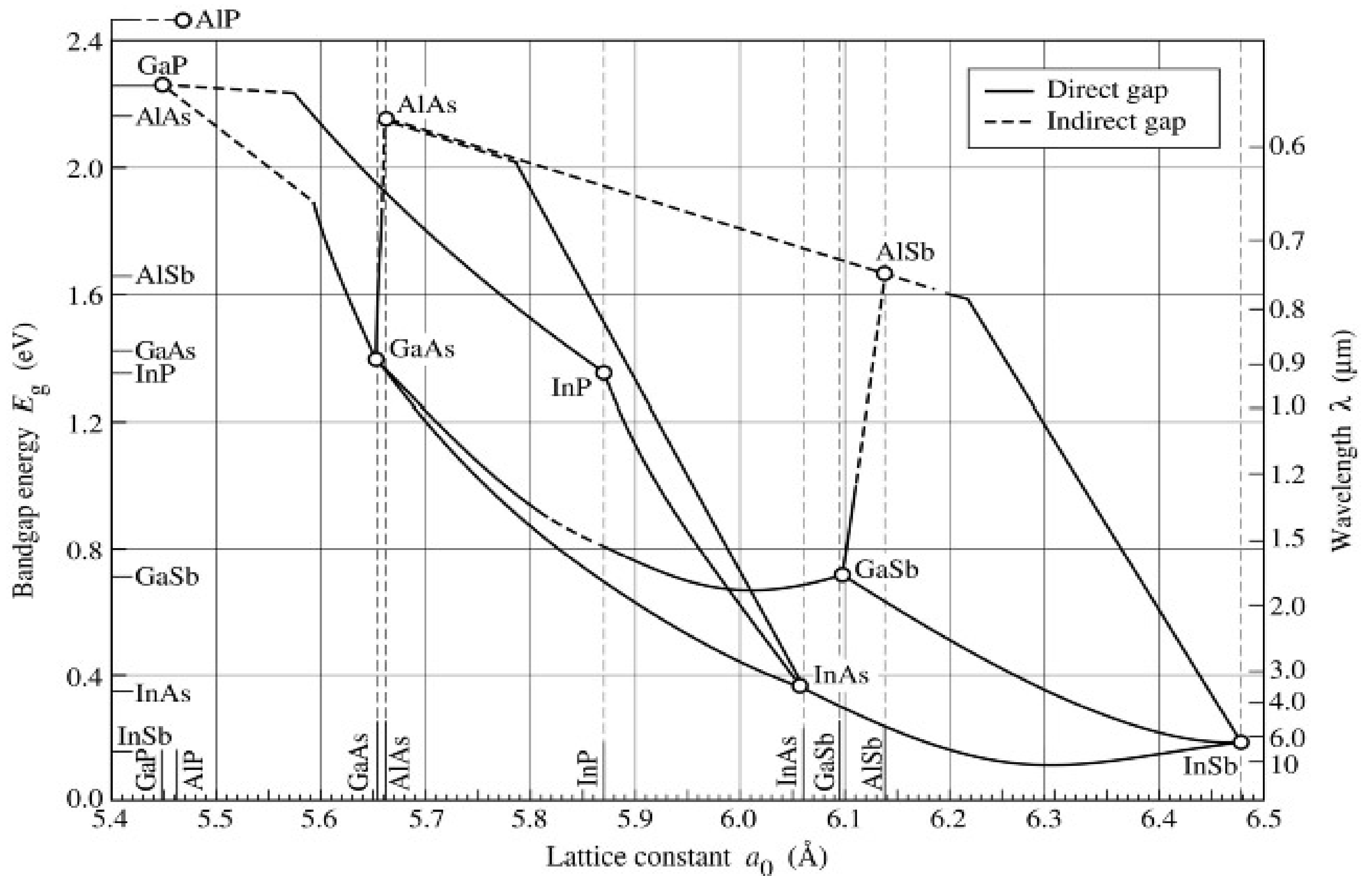
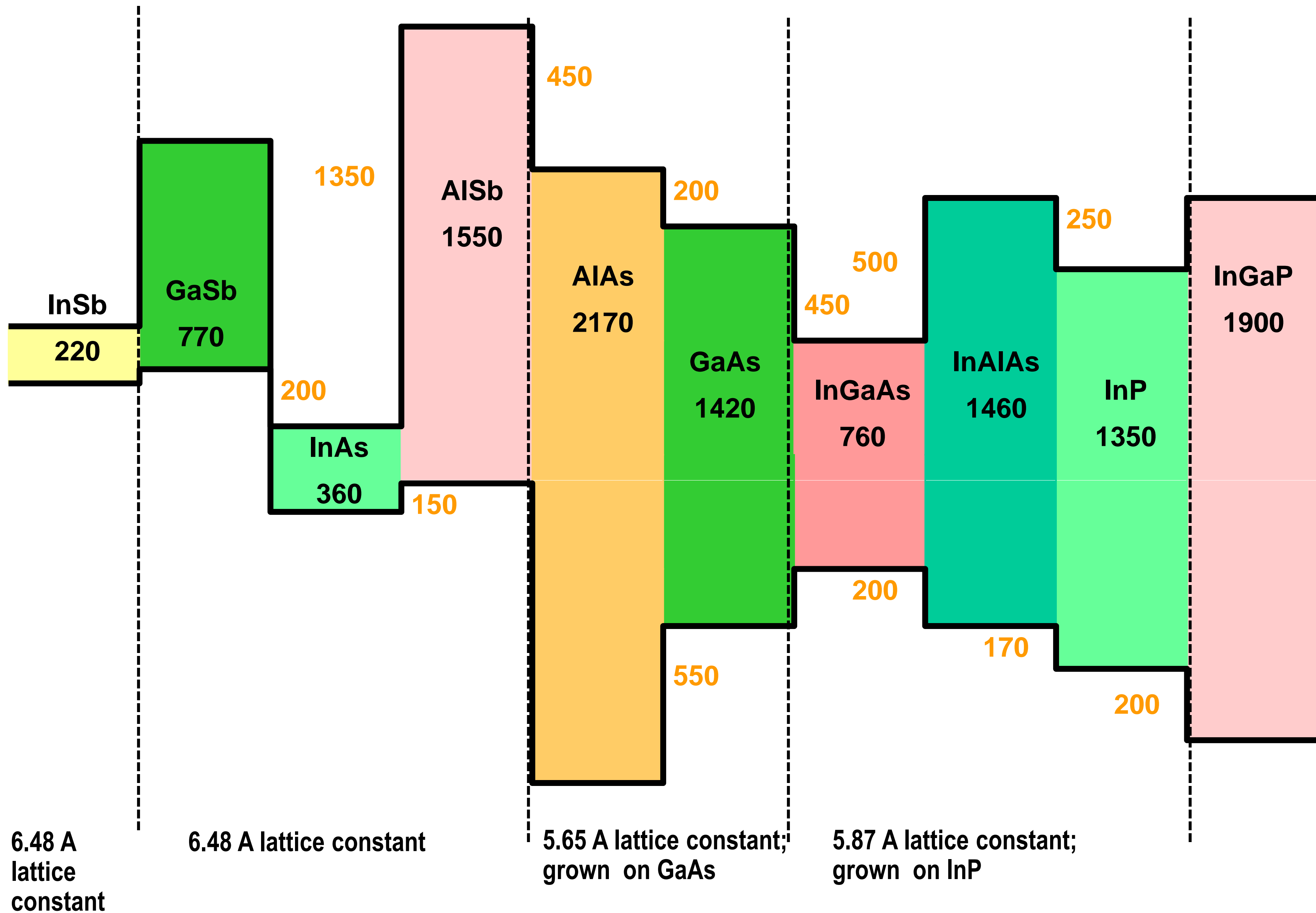


Fig. 7.6. Bandgap energy and lattice constant of various III-V semiconductors at room temperature (adopted from Tien, 1988).

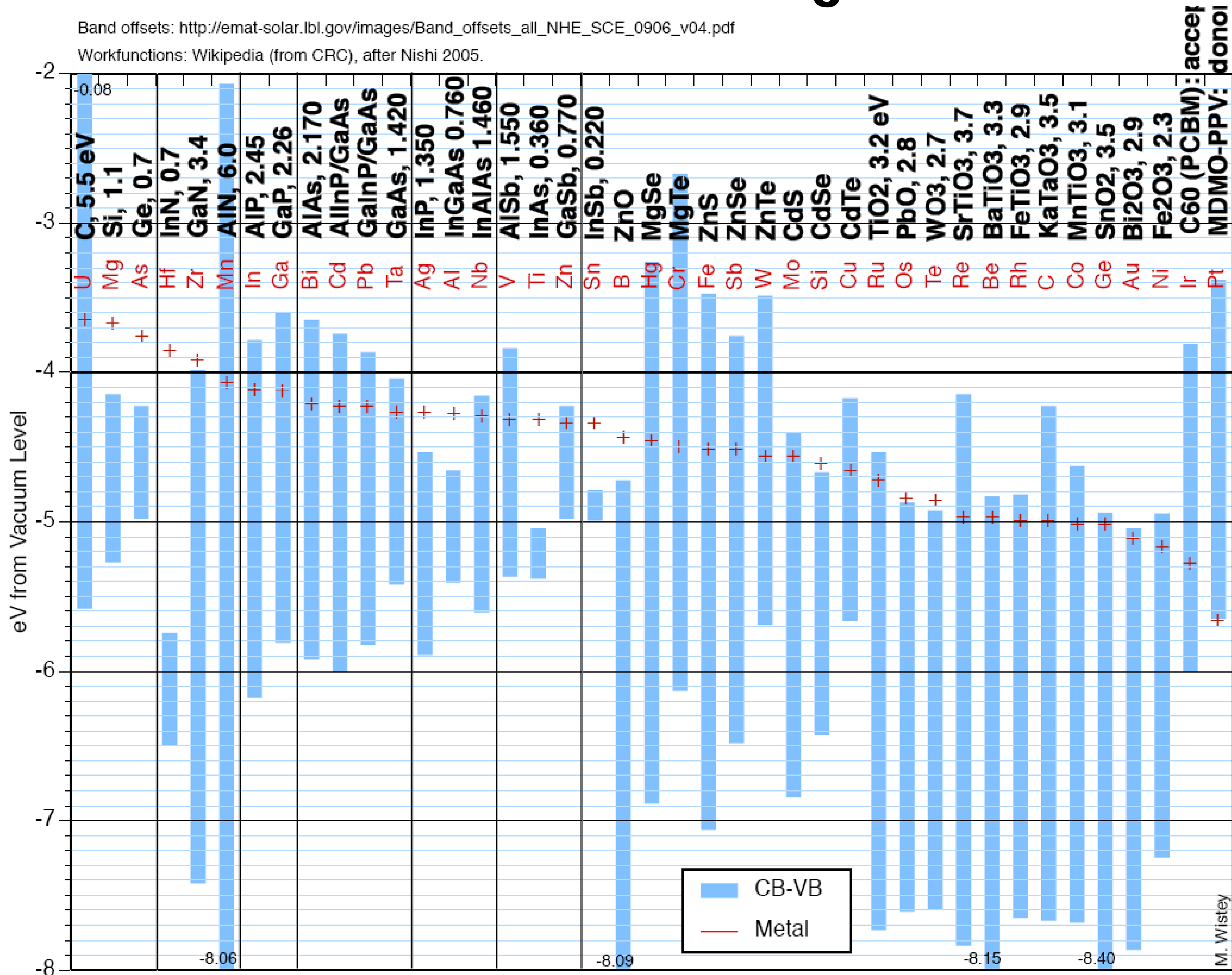
Common III-V Semiconductors

B. Brar



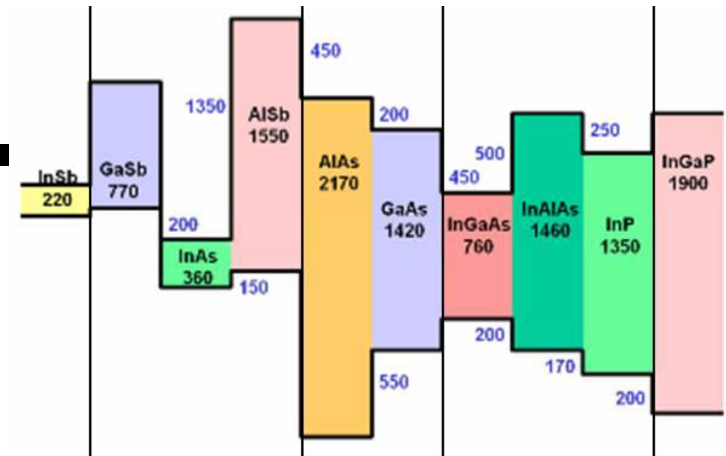
Semiconductor & Metal Band Alignments

M. Wistey



Materials of Interest

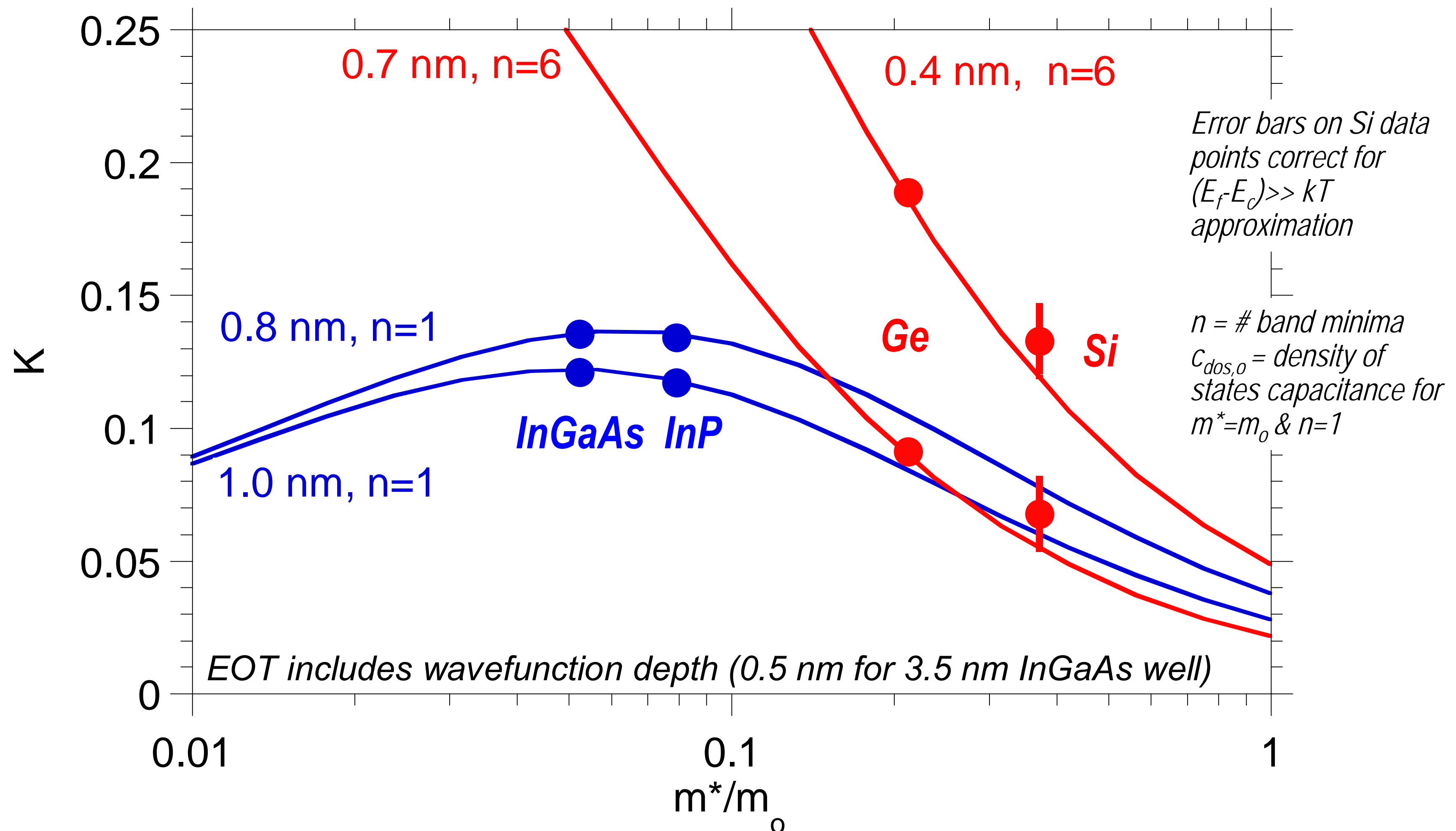
Source: Ioffe Institute
http://www.ioffe.rssi.ru/SVA/NSM/Semicond
rough #s only



material	Si	Ge	GaAs	InP	$In_{0.53}Ga_{0.47}As$	InAs
n	6	6	1	1	1	1
m*/m0	0.98 m_l 0.19 m_t	1.6 m_l 0.08 m_t	0.063	0.08	0.04	0.023
Γ-(L/X) separation, eV	--	--	0.29	~0.5	0.5	0.73
bandgap, eV	1.12	0.66	1.42	1.34	0.74	0.35
mobility, cm^2/V-s	1000	2000	5000	3000	10,000	25,000
high-field velocity	1E7	1E7	1-2E7	3.5E7	3.5E7	???

Drive Current in the Ballistic & Degenerate Limits

$$J = \underline{K} \cdot \left(84\frac{\text{mA}}{\mu\text{m}}\right) \cdot \left(\frac{V_{gs} - V_{th}}{1\,\text{V}}\right)^{3/2}, \quad \text{where } \underline{K} = \frac{n \cdot \left(m^*/m_o\right)^{1/2}}{\left(1 + (c_{dos,o}/c_{ox}) \cdot n \cdot (m^*/m_o)\right)^{3/2}}$$



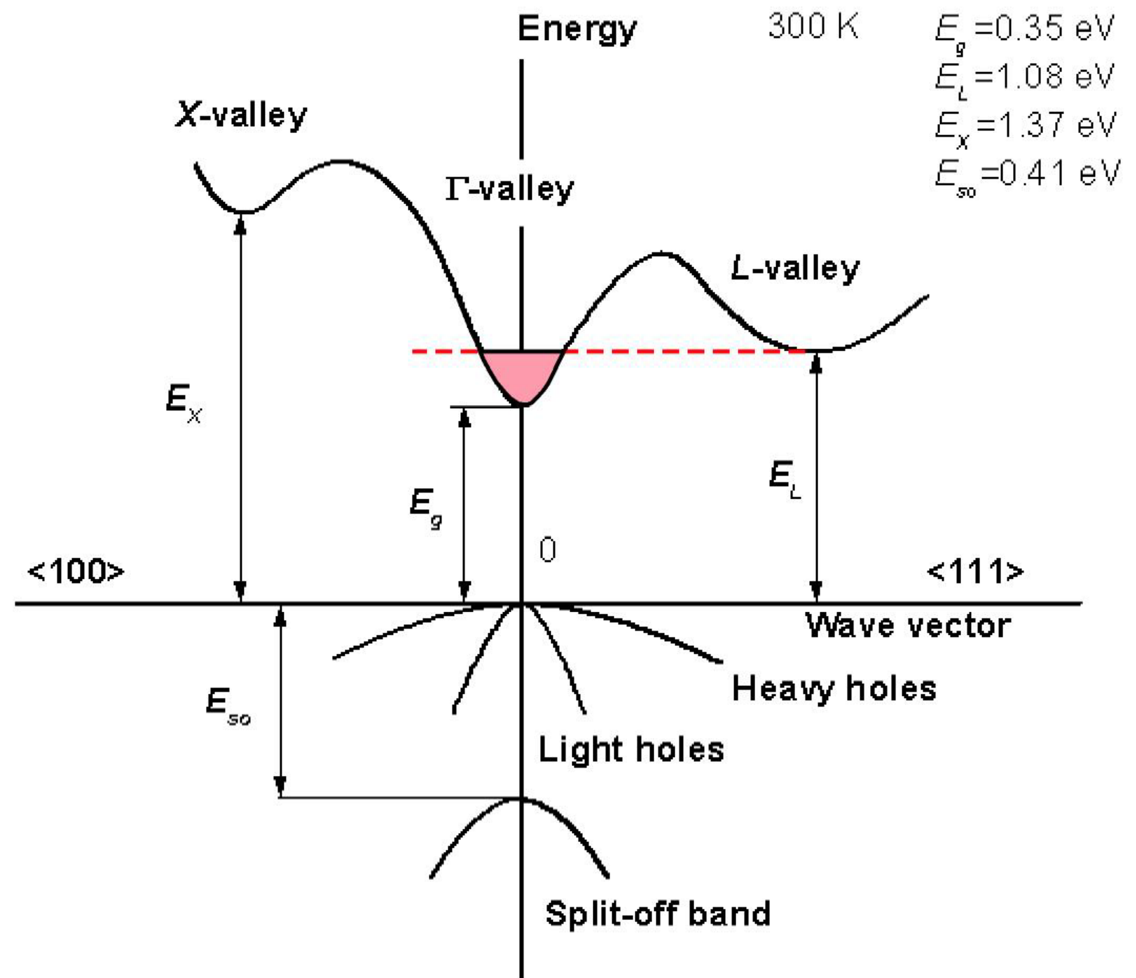
Intervalley Separation

Source: Ioffe Institute
http://www.ioffe.rssi.ru/SVA/NSM/Semicond

Intervalley separation sets:

-high-field velocity through intervalley scattering

-maximum electron density in channel without increased carrier effective mass



Choosing Channel Material: Other Considerations

Ge: *low bandgap*

GaAs: *low intervalley separation*

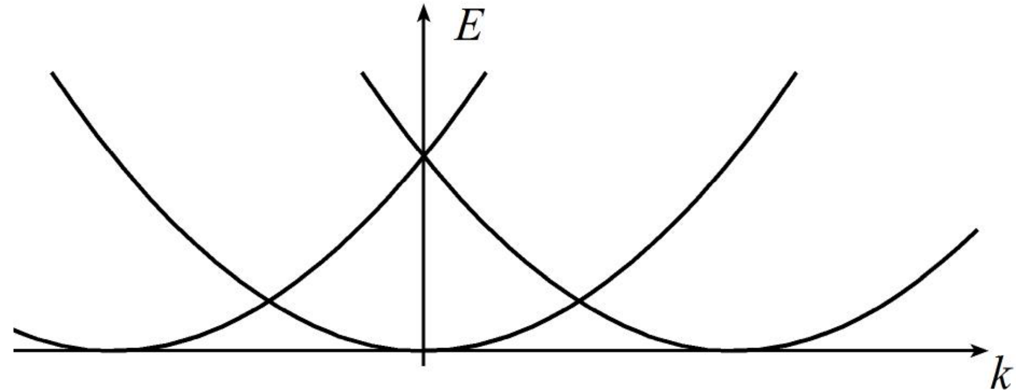
InP: *good intervalley separation*
Good contacts only via InGaAs→ band offsets
moderate mass→ better vertical scaling

InGaAs *good intervalley separation*
bandgap too low ? → quantization
low mass→ high well energy→ poor vertical scaling

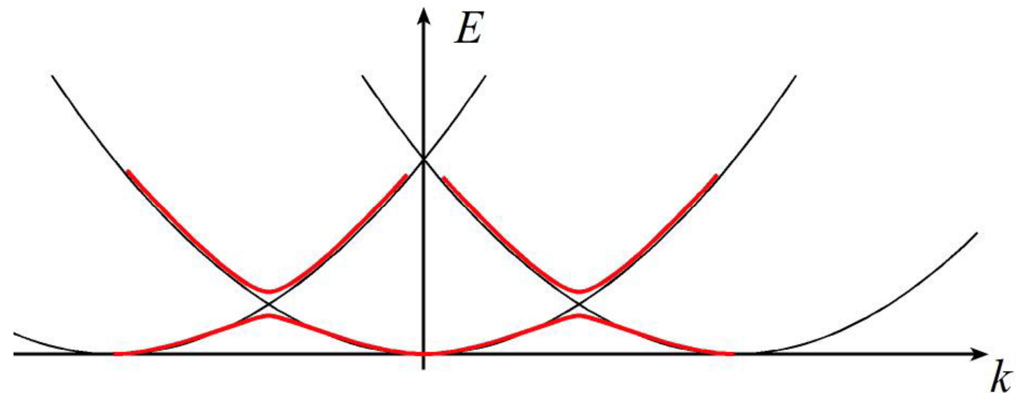
InAs: *good intervalley separation*
bandgap too low
very low mass→ high well energy→ poor vertical scaling

Non-Parabolic Bands

Bands are ~ parabolic only for k near zero.

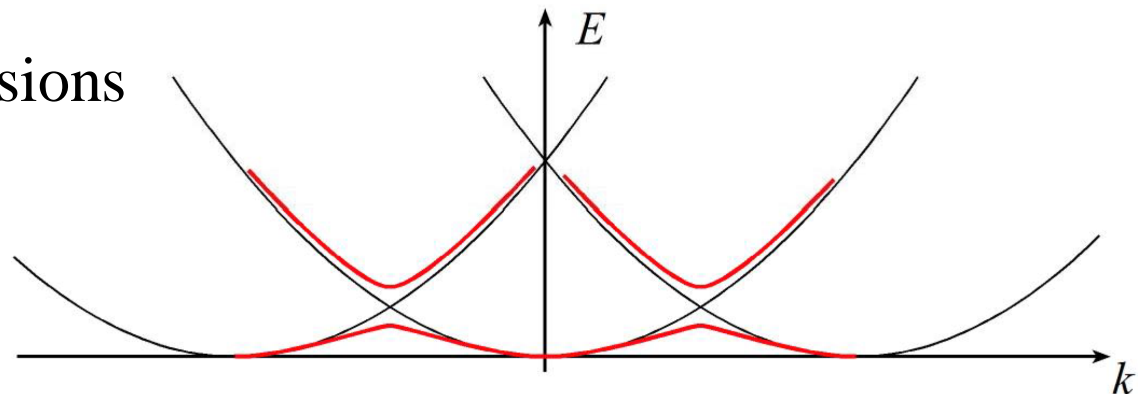


At high energies, bands become nearly hyperbolic.



$\rightarrow$ Asyptotic group velocity. Similar in most semiconductors.

Parabolic - band FET expressions are generally pessimistic.



Non-Parabolic Bands

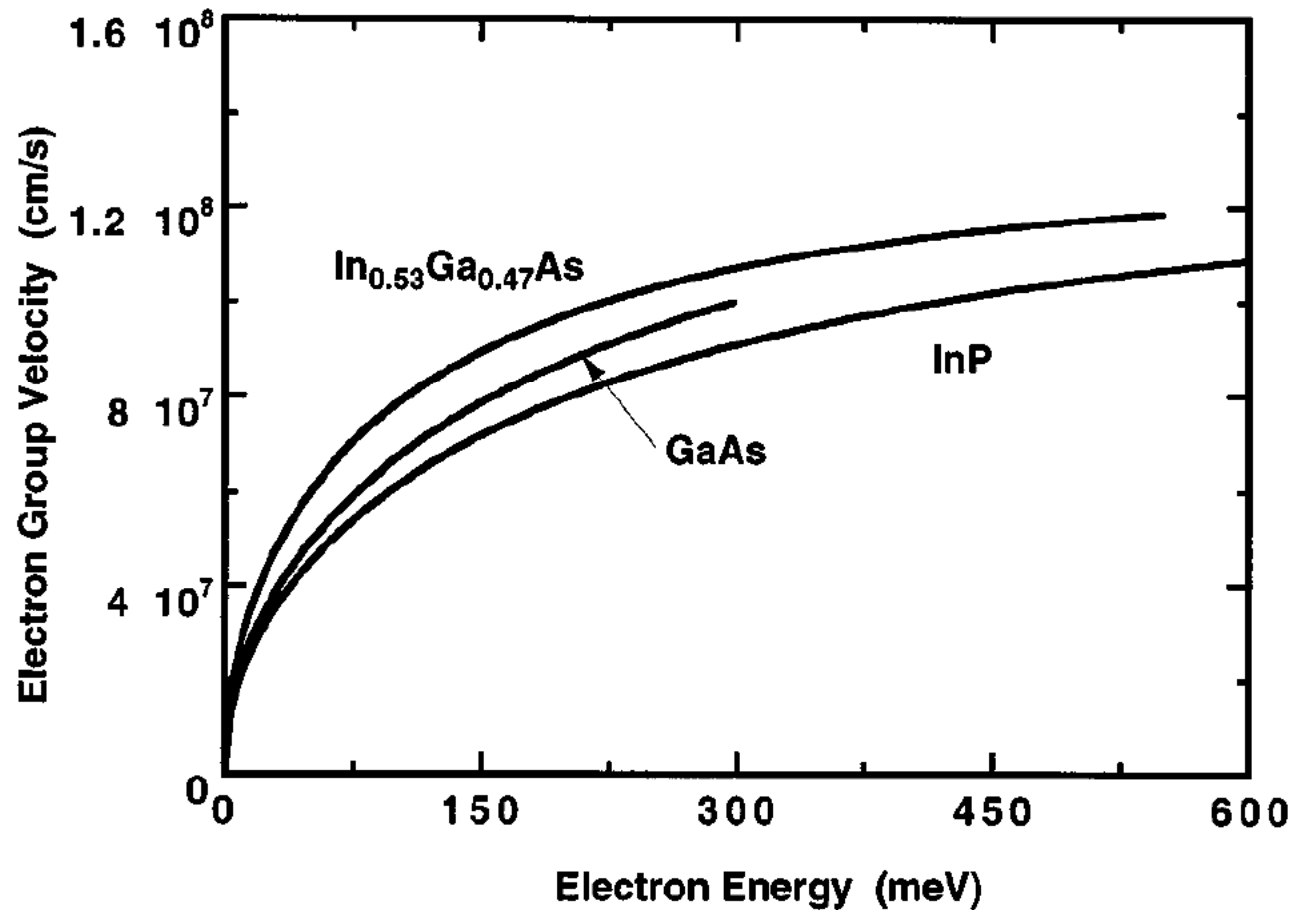
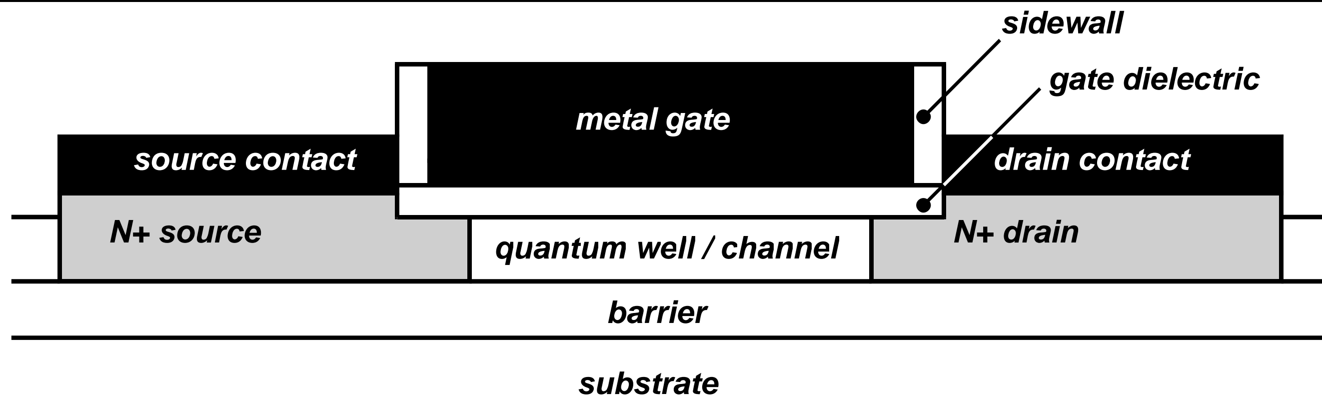


Fig. 1. Electron group velocities as a function of electron energy. In the calculation, nonparabolicity coefficients α used are 0.61, 0.63, and 1.22 for GaAs, InP, and $In_{0.53}Ga_{0.47}As$, respectively.

T. Ishibashi, IEEE Transactions on Electron Devices, 48,11 , Nov. 2001,

MOSFET Design Assuming $In_{0.5}Ga_{0.5}As$ Channel

Device Design / Fabrication Goals



Device

gate overdrive	700	500	300	mV
drive current	5	3	1.4	mA/μm
N_s	$6*10^{12}$	$4*10^{12}$	$2.5*10^{12}$	$1/cm^2$

Dielectric:

EOT 0.6 nm target, ~1.5 nm short term

Channel :

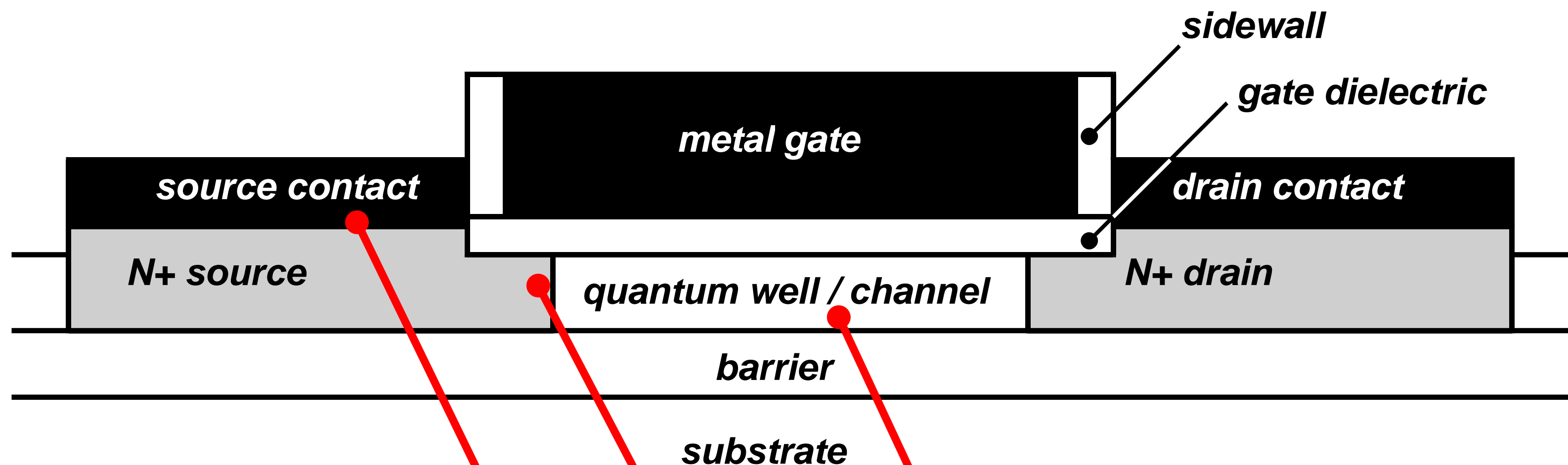
5 nm thick

$\mu > 1000\ cm^2/V\text{-}s$ @ 5 nm, $6*10^{12}\ /cm^2$

S/D access resistance:

20 Ω-μm resistivity→ 0.5 $\Omega\text{-}\mu m^2$ contacts , $\sim 2*10^{13}\ /cm^2$, $\sim 4*10^{19}\ /cm^3$, 5 nm depth

Target Device Parameters



well : $n_s \sim 5 \cdot 10^{12} \, / \mathrm{cm}^2, 5 \, \mathrm{nm} \;\; \mathrm{thick}$

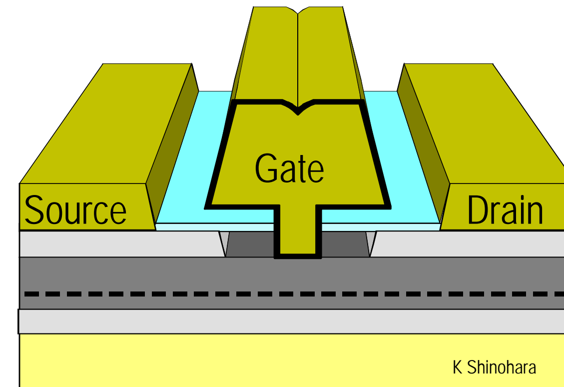
$5 \cdot 10^{19} \, / \mathrm{cm}^3 \, , 5 \, \mathrm{nm} \; \mathrm{thick} \rightarrow n_s = 2.5 \cdot 10^{13} \, / \mathrm{cm}^2$

$(0.25 \, \Omega - \mu\mathrm{m}^2) \, / (25 \, \mathrm{nm} \; \mathrm{wide} \; \mathrm{contact}) = 10 \, \Omega - \mu\mathrm{m}$

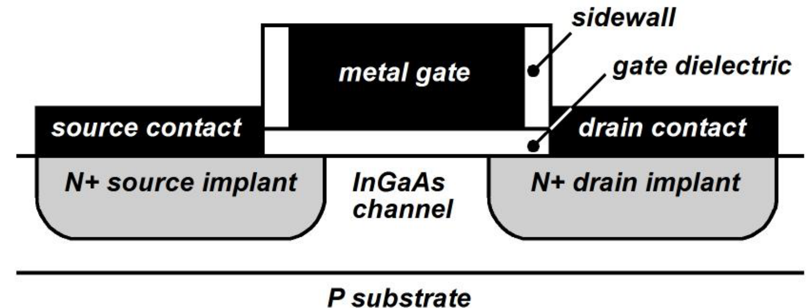
Device Structure
&
Process Flow

Device Fabrication: Goals & Challenges

III-V HEMTs are built like this→

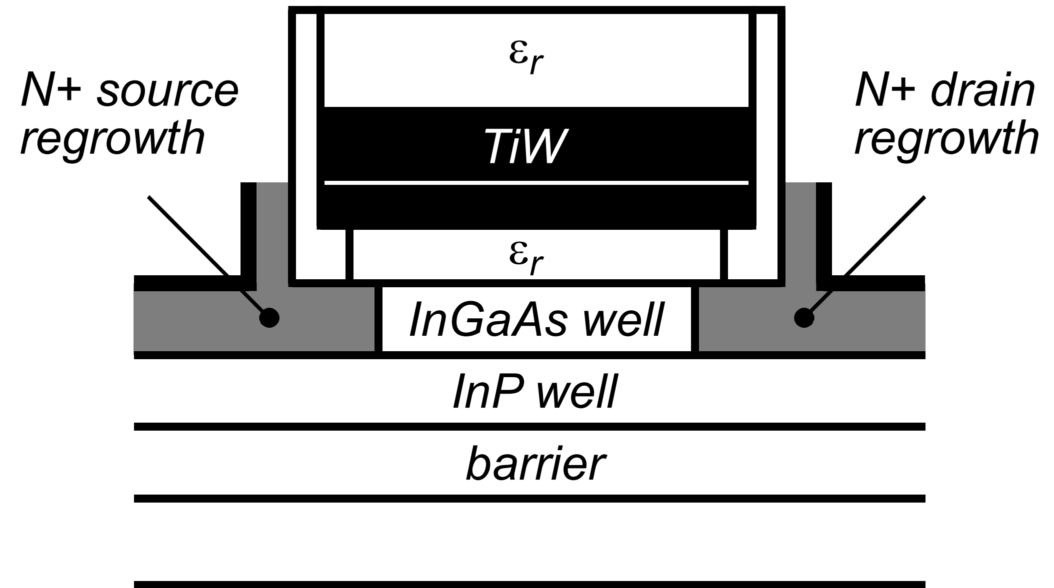


....and most
III-V MOSFETs are built like this→

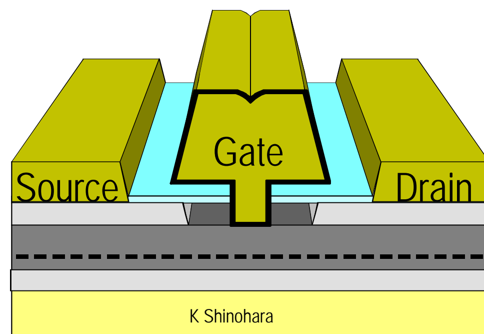


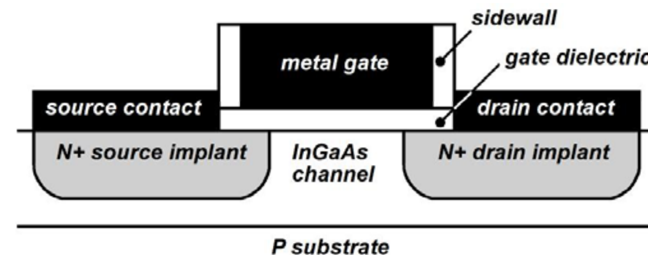
Device Fabrication: Goals & Challenges

Yet, we are developing,
at great effort,
a structure like this →



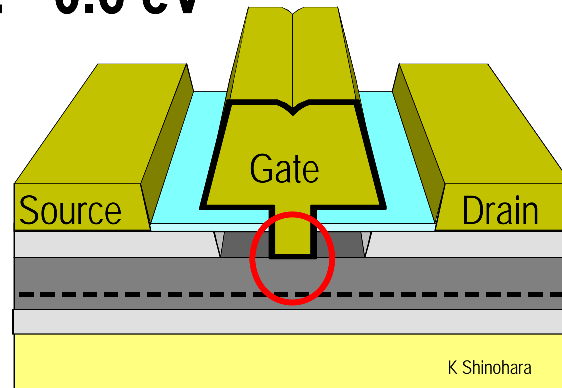
Why ?

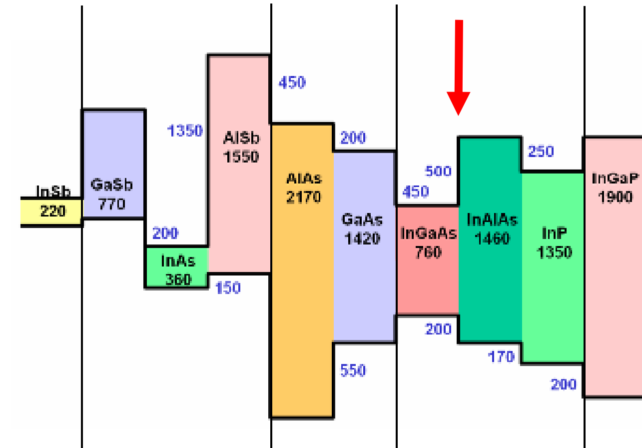




Why not just build HEMTs ? Gate Barrier is Low !

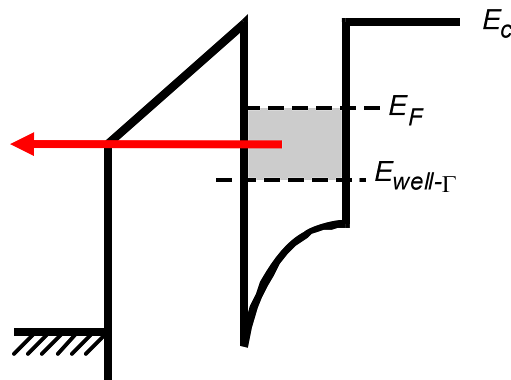
Gate barrier is low: ~0.6 eV

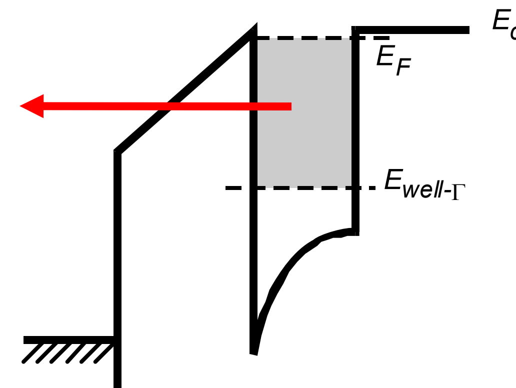




Tunneling through barrier
→ sets minimum thickness

Emission over barrier
→ limits 2D carrier density

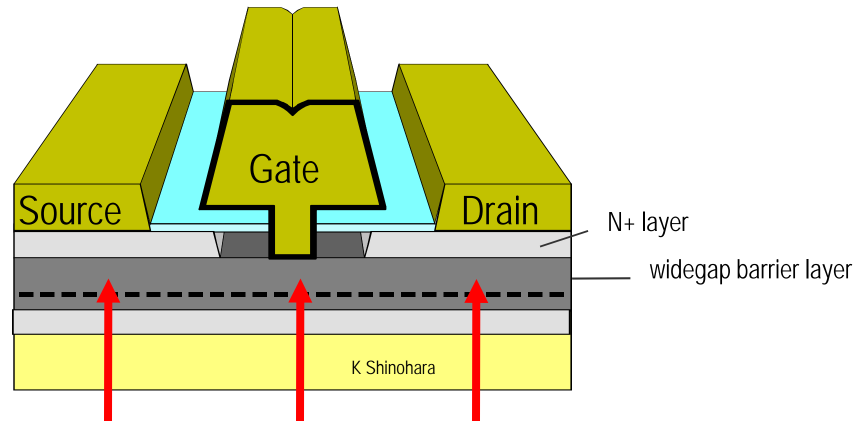




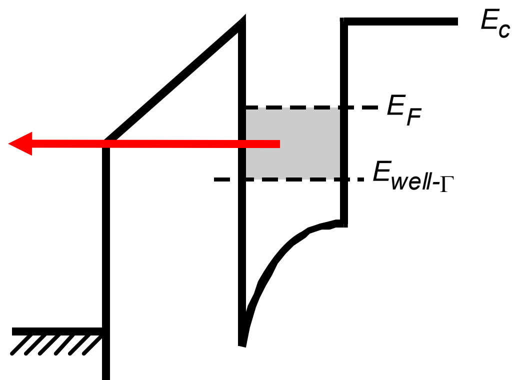
At $N_s = 10^{13}/\text{cm}^2, (E_f - E_c) \sim 0.6\,\text{eV}$

Why not just build HEMTs ?

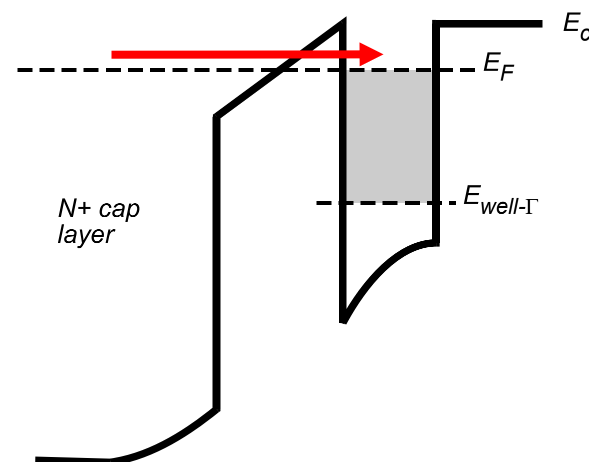
Gate barrier also lies under source / drain contacts



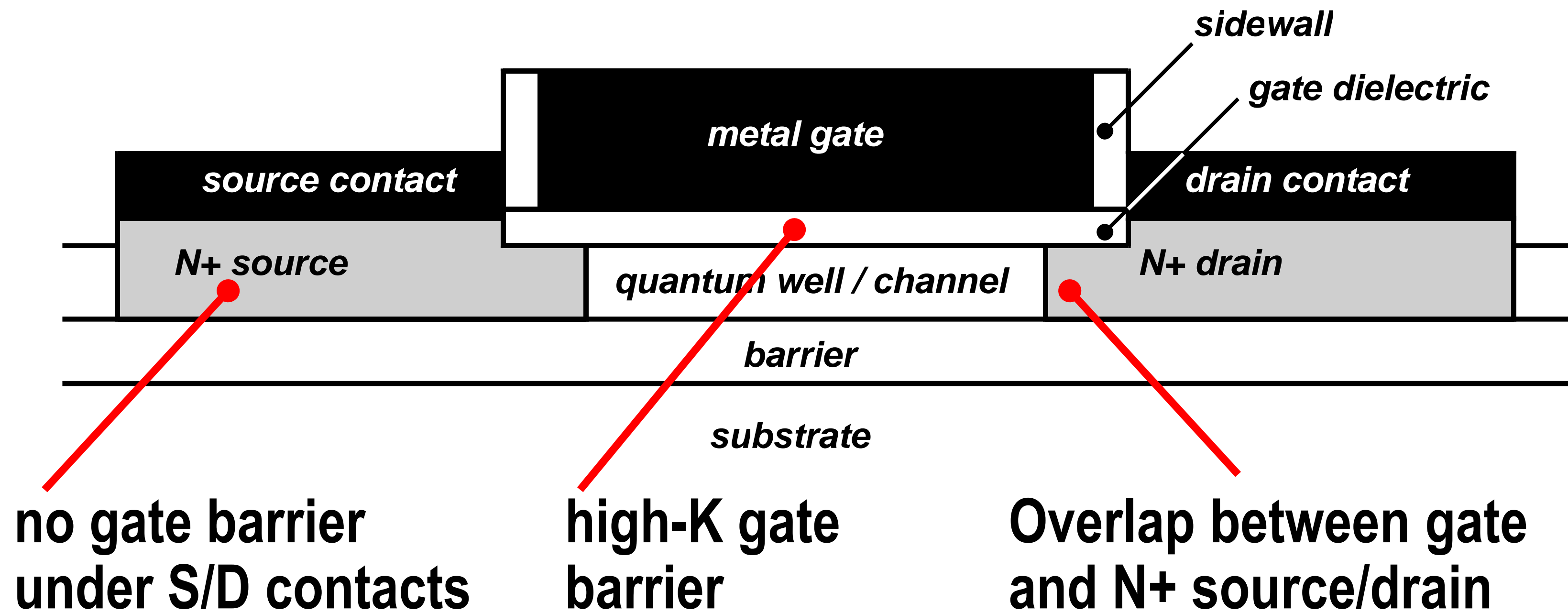
low leakage:
need high barrier under gate



low resistance:
need low barrier under contacts



The Structure We Need -- is Much Like a Si MOSFET

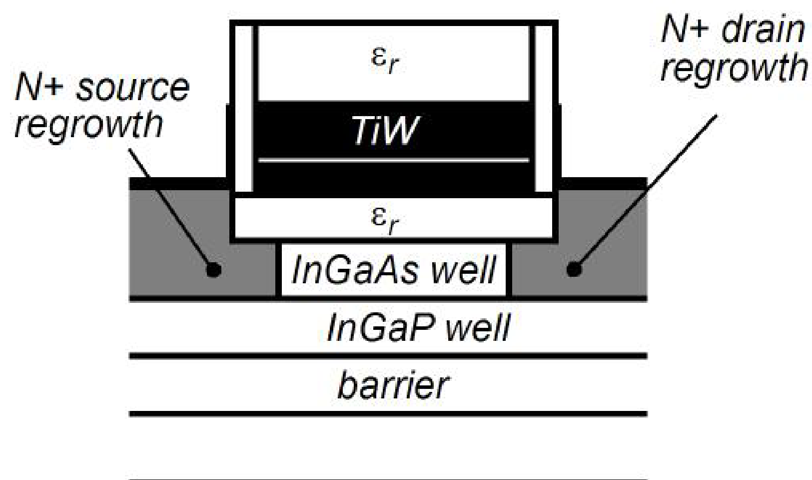


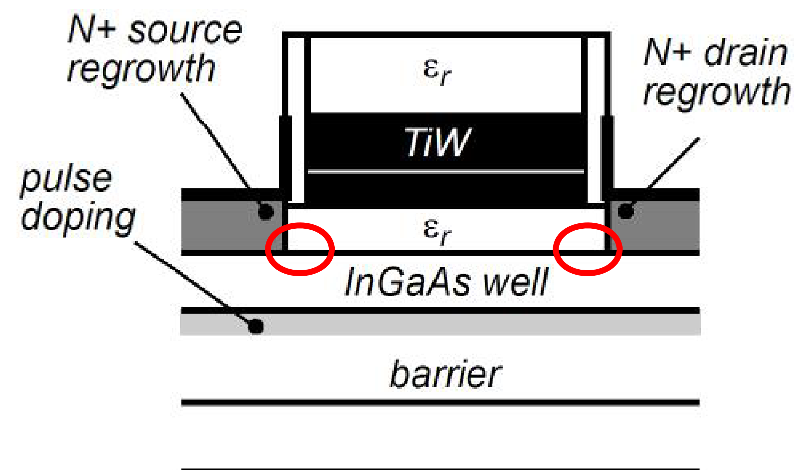
How do we make this device ?

S/D Regrowth Process Flow

Regrown S/D FETs: Versions

Wistey et al 2008 MBE conference





regrowth under sidewalls

planar regrowth

need thin sidewalls (now ~20-30 nm)

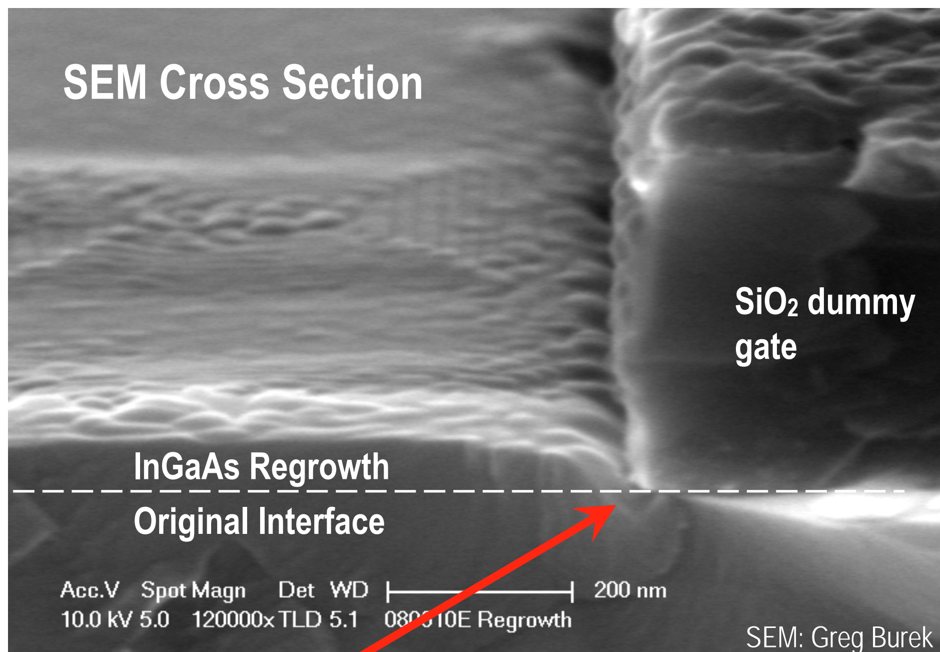
..or doping under sidewalls

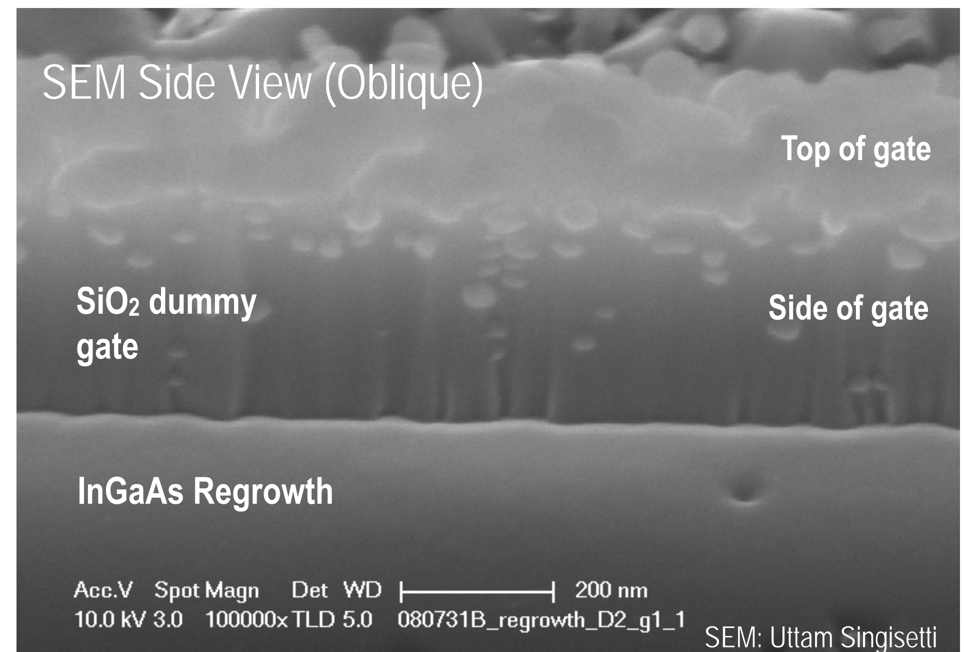
S/D Regrowth by Migration-Enhanced Epitaxy

Wistey et al 2008 MBE conference

MBE growth is line-of-sight → gaps in regrowth near gate edges

MEE provides surface migration during regrowth→ eliminates gaps





No gaps

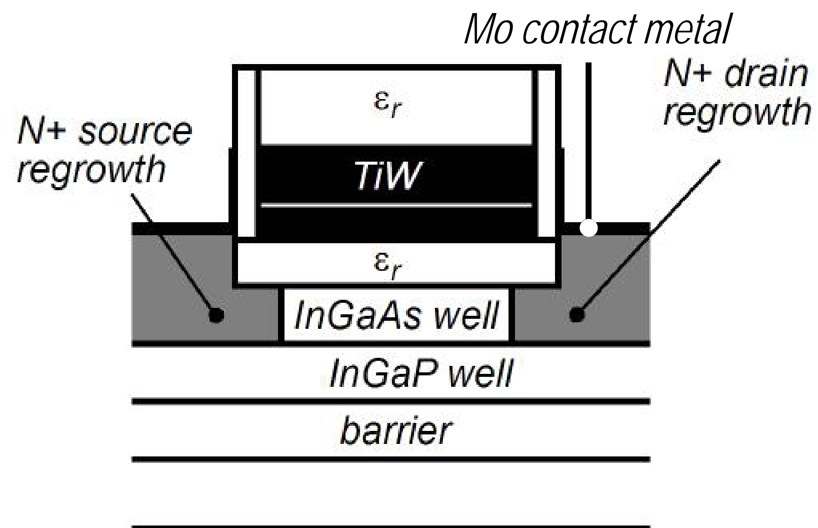
Smooth surfaces.

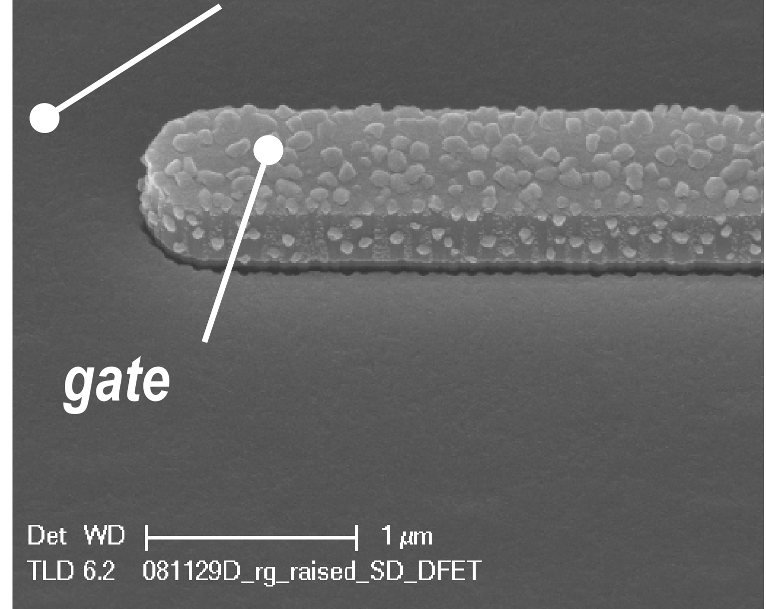
High Si activation (4×10^{19} cm^{-3}).

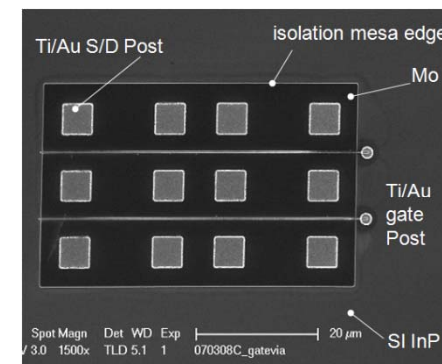
Quasi-selective: no growth on sidewalls

Self-Aligned Planar III-V MOSFETs by Regrowth

Wistey
Singisetti
Burek
Lee







Self-Aligned Planar III-V MOSFETs by Regrowth

Wistey
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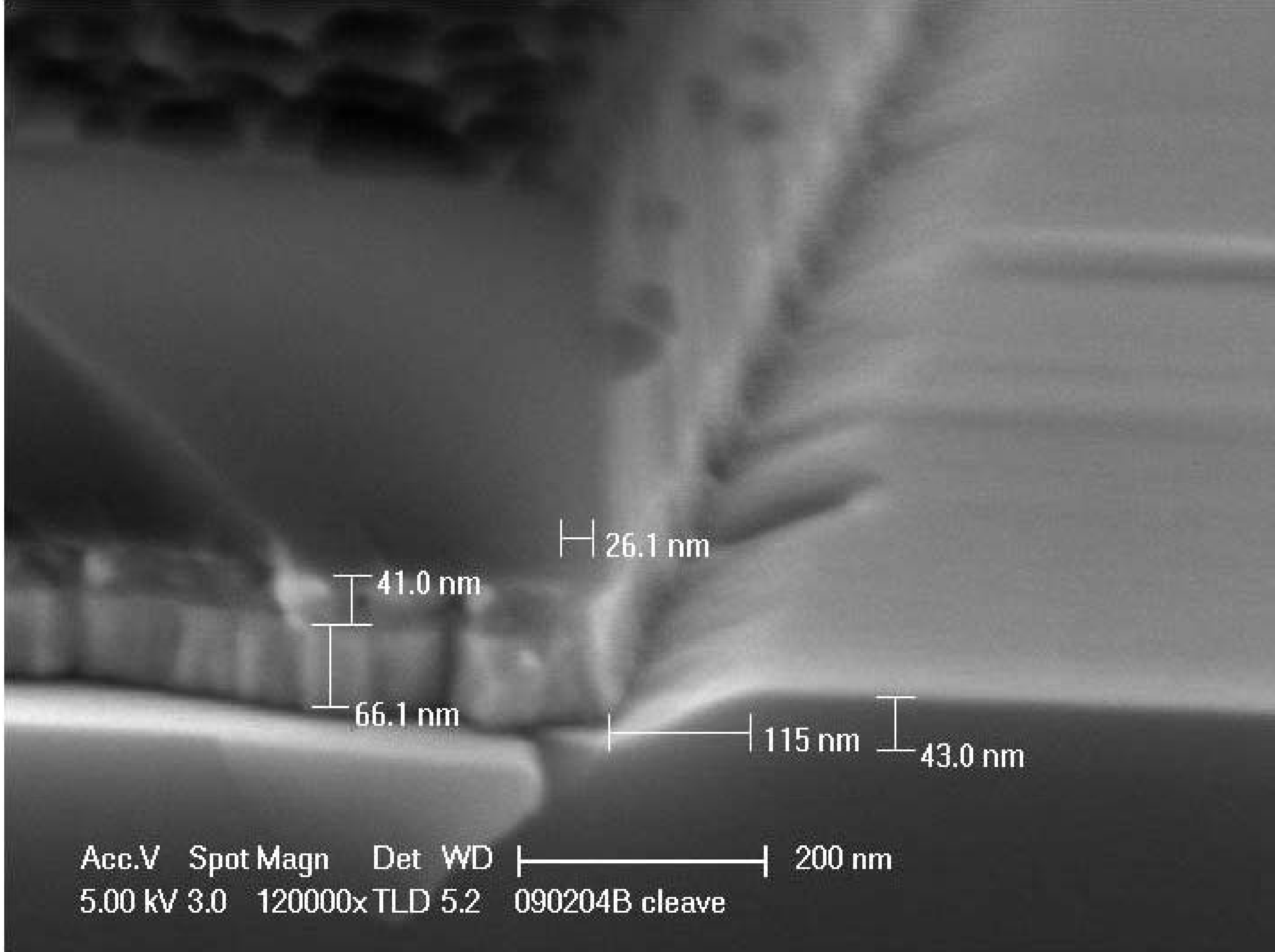
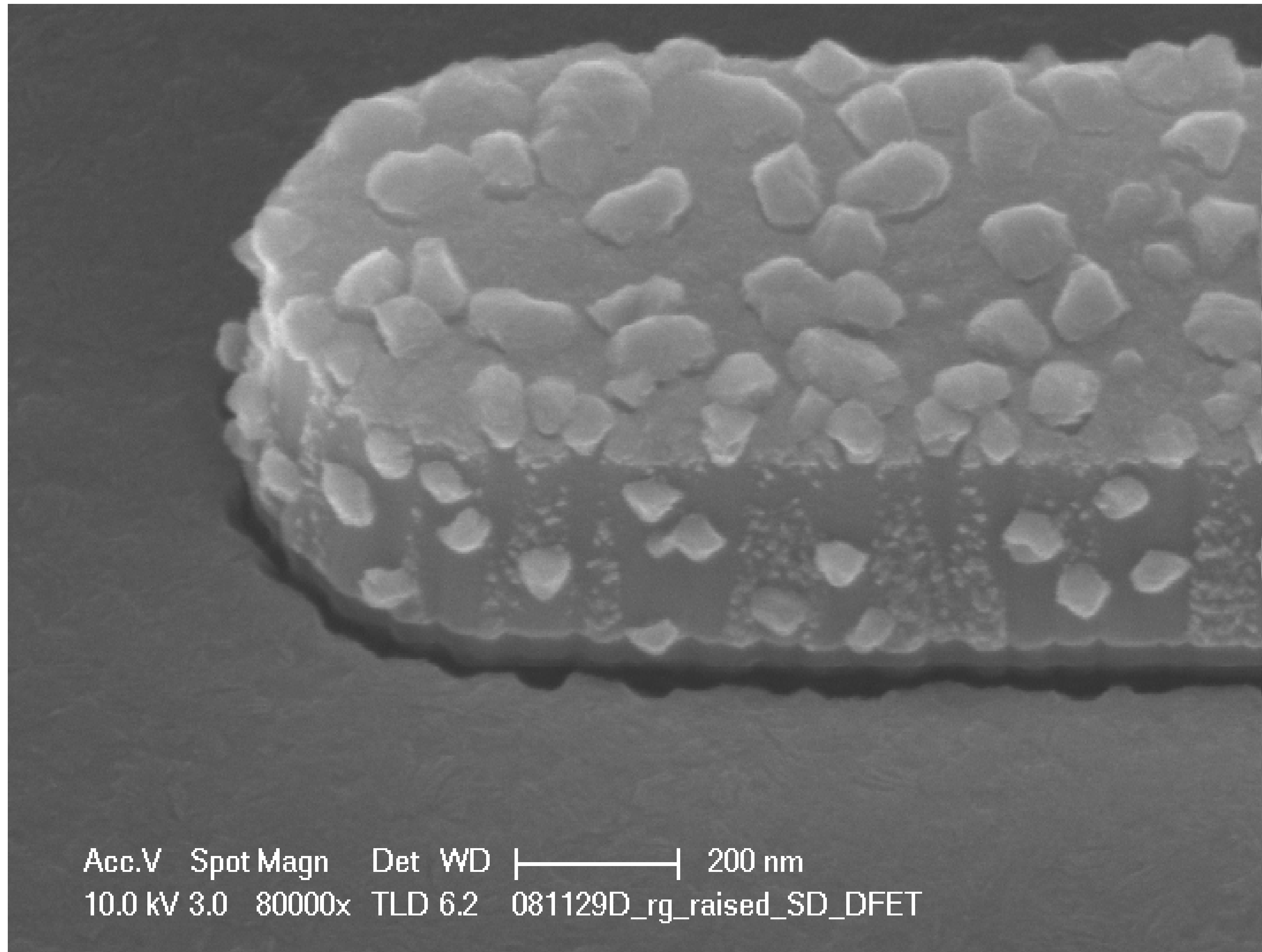
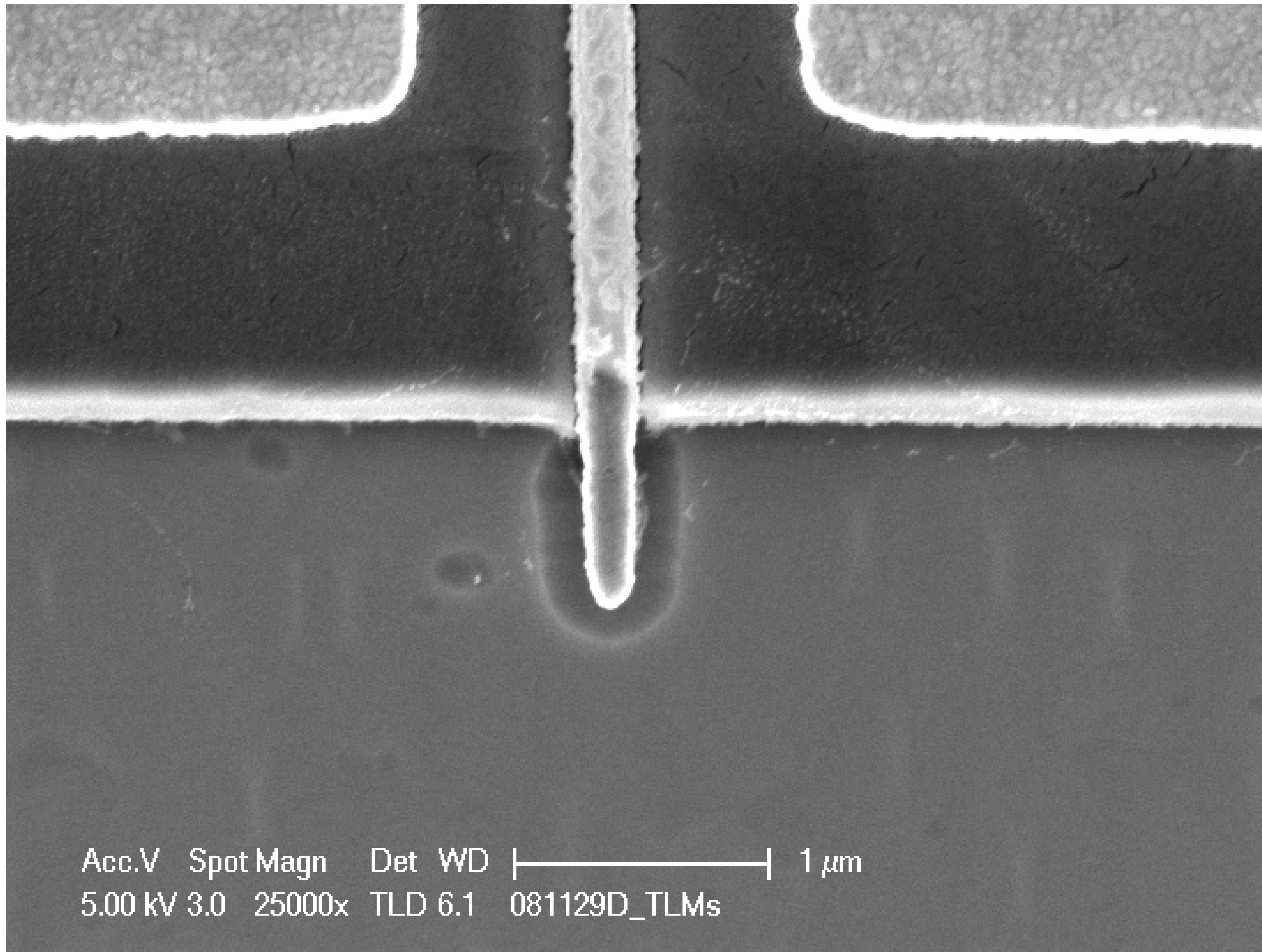
Lee



Regrown S/D FETs: Images



Regrown S/D FETs: Images



III-V MOS

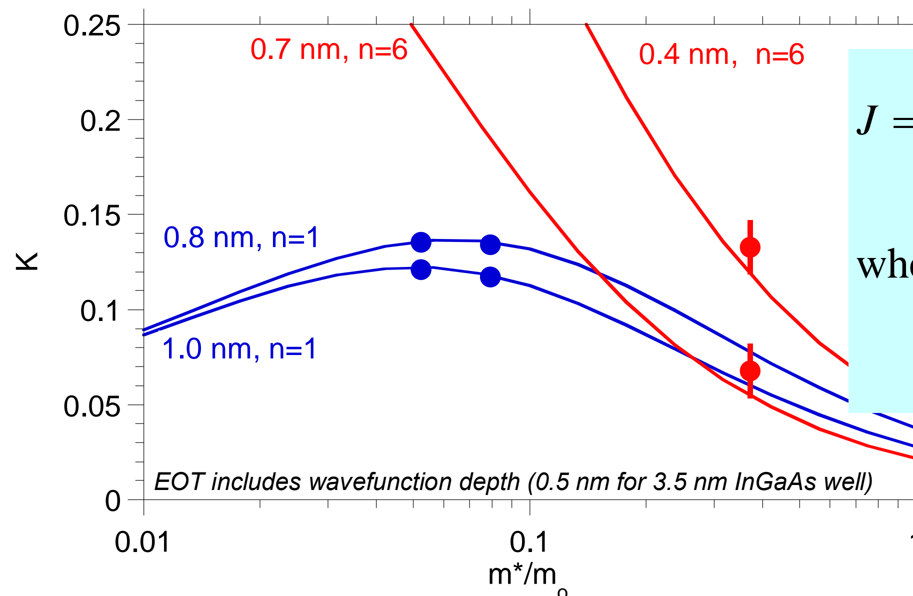
InGaAs / InP MOSFETs: Why and Why Not

low $m^*/m_0 \rightarrow$ high $v_{carrier}$ $\rightarrow$ more current
low $m^*/m_0 \rightarrow$ low density of states $\rightarrow$ less current

ballistic / degenerate calculation

Error bars on Si data points correct for $(E_f - E_c) >> kT$ approximation

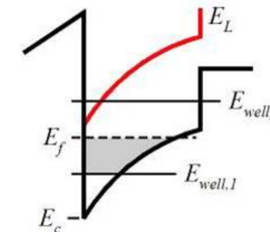
n = # band minima
$c_{dos,o}$ = density of states capacitance for $m^*=m_0$ & $n=1$



$$J = K \cdot \left(84 \frac{\text{mA}}{\mu\text{m}}\right) \cdot \left(\frac{V_{gs} - V_{th}}{1\text{ V}}\right)^{3/2},$$

$$\text{where } K = \frac{n \cdot \left(m^*/m_o\right)^{1/2}}{\left(1 + \left(\frac{c_{dos,o}}{c_{ox}}\right) \cdot n \cdot \left(\frac{m^*}{m_o}\right)\right)^{3/2}}$$

Low m* impairs vertical (hence L_g) scaling ;
InGaAs no good below 22-nm.



InGaAs allows very low access resistance

Si wins if high-K scales below 0.6 nm EOT; otherwise, III-V has a chance

InGaAs/InP Channel MOSFETs for VLSI

Low-m materials are beneficial only if EOT cannot scale below ~1/2 nm*

Devices cannot scale much below 22 nm Lg→ limits IC density

Little CV/I benefit in gate lengths below 22 nm Lg

Need device structure with very low access resistance
radical re-work of device structure & process flow

Gate dielectrics, III-V growth on Si: also under intensive development