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Enhancement Mode $In_{0.53}Ga_{0.47}As$ MOSFET with self-aligned epitaxial Source/Drain regrowth

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Abstract

A scalable, self-aligned $In_{0.53}Ga_{0.47}As$ MOSFET process was developed and enhancement mode device operation was demonstrated. The 0.7 μm L_g device shows a maximum drive current of 0.14 mA/μm at V_{gs}=4.0V and V_{ds}=2.5 V. The devices have almost an order of magnitude larger drive current than our previously reported MOSFETs. The channel layer was 5 nm thick InGaAs with InAlAs bottom barrier for vertical confinement. 4.7 nm of Al_2O_3 (~ 2 nm EOT) dielectric was deposited in an atomic layer deposition tool. After gate formation, self-aligned source/drain regions were defined by migration enhanced epitaxial (MEE) regrowth, and self-aligned *in-situ* Mo source/drain contacts were formed.

Index Terms—InGaAs MOSFET, III-V MOSFET, MBE regrowth, MEE

I. Introduction

Silicon MOSFETs may reach the scaling limit, if reliable low leakage sub-0.5 nm equivalent oxide thickness (EOT) gate dielectrics are not realized [1]. In this scenario, III-V semiconductors are investigated as alternative channel material because of their low electron effective mass (m^*) and thus high electron velocities (v). $In_xGa_{1-x}As$ ($x \geq 0.53$) is a leading candidate because of the experimentally observed high electron velocities in InGaAs channel HEMTs [2]. Besides the low electron effective mass, InGaAs has large inter-valley separations (0.5 eV for $In_{0.53}Ga_{0.47}As$) which means high velocities even under high applied fields. This ensures no degradation in electron transport properties in a high field drain region encountered in scaled MOSFETs.

The key obstacle of unpinned high-k dielectric interface to InGaAs is investigated by various groups with different dielectrics [3, 4, 5, 6], and is not addressed in this paper. Instead, we focus on the self-aligned source/drain formation on vertically scaled InGaAs MOSFETs. Detailed MOSFET scaling laws and sub-22nm InGaAs MOSFET design are discussed in references [1, 7, 8], the key features of which are briefly summarized here. Horizontal lithographic scaling of the gate length dictates a vertical scaling of the gate dielectric and the channel to maintain electrostatic integrity. At sub-22nm gate lengths a maximum of 1 nm EOT gate dielectric and 5 nm channel with strong confinement are required for maximum transconductance (g_m) and acceptably low drain induced barrier lowering (DIBL) or G_{ds}/g_m ratio. High drive currents (I_d=5mA/μm) and high transconductances (g_m=7mS/μm) are simulated for these scaled InGaAs MOSFETs [1, 8]. We use a 5 nm $In_{0.53}Ga_{0.47}As$ (InGaAs) channel with bottom $In_{0.48}Al_{0.52}As$ (InAlAs) layer for vertical confinement.

The source access resistance plays an important role in scaled devices because it degrades the available drive current and transconductance from the device. Even a low 10 Ω–μm source access resistance degrades I_d of 22 nm InGaAs MOSFETs by 10%. In a VLSI device, where packing density is an important parameter, the source contact length L_c must scale with gate length. Assuming a 25 nm L_c and 10 nm link length for 22 nm gate length device, an extremely low contact resistance (ρ_c = 0.25 Ω–μm^2) and high doping density (n = 5×10^{19} cm^{-3}) is required in the source/drain region [1]. Unlike silicon, ion-implantation may not a viable technique in III-V semiconductors due to various difficulties. The III-V ternaries usually have high residual damage even after annealing, and these defects compensate shallow dopants making it difficult to achieve target high carrier densities [9]. Moreover, loss of group V elements during high temperature anneals irreversibly ruins the stochiometry of the semiconductor [9]. The residual damage may also increase the junction leakage. The difficulty is made more serious in the presence of a bottom confinement

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InAlAs layer. Furthermore abrupt vertical and lateral dopant profile is necessary for sub-22nm gate length devices. S/D contacts must be self-aligned to the gate, yet there is no known equivalent of self-aligned silicides in III-V materials.

Traditionally, epitaxial growth techniques such as metal organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE) and chemical beam epitaxy (CBE) have been the strength of III-V semiconductors. These epitaxial

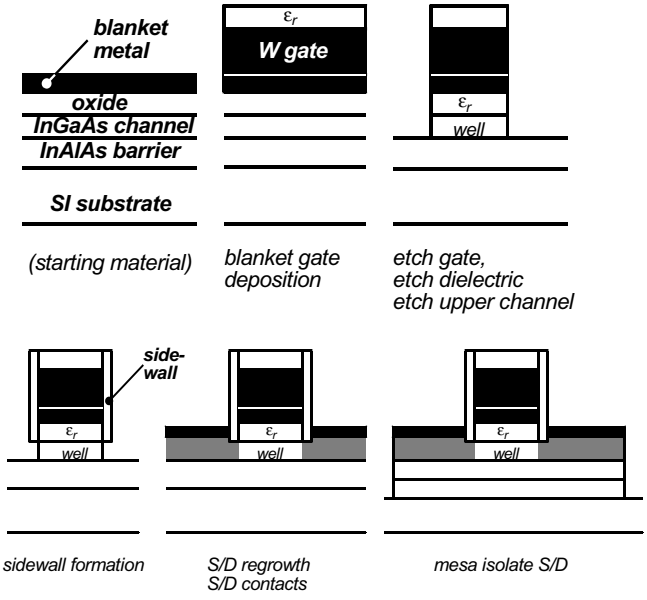


Figure 1: Process flow (Not to scale)

techniques can all produce high active doping densities (~ 4-10 × 10^{19} cm^{-3}) in InGaAs without the necessity of high temperature anneals. These densities are higher than available by ion implantation and avoid the damage and crystal disordering from implantation as well. In addition, *in-situ* Mo contacts to regrown n^{++} InGaAs have shown very low 2.5 Ω–μm contact resistivities [10].

Here we report InGaAs MOSFETs with n^{+} source/drain regions formed by epitaxial regrowth and self-aligned *in-situ* Mo contacts. The MOSFETs have a peak drive current of 0.14 mA/μm and a peak transconductance of 0.02 mS/μm. This is an order of magnitude larger drive current than the previously reported devices using this process [11, 12]. The increase in drive current is achieved because of a modified migration enhanced epitaxial regrowth technique which results in a lower source access resistance.

II. Growth and Fabrication

The complete process flow is described in detail in the reference [12] and a summary of which is shown in Fig 1. First 5 nm InGaAs channel with NID InAlAs back barrier is grown on semi-insulating InP by molecular beam epitaxy (MBE) and capped with arsenic. The cap layer was desorbed *in-situ* in an atomic layer deposition (ALD) chamber at 480 ºC, and 4.7 nm of Al_2O_3 (~ 2.0 nm EOT) was deposited. A dry etched metal gate stack was then defined and sidewalls deposited. The high-k dielectric was wet etched and *n*+ InGaAs is regrown by MBE for source/drain definition. Next

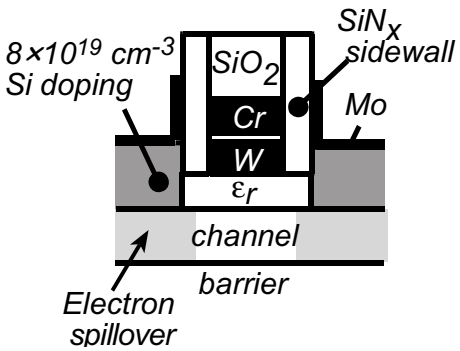


Figure 2: Cross-sectional schematic of the finished device

self-aligned *in-situ* Mo contacts were defined. The final device (Fig. 2) has both self-aligned source/drain and contacts, the source access distance given by the well controlled SiN_x sidewall thickness. Unlike implanted or diffused techniques, there is no extrinsic doping under the sidewall. Electron "spill over" from the n^{++} regrowth region provides the necessary carriers in this region.

Thin channel layers (~ 5 nm) are prone to ion damage and contamination during processing. Any dry etch damage to this thin layer can prevent good epitaxial regrowth leading to high source resistance [12]. Additionally, any pinholes introduced in this layer would expose the underlying InAlAs layer. The

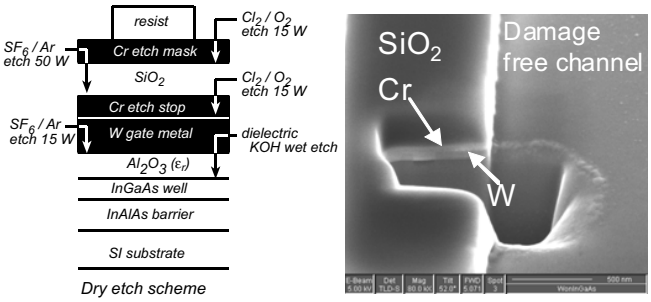
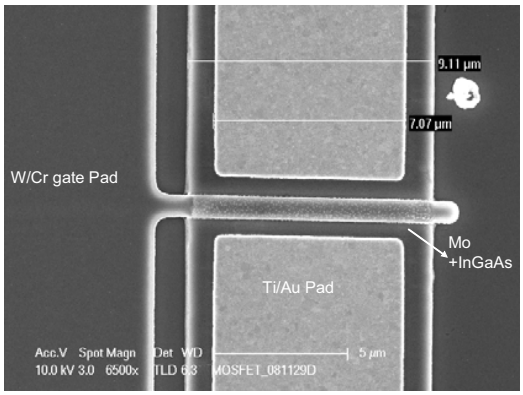


Figure 3: Gate dry etch process and FIB X-section SEM of the gate after dry etch before regrowth

aluminum containing layer is rapidly oxidized in air which can prevent good epitaxial regrowth. Therefore a multiple layer gate stack is defined in which each layer is an etch stop for the layer above it. As seen in Fig. 3, an alternative series of selective etches is used to define the gate, stopping gently on the high-k dielectric. Then 20-25 nm of SiN_x sidewalls are defined by a low power anisotropic ICP-RIE etch. The Al_2O_3 dielectric layer was then etched off in dilute KOH (AZ 400K developer) stopping on the InGaAs channel layer. As seen in scanning electron micrograph (SEM) 400 nm tall gates are defined on thin (3-5 nm) channel layers with no apparent surface damage (Fig. 3). The gate metal is encapsulated on all sides with dielectric layers preventing possible contamination

of MBE during regrowth. The process is easily scalable to sub-100nm gate lengths with advanced photo or electron lithography technologies.

The wafer was then exposed to UV-Ozone for 30 minutes followed by a 60s dip in dilute HCl to remove surface oxides, then rinsed in DI water. Next the wafer was blown dry in N_2 and loaded immediately into the MBE chamber. After an overnight bake at 200 ºC, the wafer was hydrogen cleaned at 400-420 ºC. A (4×2) surface reconstruction was seen in reflection high energy electron diffraction (RHEED) before regrowth, indicating an epi-ready surface. 50 nm of 8×10^{19} cm^{-3} Si (~ n=4×10^{19} cm^{-3}) doped InGaAs was grown at 540 ºC by migration enhanced epitaxy (MEE). Then wafer was transferred under ultra high vacuum (UHV) to an electron beam evaporator and 20 nm of Mo was deposited. Because the Mo is also deposited on the gate top surface, the source and drain are short-circuited. The wafer was therefore planarized



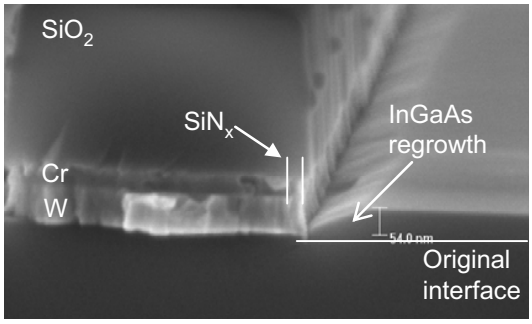


Figure 4: Top view SEM of a finished device. X-section SEM of MOSFET after regrowth before Mo depostion.

with photoresist and the Mo on the gate removed with a height-selective etch [13]. S/D pads were then deposited, and devices mesa-isolated. To contact the gates, the silicon dioxide on top of the gate pads was removed by etching in buffered HF (Fig. 4).

III. Measurements and Results

The cross-section SEM (Fig. 4) shows a slope in the regrowth surface next to gate, but no gap is observed between the N+ regrown material and the gate edge. The regrowth is quasi-selective, i.e. material is deposited on the gate top surface, but there is little growth on the gate sidewalls. The

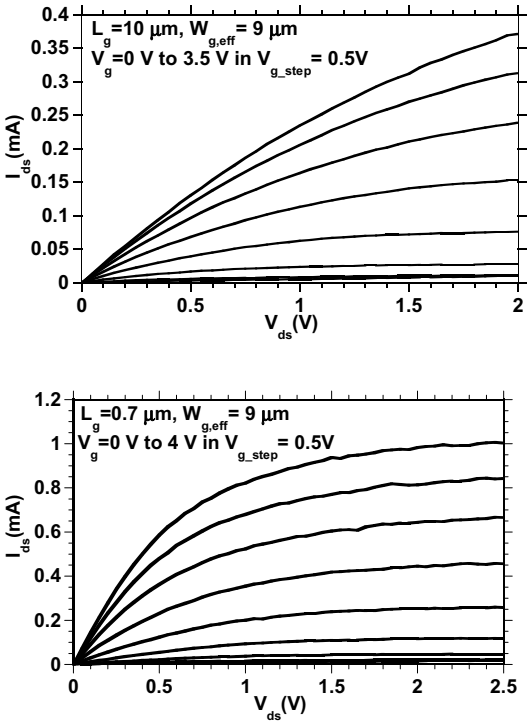


Figure 5: DC characteristics of the 10 µm L_g and 0.7µm L_g MOSFETs

DC characteristics of the MOSFETs is shown in Fig. 5. The L_g= 0.7 µm devices has peak I_d is 0.14 mA/µm and peak transconductance g_m is 0.02 mS/µm at V_{gs}=4.0 V and V_{ds}=2.5 V. The peak drive current is an order magnitude larger than our previously reported MOSFETs in this technology [11,12]. The improved drive current is because of absence of any gaps between the gate and regrowth edge in the MEE technique and

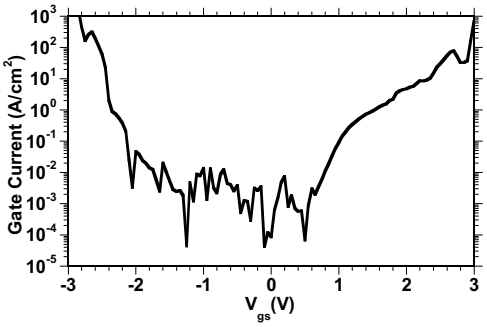


Figure 6: Measured Gate Leakage

hence absence of carrier depletion in the thin channel due to surface states. The gate leakage current is shown in Fig. 6. The leakage current does not scale with gate length but scales with gate width, suggesting a dominant leakage through the SiN_x sidewalls.

From measurements of zero-bias on-resistance (Fig. 7), a 3.8 kΩ–µm source resistance is determined. TLMs patterns on the regrown material located far from MOSFET showed 28 Ω/□ sheet resistance and 17 Ω–µm Mo/InGaAs (lateral) contact resistance. The large discrepancy between the source

resistance observed in the FET and lateral access resistance observed in TLM patterns may indicate that the regrown

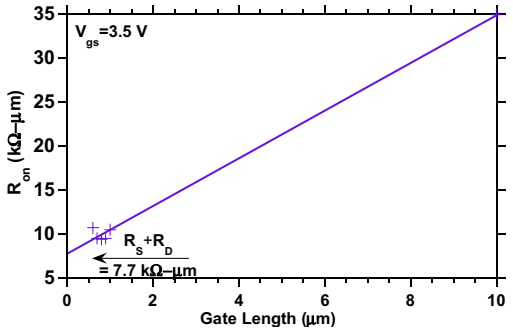


Figure 7: FET on resistance at Vds=0.

InGaAs close to the gate has higher resistivity than in the far field. Possible causes of high source resistance include lack of Si doping next to gate, lattice mismatched growth next to gate causing dislocations which deplete electrons, or high defect density at the regrowth interface. Any defects induced at Al_2O_3/InGaAs interface during regrowth will deplete electrons in the channel under the sidewall. This will also increase the source resistance.

Experiments to evaluate the electrical properties of the regrown InGaAs next to gate are currently in progress. Devices fabricated with modulation doping of the channel to compensate for any surface/interface and bulk defects show an order of magnitude higher drive current. These results will be presented elsewhere [14].

In conclusion, we have demonstrated enhancement mode InGaAs MOSFETs with 5 nm channel thickness with self aligned epitaxial source/drain and self-aligned contacts. The devices show that raised S/D InGaAs regrowth can be a potential technology for highly scaled III-V devices. Improved regrowth next to gate could enable the high drive currents predicted by simulations of scaled InGaAs MOSFETs.

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