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III-V/Ge Channel Engineering for Future CMOS

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Outline: Channels for Future CMOS

UCSB

- FET scaling requirements... and failures
- Motivation for Regrown MOSFETs
- III-V Benefits and Challenges
- Fabrication Process Flow
- Depletion-mode MOSFETs
- The Shape of Things to Come

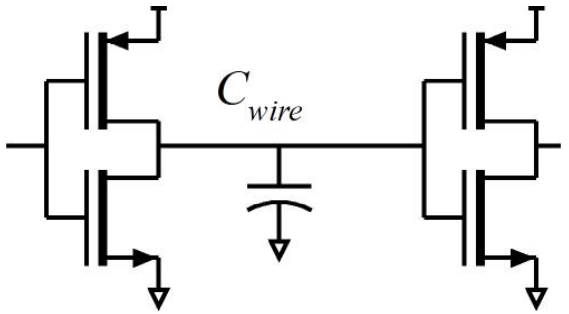
Future CMOS Priorities

UCSB

High Performance

High drive current I_d / W_g for wiring

Low gate delay $C_{FET}\Delta V/I_d$ for local

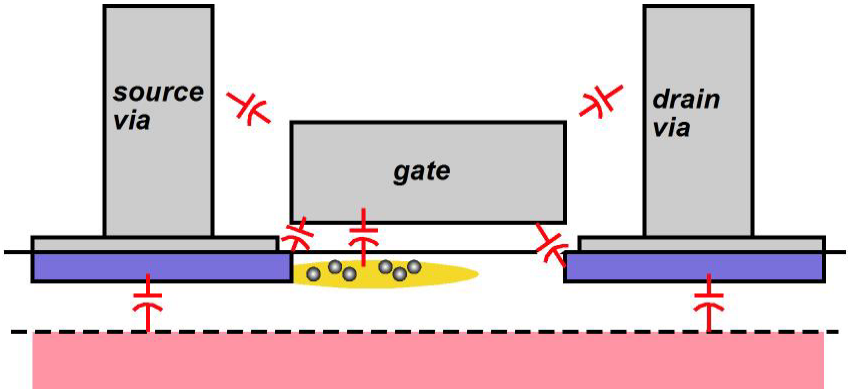


Low Parasitics

Capacitance – already 1-2 fF/μm

Resistance – already ~50% R_{tot}

Leakage Currents – now 50% power



Compatible with Existing CMOS

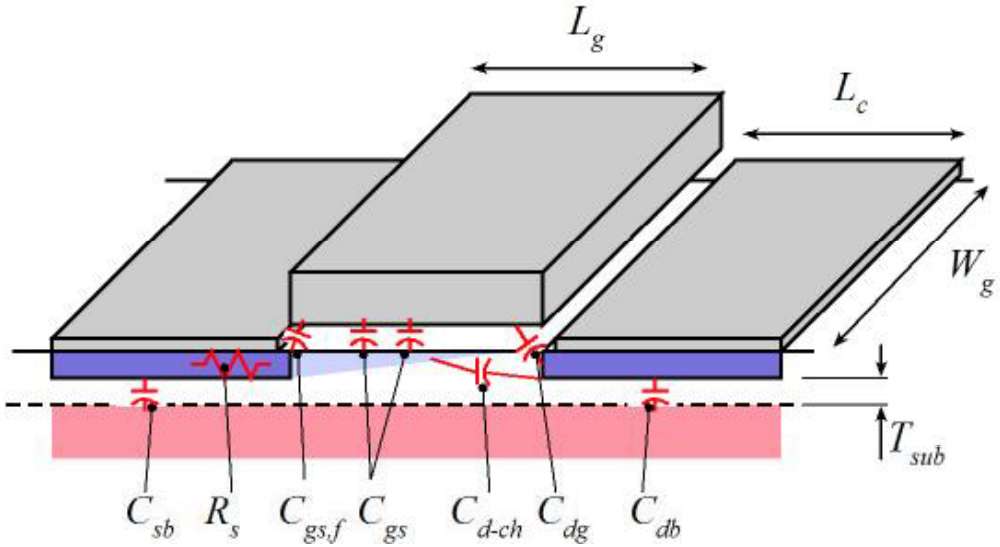
High packing density –width & contacts small

Growable on Si substrates

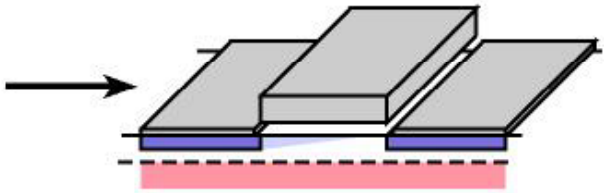
Graphics: Mark Rodwell

Simple FET Scaling

*Goal double transistor bandwidth when used in **any** circuit*
→ reduce 2:1 all capacitances and all transport delays
→ keep constant all resistances, voltages, currents



reduce 2:1 all lengths, widths, thicknesses



$g_m \sim (\varepsilon / T_{ox}) v_{th} W_g$ → *g_m , I_d held constant* ✓ *(doubles mA/⌈m, mS/⌈m)*

$G_{ds} \sim C_{d-ch} v_{th} / L_g \sim \varepsilon W_g v_{th} / L_g$ → *held constant* ✓

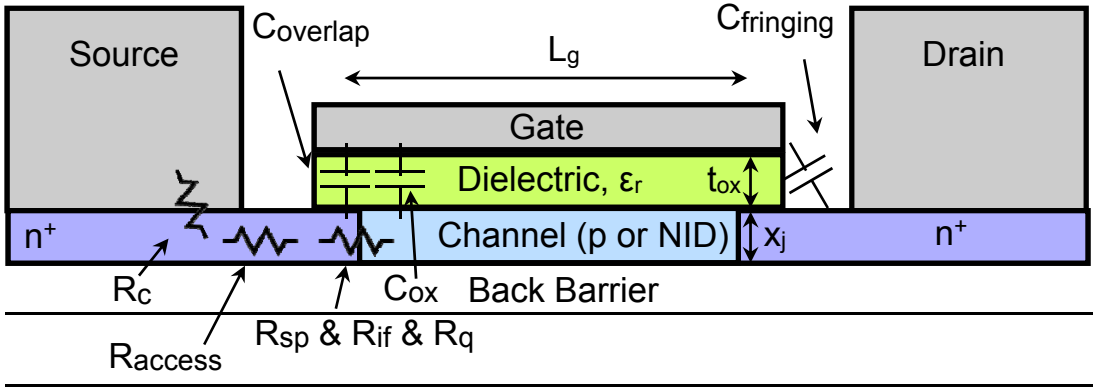
$C_{gs} \sim \varepsilon W_g L_g / T_{ox}$ → *reduced 2:1* ✓

$C_{gs,f} \sim C_{gd} \sim \varepsilon W_g$ → *edge capacitances reduced 2:1* ✓

$C_{s-b} \sim C_{d-b} \sim \varepsilon W_g L_c / T_{sub}$ → *substrate capacitances reduced 2:1* ✓

$R_s \sim \rho_{sheet} L_c / 3W_g + \rho_{contact} / L_c W_g$ → *must reduce ⟩$_c$ 4:1*

"External" Resistances are Critical



Resistances constant ⇒ Resistivities must scale as $1/L_g^2$:

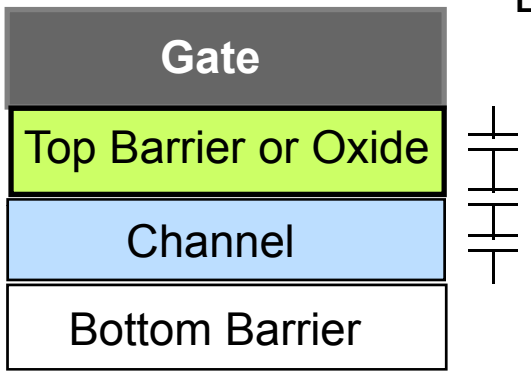
- **Contact resistance R_c**
- **Access & spreading resistance**
- **Interface resistance & source starvation**
- **Sharvin resistance (quantized c**

$$R_q W = \frac{\pi\hbar}{q^2}\frac{\lambda_F}{2} = \frac{\pi\hbar}{q^2}\sqrt{\frac{2}{n_s}} = (52\,\Omega - \mu\text{m})\sqrt{\frac{10^{13}/\text{cm}^2}{n_s}}$$

Transconductance Scaling Challenges

$g_m \sim (1/C_{g\text{-}ch}) v_{th} W_g$ ...Should stay constant (double mA/μm)

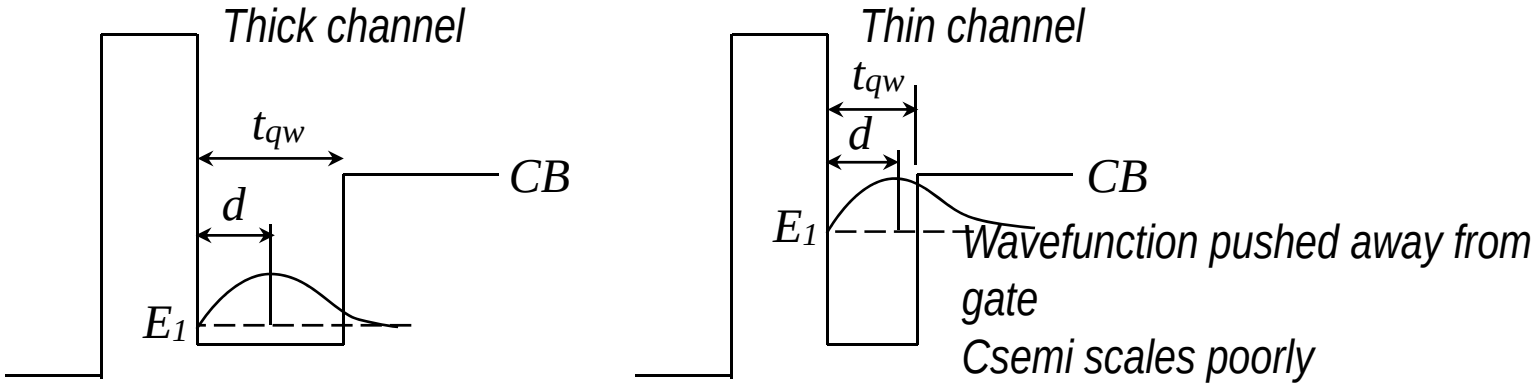
But voltage divider exists: $\frac{1}{C_{g-ch}} = \frac{1}{C_{ox}} + \frac{1}{C_{semi}} + \frac{1}{C_{dos}}$



C_{ox} scales as 1/EOT ...EOT scales poorly ☹

$C_{semi} \sim \varepsilon_{chan} L_g W/d$ ...Smaller ☹

$C_{dos} = \frac{2\pi\hbar^2}{q^2 m^*} L_g W$ ...Smaller ☹



Similar problem with overlap & fringing capacitances.

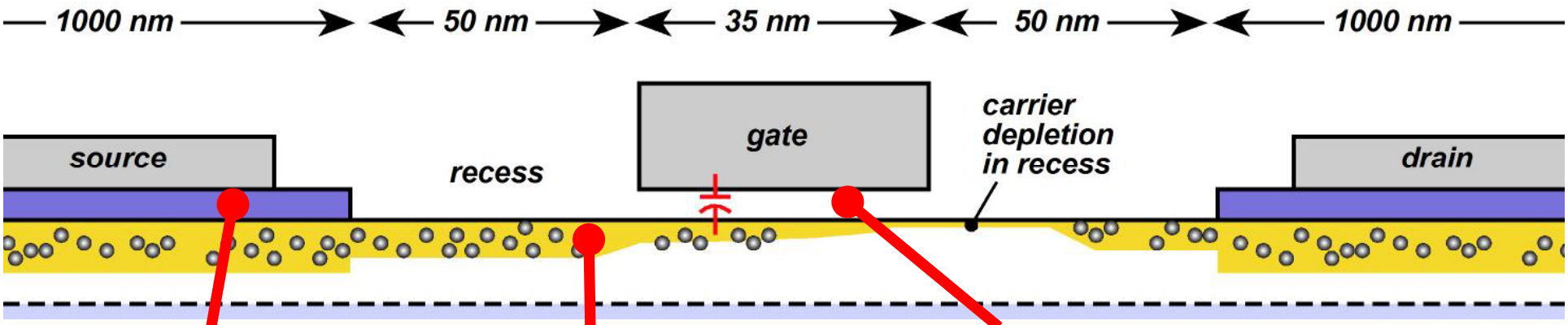
Solution: Increase v_{th} using new material.

MOTIVATION FOR REGROWN FETs

Device Choice: Why not HEMTs?

Wide recess→ okay DIBL, subthreshold slope, C_{gd}
Wide contacts→ Rc okay even with poor contacts

} Not scaled



Injection thru barrier

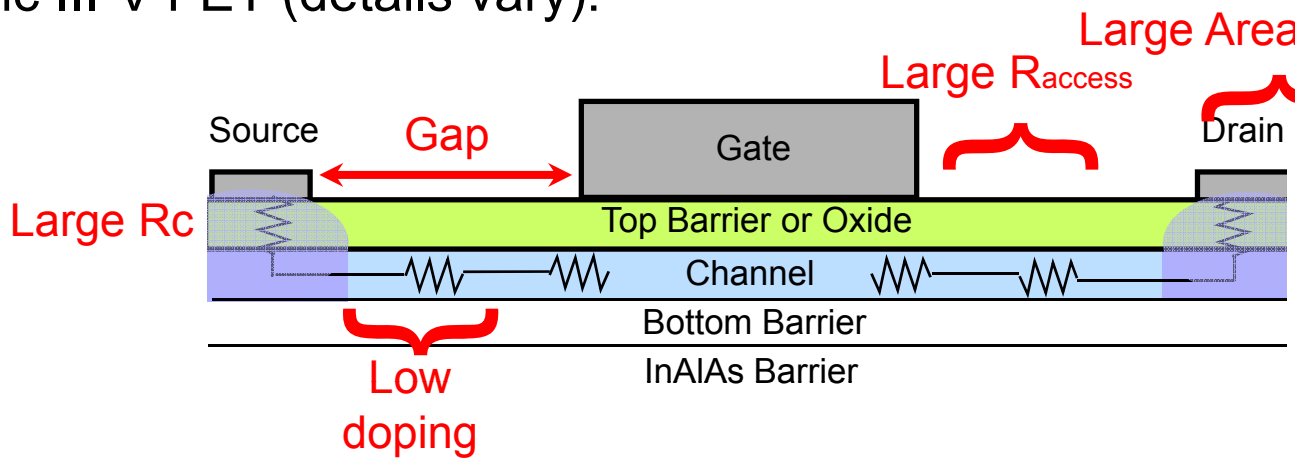
Long recesses, lightly doped
= high R_{access}

Low gate barrier
= Limited carrier density

○ HEMTs obscure scaling issues.

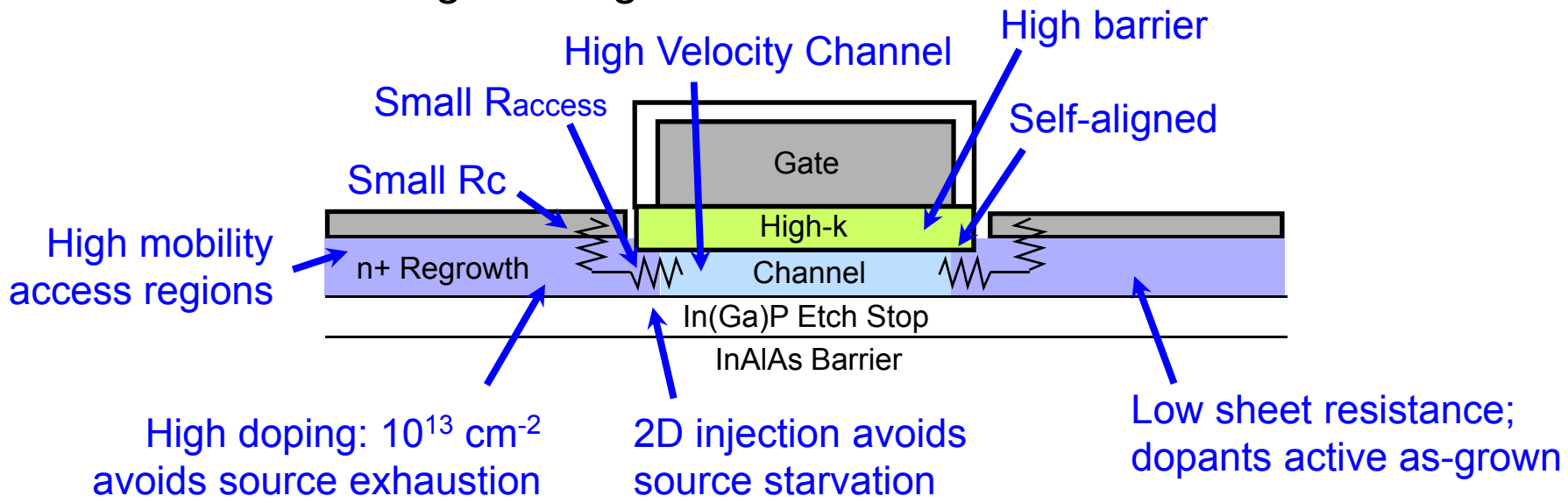
Scalable III-V FET Design

Classic III-V FET (details vary):



- Advantages of III-V's
- Disadvantages of III-V's

III-V FET with Self-Aligned Regrowth:



Big Picture: Salicide-like Process

Analogy: Self-aligned silicide (salicide) process:

Take from Silicon:
Unlike classic III-V devices:
Avoid liftoff
Dry etches
Self-aligned processes
Surface channels
Do III-V fabrication in Si-like fashion.

Break from Silicon:
No implantation
Insufficient doping
Surface damage
Annealing is no panacea
Encapsulate gate metals
Arsenic capping
Ship wafers for high-k
Strain is cheap

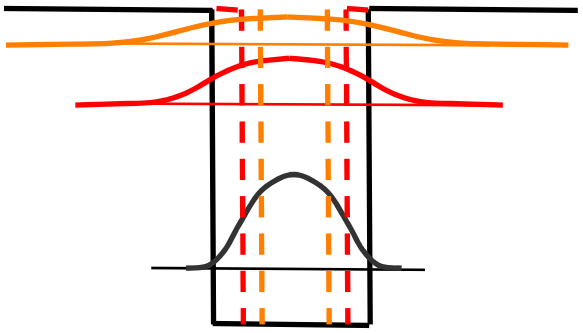
III-V Benefits and Challenges

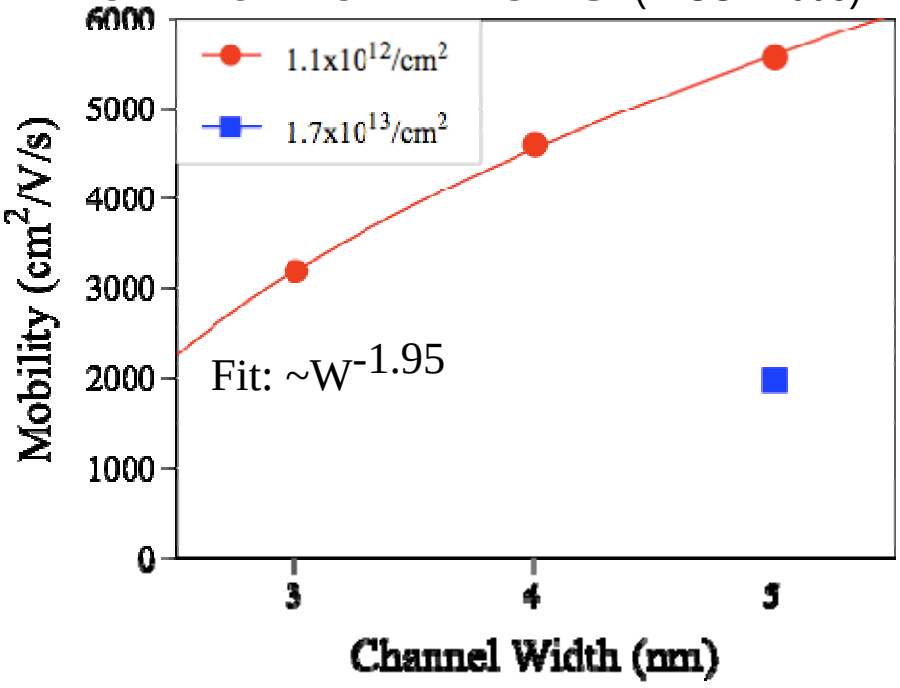
Channel Roughness Scattering

- Challenge: Sixth power (!) scattering from interface roughness:

  $\mu \sim (1/M_{scat})^2 \sim 1/(\partial E/\partial W)^2 \sim W^6$ (Gold SSC 1987)

- Trend weaker in shallow or narrow wells (Li SST 2005)

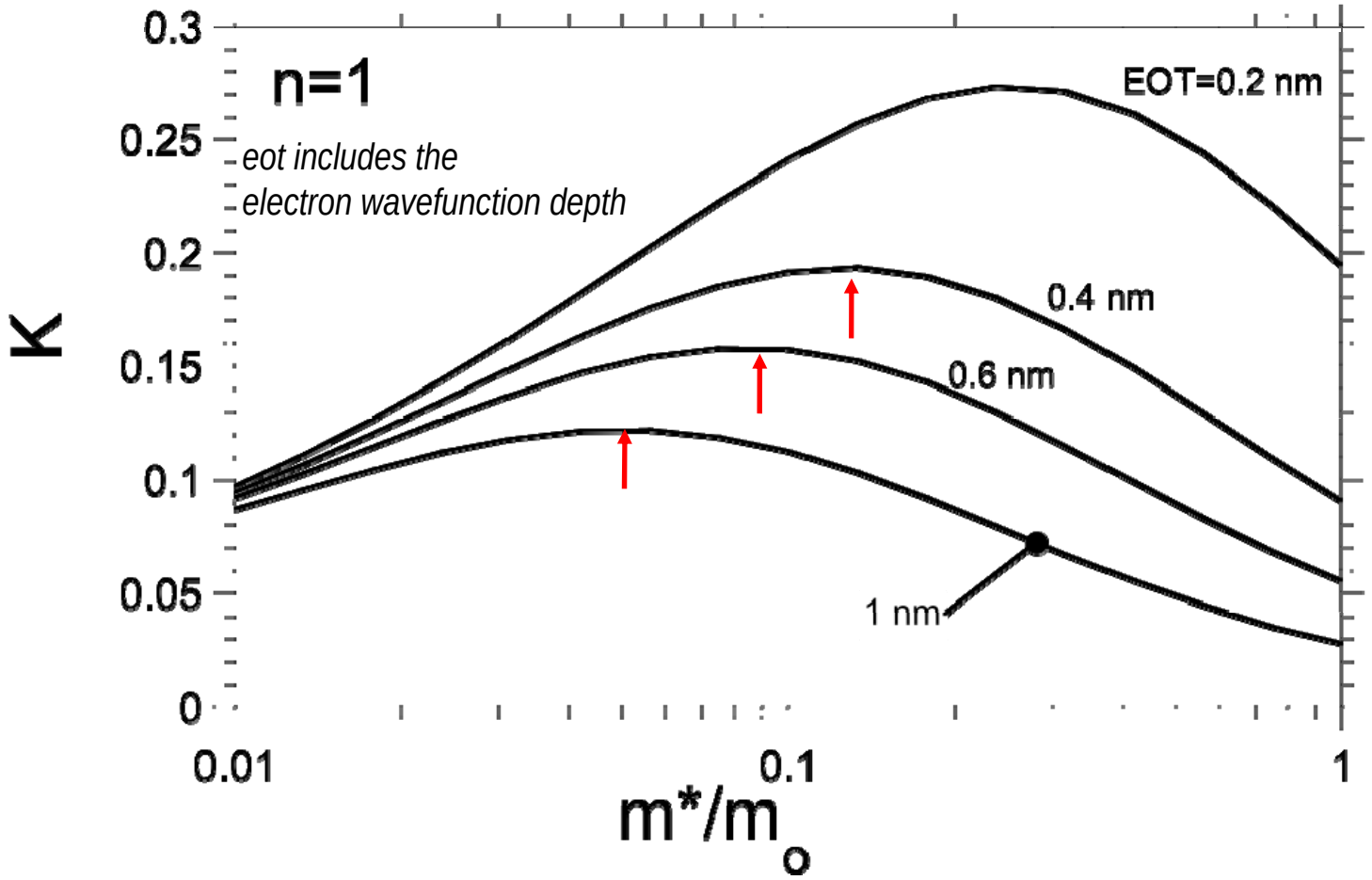




- Screening helps too
- Does not seem to be a problem for 5nm InGaAs channels.

Drive Current in the Ballistic & Degenerate Limits

$$J = K \times \left(84\frac{mA}{\mu m}\right) \times \left(\frac{V_{gs} - V_{th}}{1V}\right)^{3/2} \qquad \text{where} \qquad K = \frac{n \times \left(m^* / m_0\right)^{1/2}}{\left[1 + \left(c_{dos,o} / c_{ox}\right) \times \left(m^* / m_0\right)\right]^{1/2}}$$

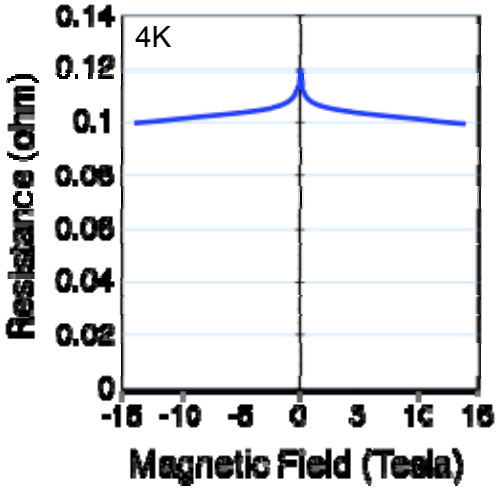


Inclusive of non-parabolic band effects, which increase c_{dos} ,

InGaAs & InP have near-optimum mass for 0.4-1.0 nm EOT gate dielectrics

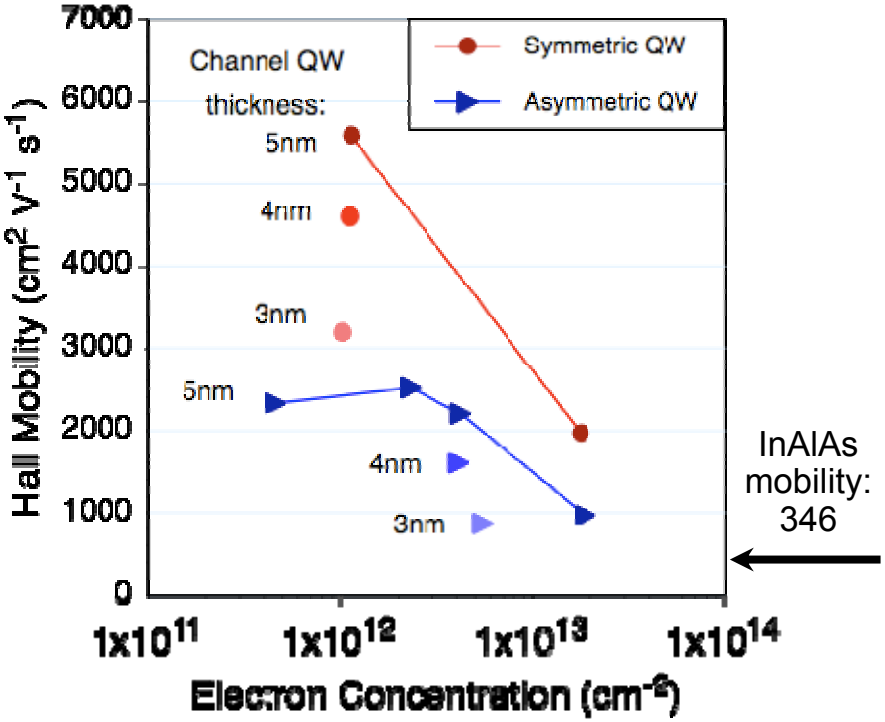
High Mobility in Narrow InGaAs Channels

No Shubnikov-de Haas Oscillations



○ Electrons occupy multiple channels

Hall Measurements



○ But electrons aren't in InAlAs...?

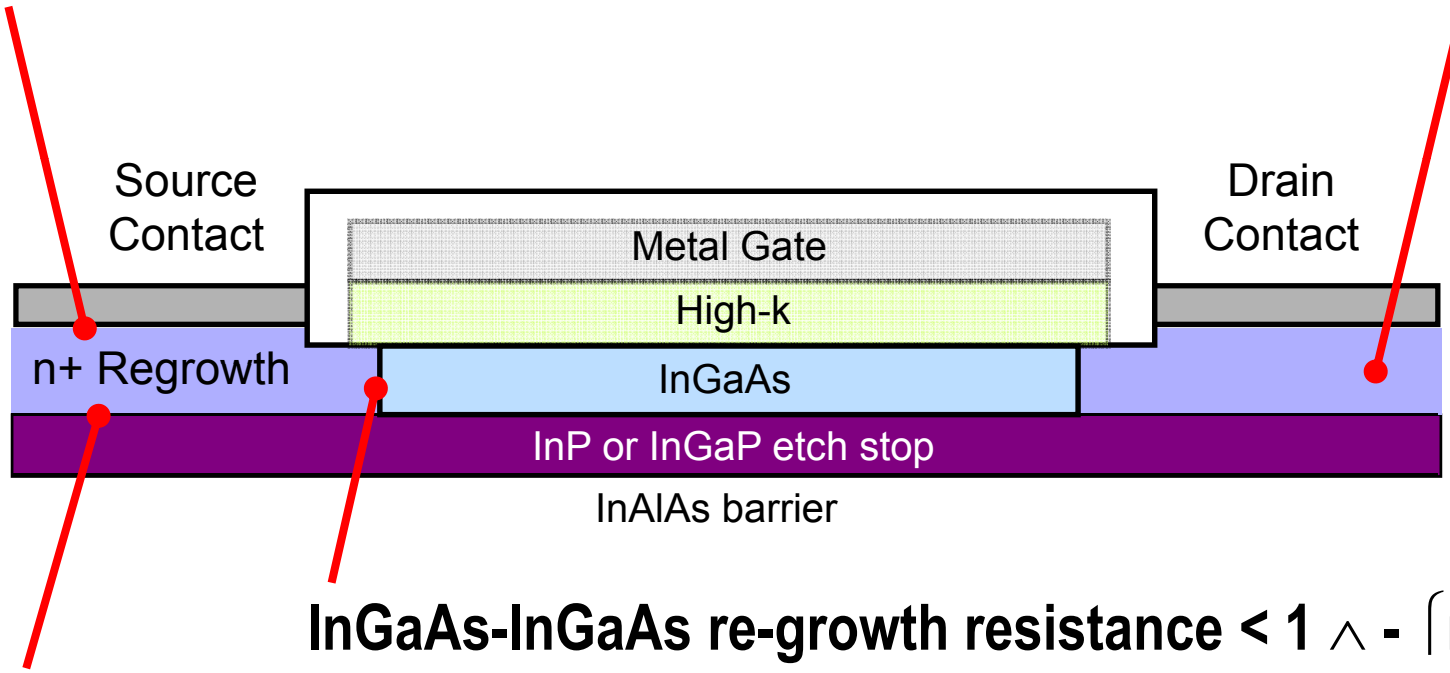
- **Unclear whether high mobility is in narrow channel**
- **Unreasonable simulation difficulty.**
  - Nonparabolic bands, degenerate statistics, bandgap renormalization, screening...
- **Need FET to remove uncertainty: eliminate doping altogether.**

Regrowth Interface Resistances

Interface resistances tested in separate blanket regrowths (no gates):

In-situ Mo Contact ρ_c < 1 Ω - μm^2

25 nm regrown InGaAs R_{sh}=70 Ω/sq



InGaAs-InGaAs re-growth resistance < 1 Ω - μm^2.

InGaAs-InP re-growth resistance = 6 Ω - μm^2 (on thick InP).

FABRICATION PROCESS FLOW

Process Flow: Gate Deposition

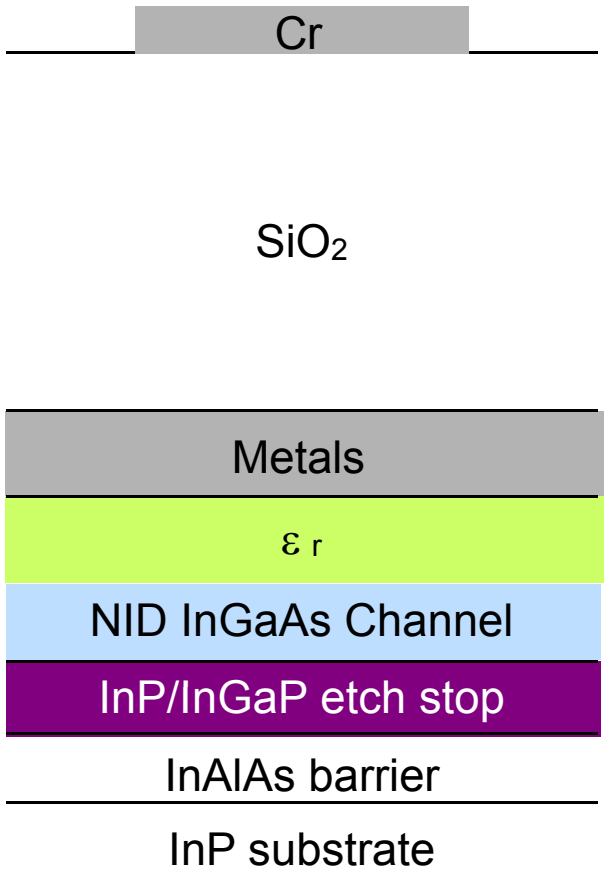
High-k first on pristine channel.

Tall gate stack.

Litho.

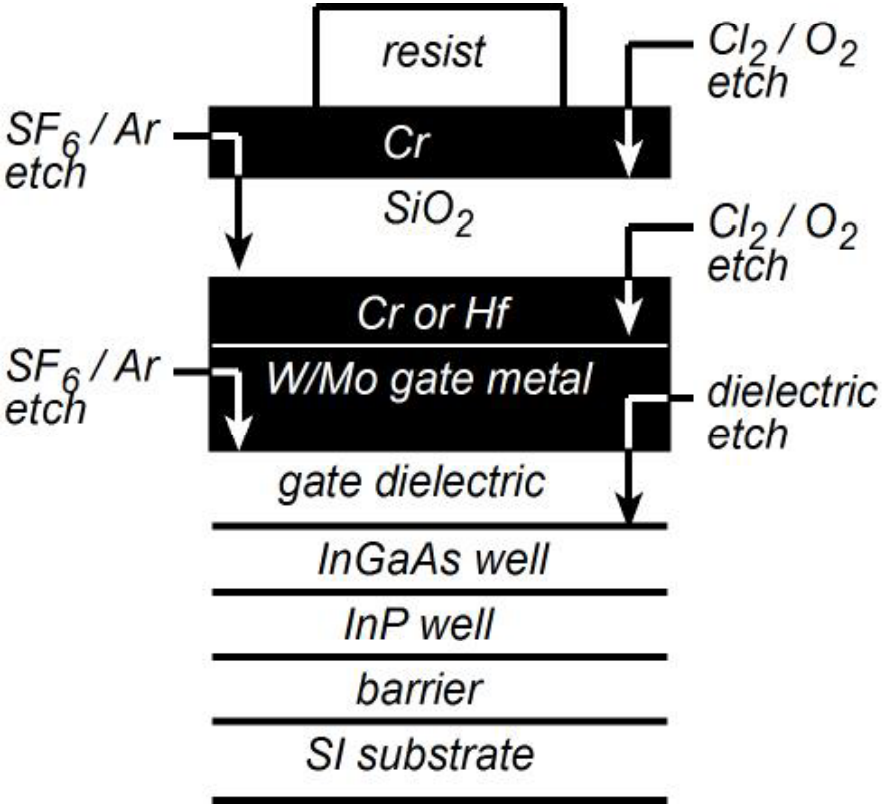
Selective etches to channel.

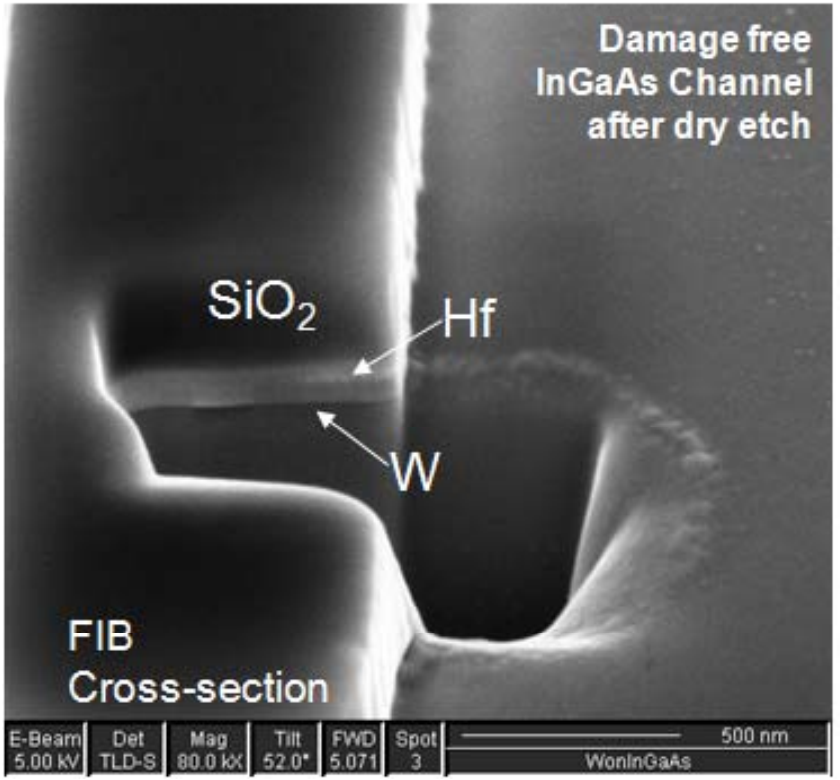
Critical etch process:
Stop on channel with no damage →



Gate Stack: Multiple Layers & Selective Etches

Key: stop etch before reaching dielectric, then gentle low-power etch to stop on dielectric

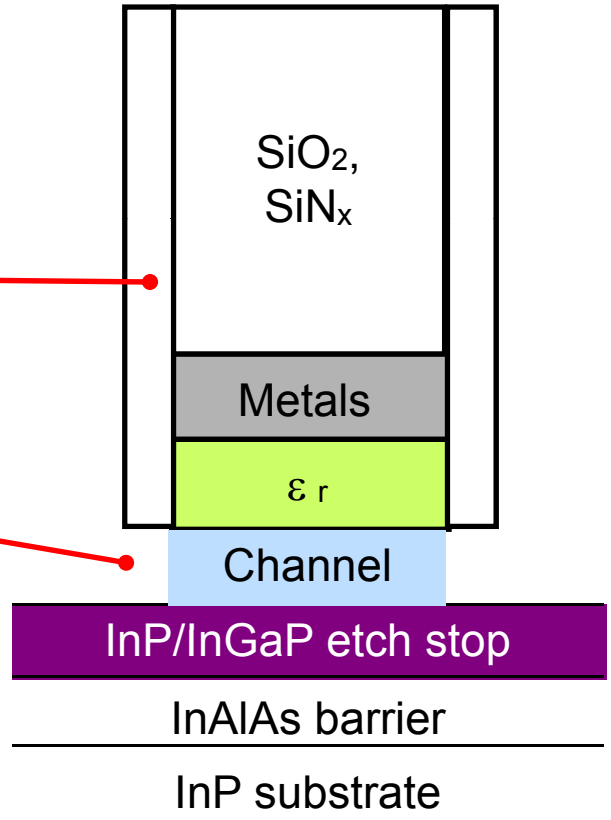




Process Flow: Sidewalls & Recess Etch

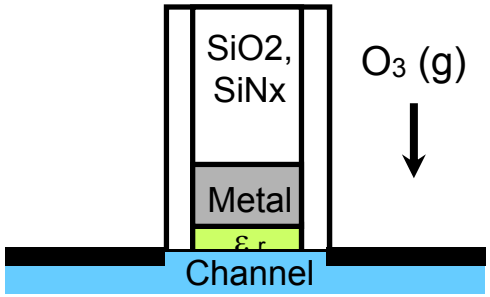
SiN_x or SiO_2 sidewalls
Encapsulate gate metals

Controlled recess etch
Slow facet planes
Not needed for depletion-mode FETs

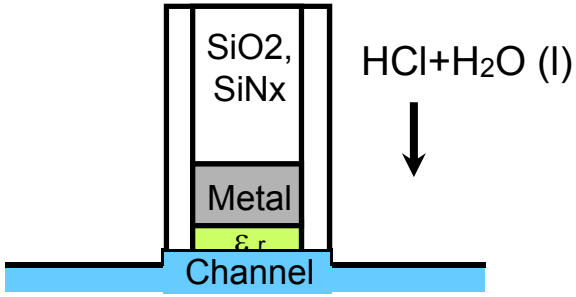


Surface Preparation Before Regrowth

UV-ozone (20 min)

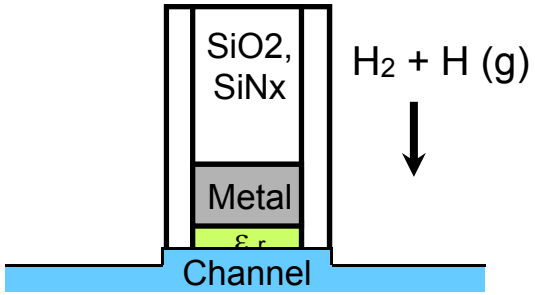


HCl:H_2O 1:10 etch (60 sec)
H_2O rinse, N_2 dry

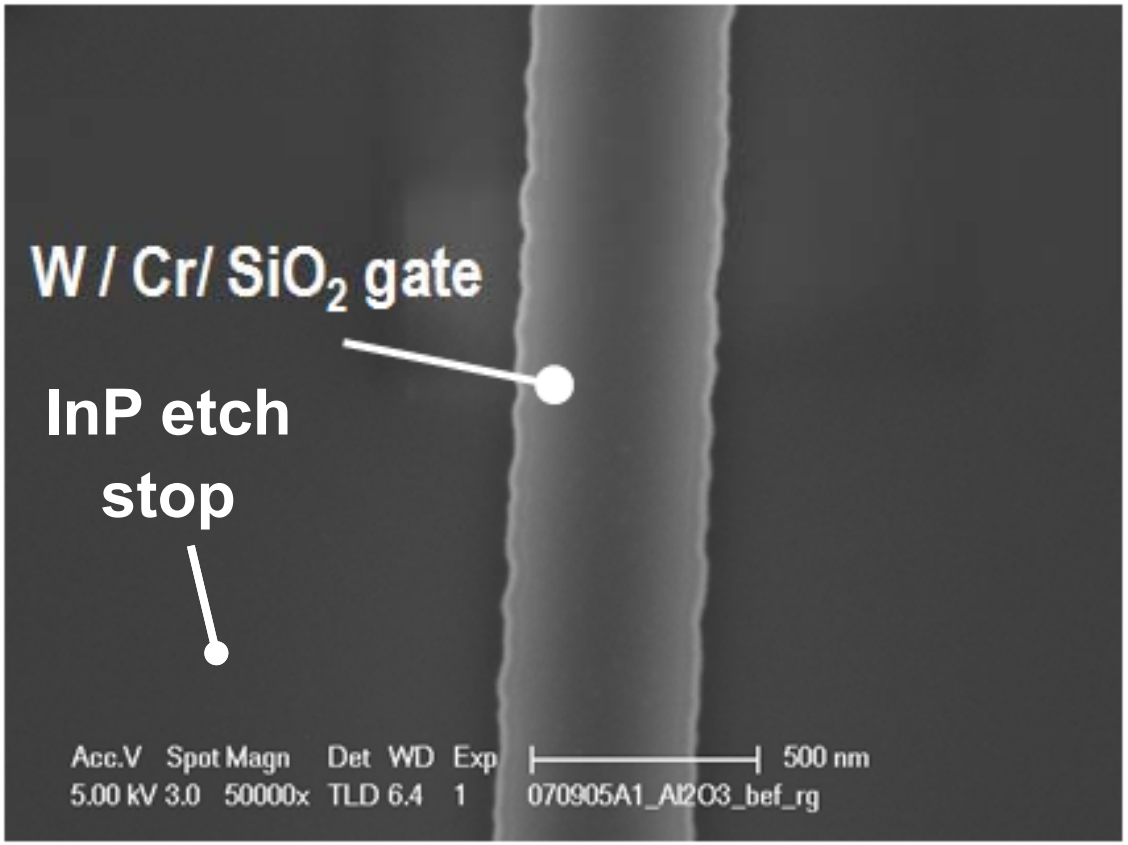


Bake under ultrahigh vacuum

Hydrogen cleaning
10^{-6} Torr, 30 min.,
400°C (InP) or 420°C (InGaAs)
Thermal deoxidation may work also.



Clean Surface Before Regrowth



Clean, undamaged surface after Al_2O_3 dielectric etch & InGaAs recess etch.

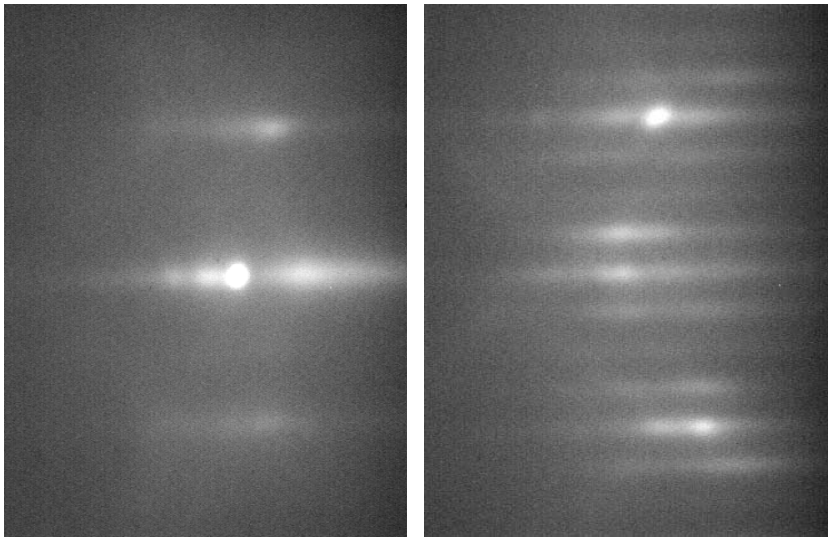
At Last: Regrowth & Metal

Regrow n++ InGaAs

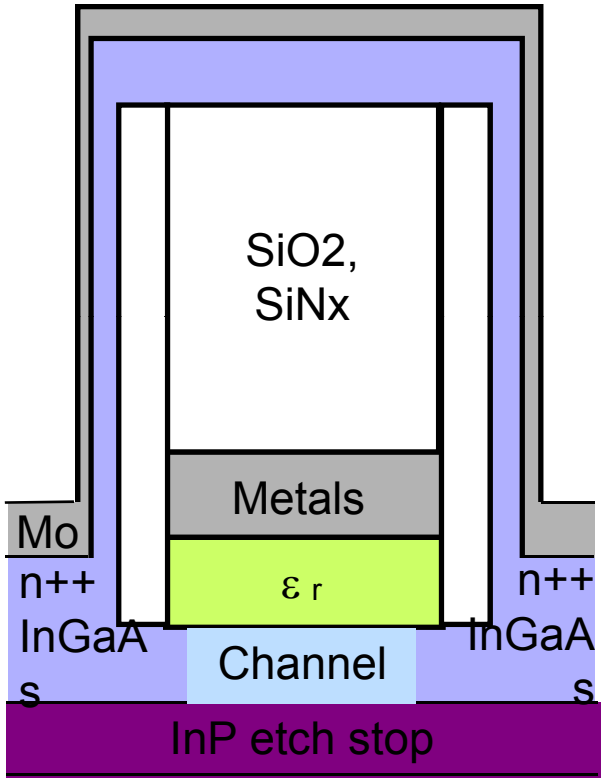
Doping: n~3.6x10^{19} cm^{-3} (Si~8x10^{19} cm^{-3})

V/III ratio=30

T_{sub} = 460°C



RHEED before growth



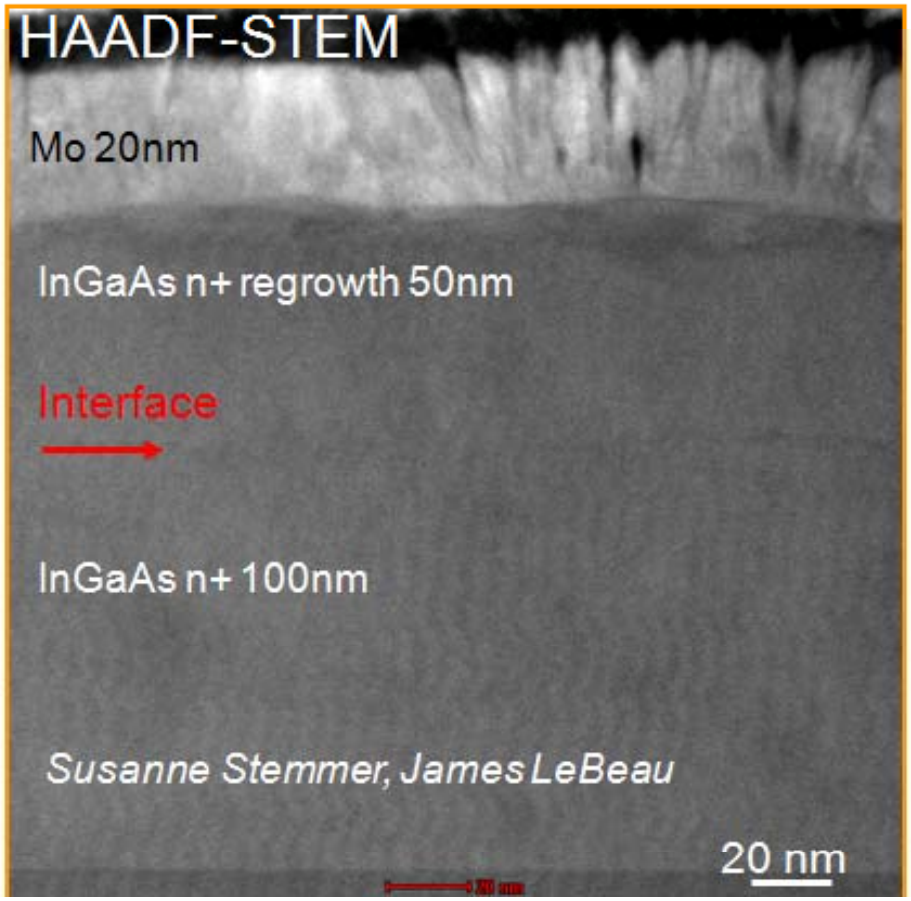
InAlAs barrier

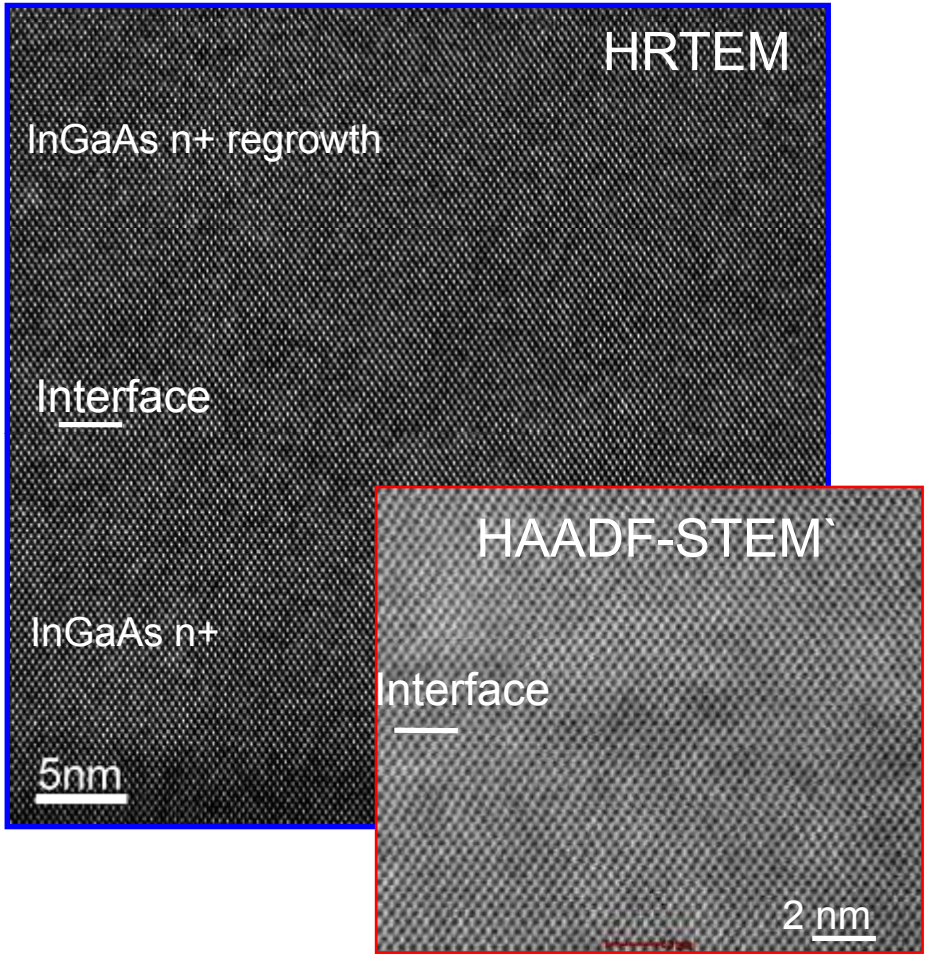
Blanket metallization:

Either in-situ Mo or ex-situ TiW

Singisetti APL, submitted, or Crook APL 2007

TEM of Regrowth: InGaAs on InGaAs





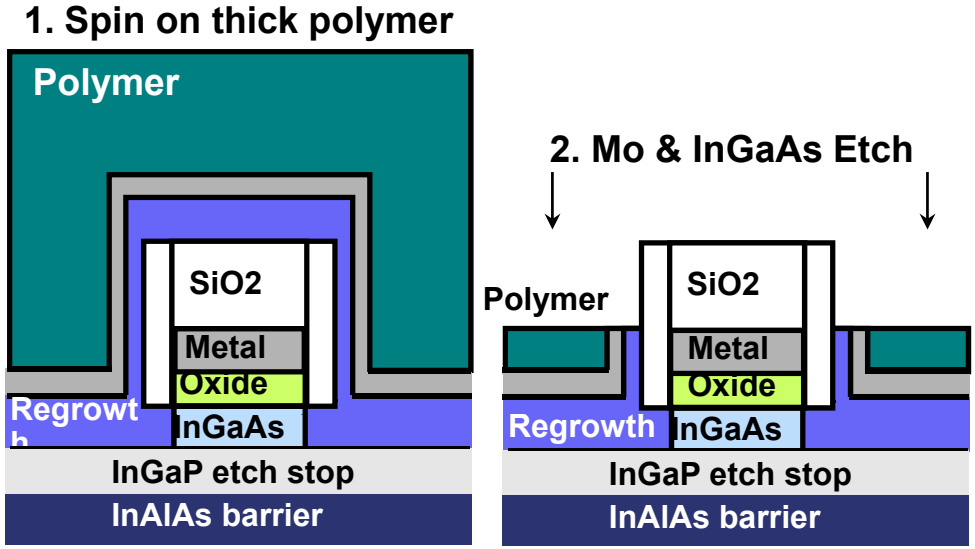
Regrowth on processed but unpatterned InGaAs.
No extended defects.

Removing Excess Overgrowth

Approach #1: Remove it

Height-selective etch

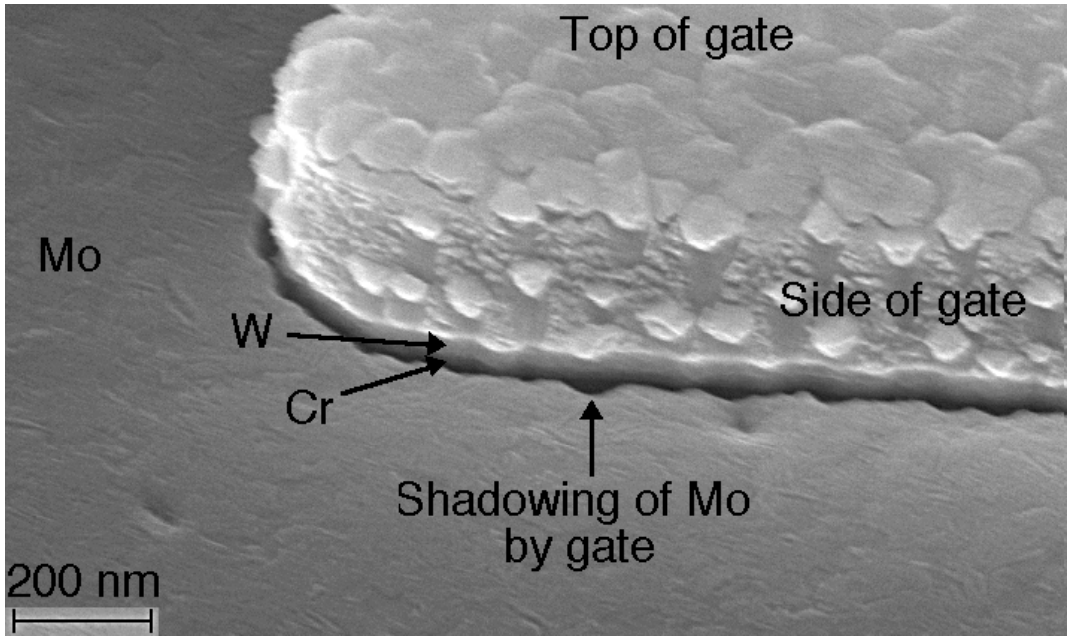
Wistey MBE 2008 & Burek JCG 2009



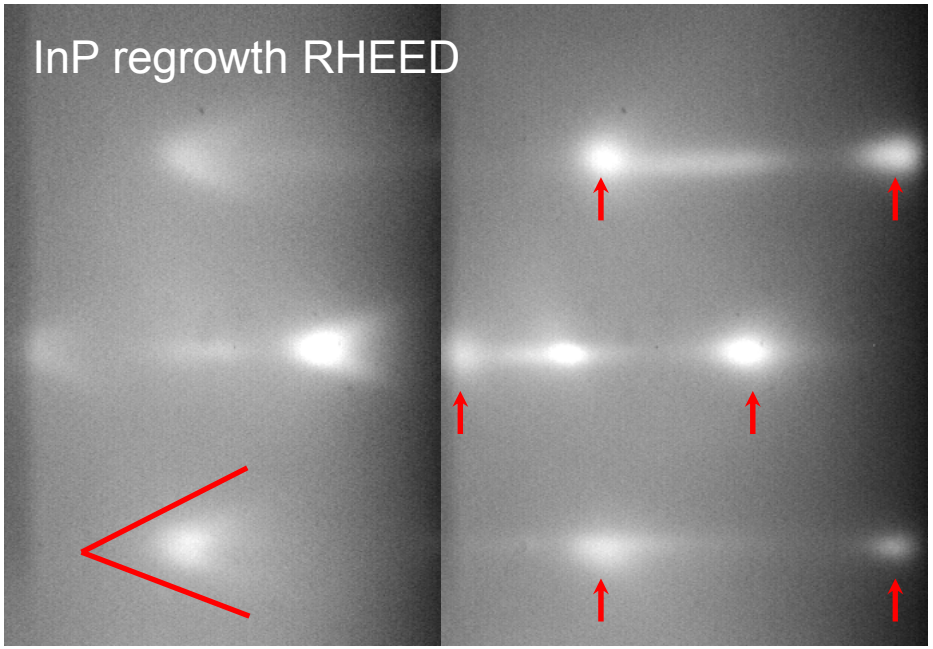
Approach #2: Don't Grow It

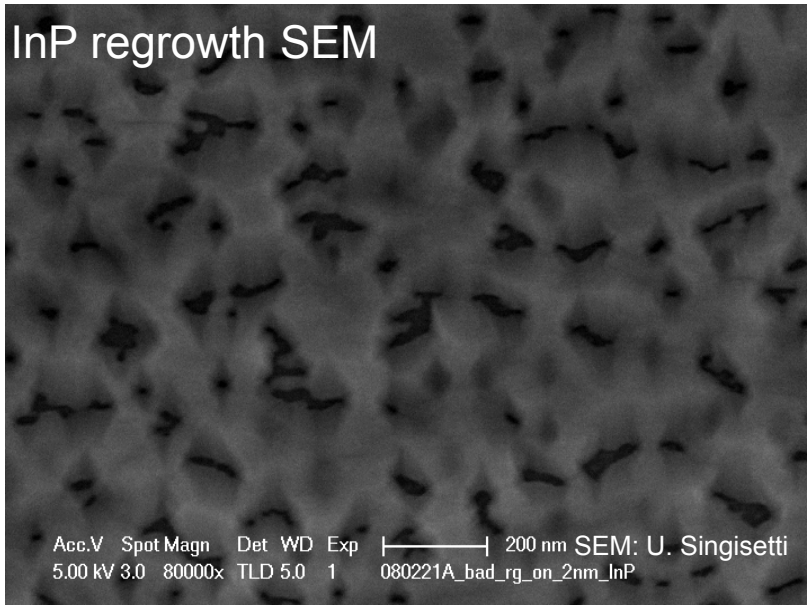
Quasi-Selective growth

Wistey EMC 2009

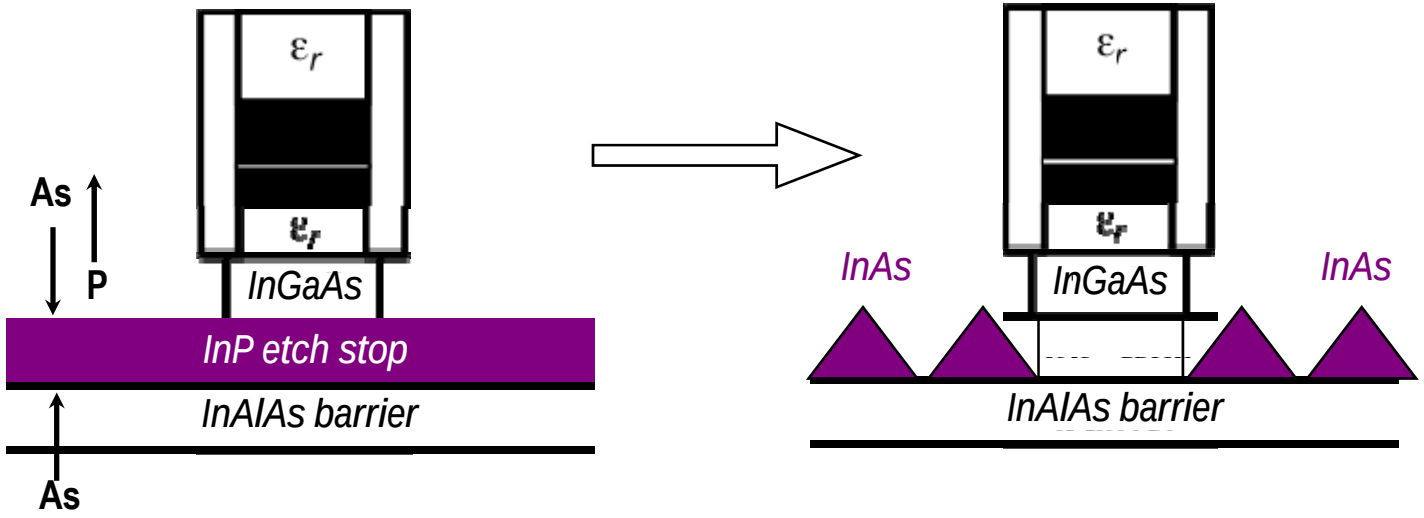


Regrowth on InP vs. InGaP





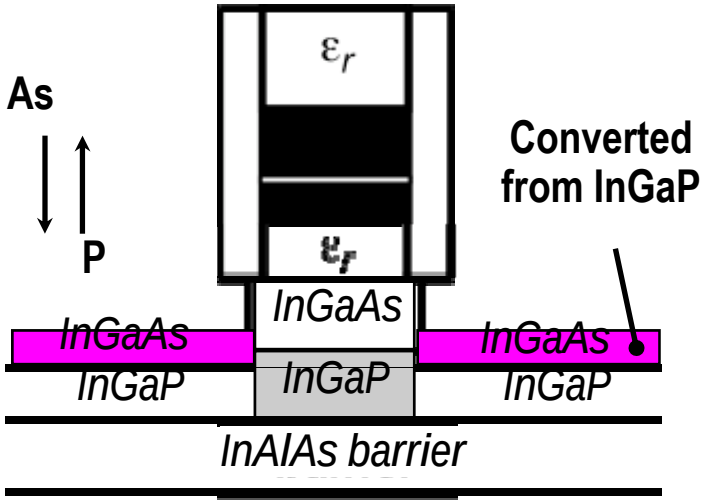
- Conversion of <6nm InP to InAs
- Strain relaxation

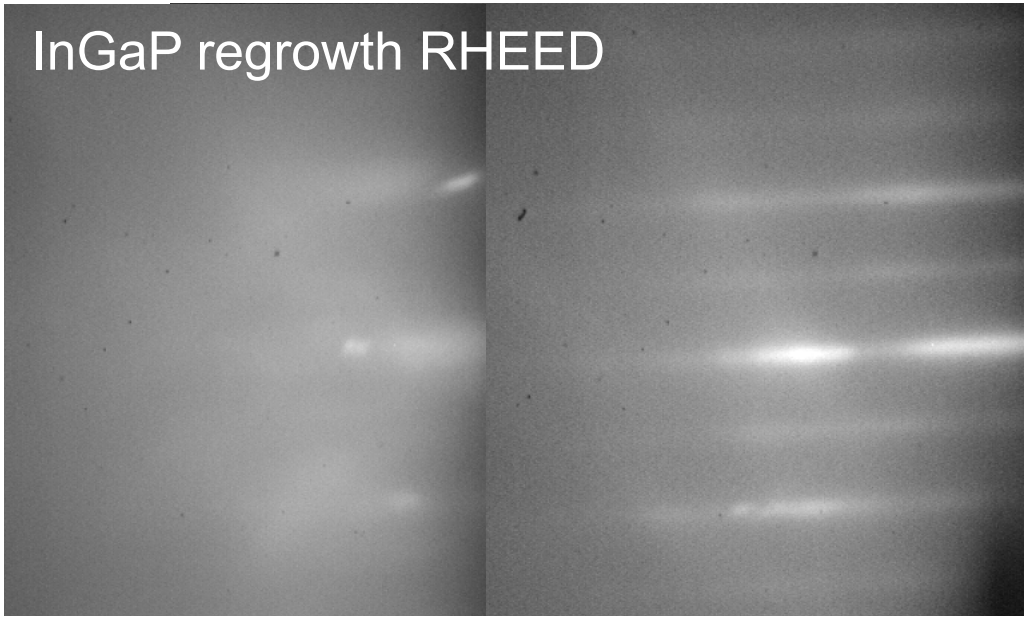


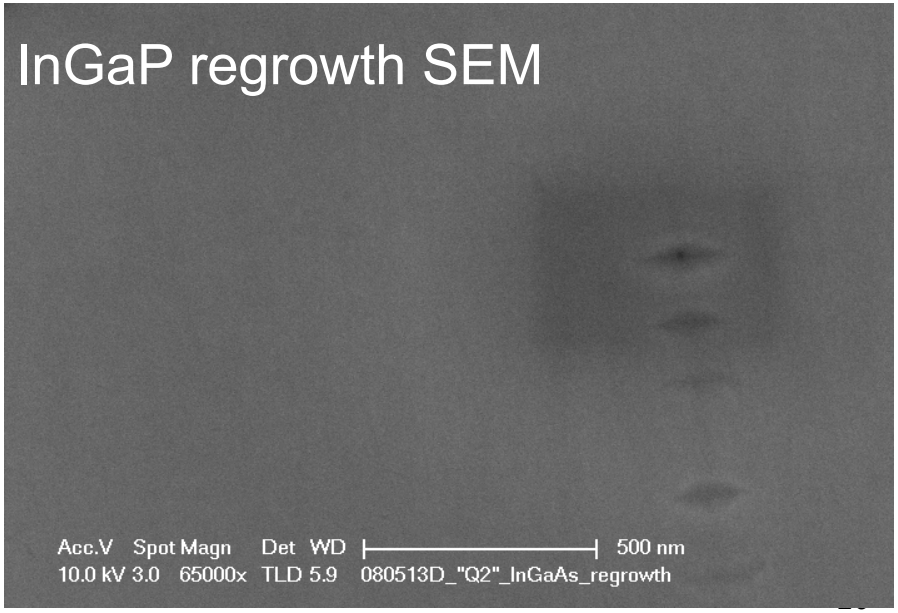
Regrowth on InGaP

- Replace InP with InGaP
- Converts to InGaAs (good!)
- Strain compensation

Wistey EMC 2008

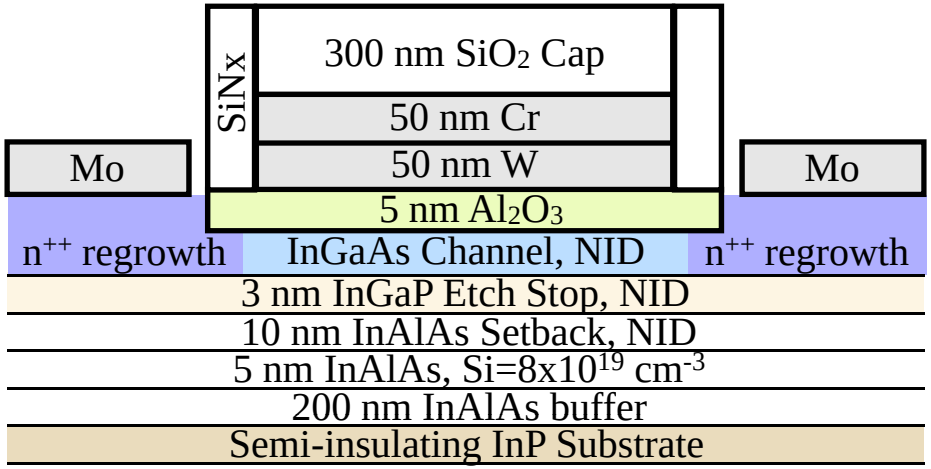


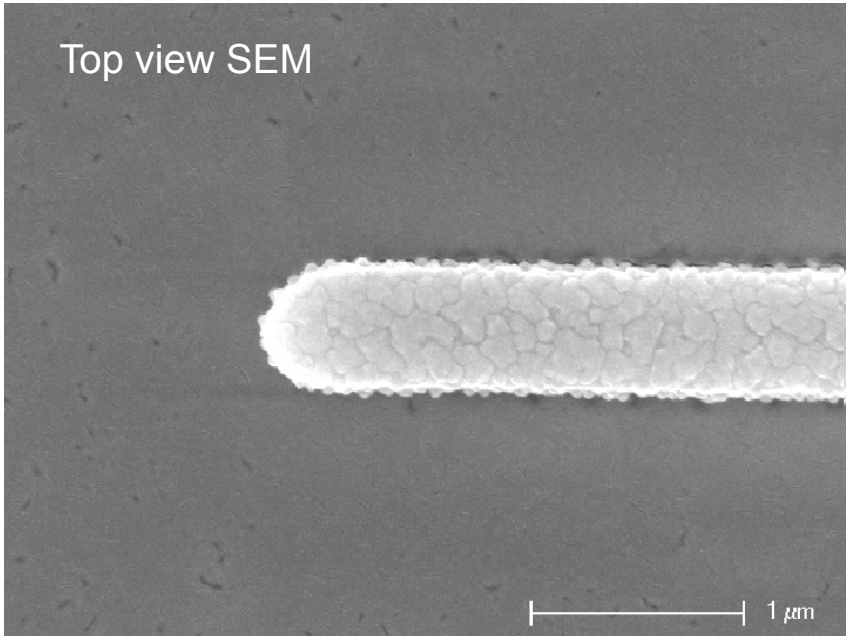


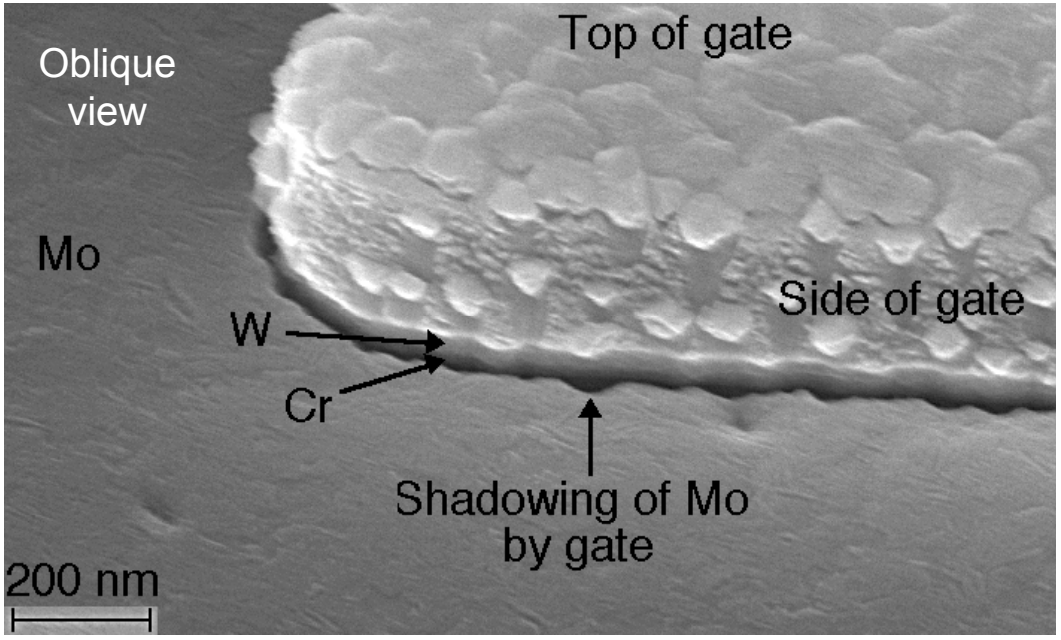


DEPLETION-MODE MOSFETS

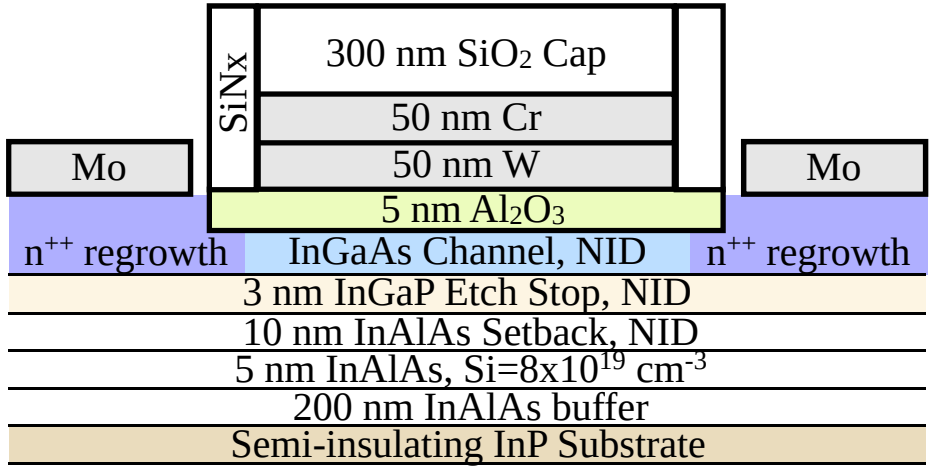
Scalable InGaAs MOSFETs



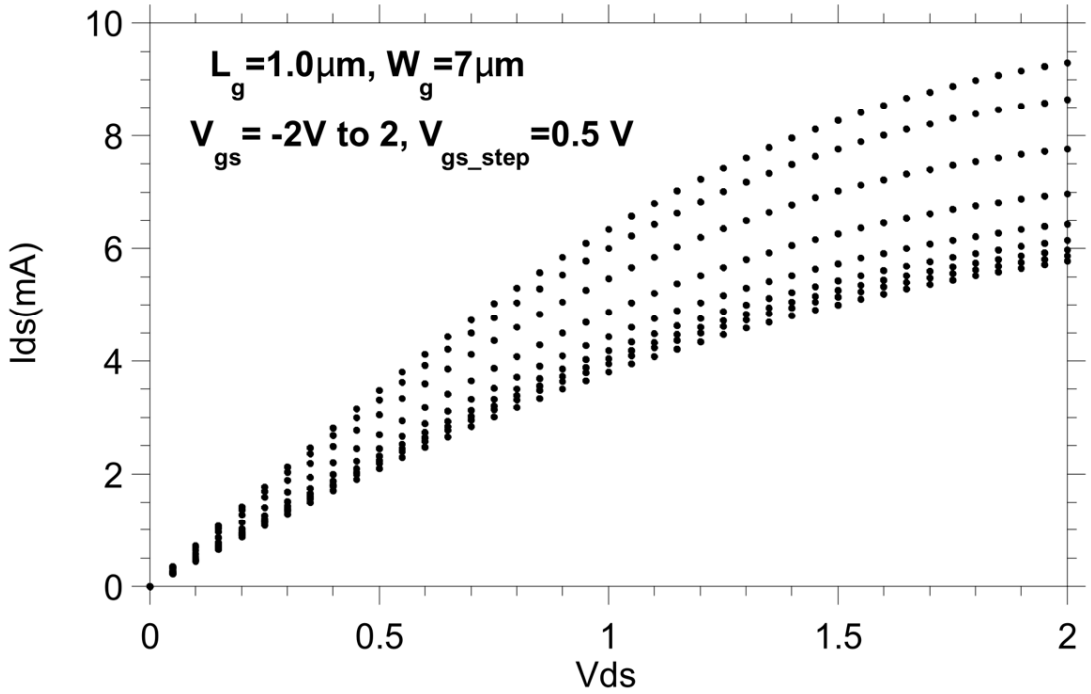


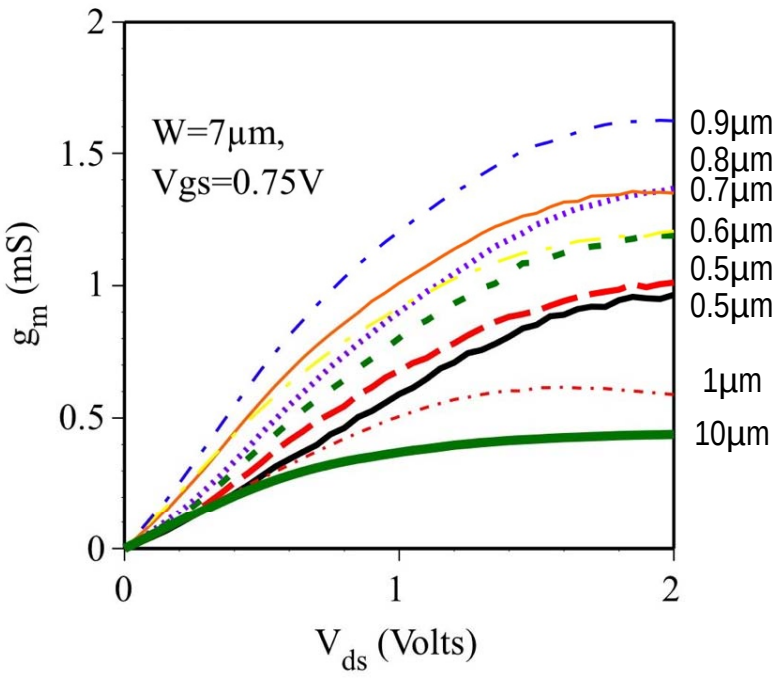


Scalable InGaAs MOSFETs

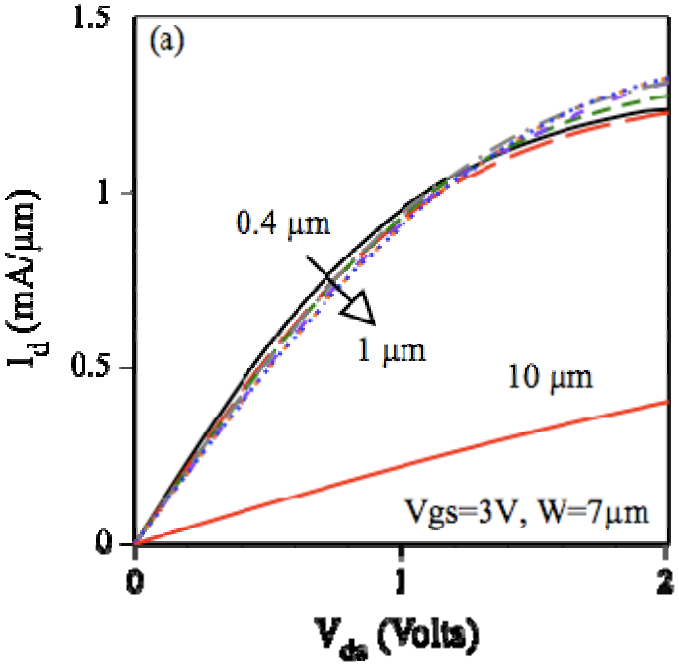


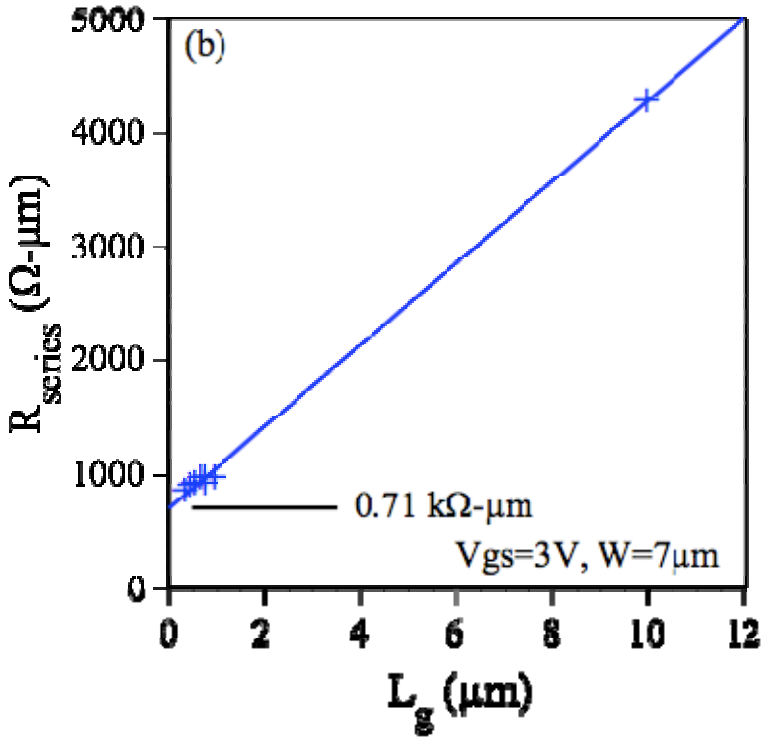
- Conservative doping design:
  - [Si] = 4×10^{13} cm^{-2}
  - Bulk n = 1×10^{13} cm^{-2} >> Dit
- Large setback + high doping = Can't turn off

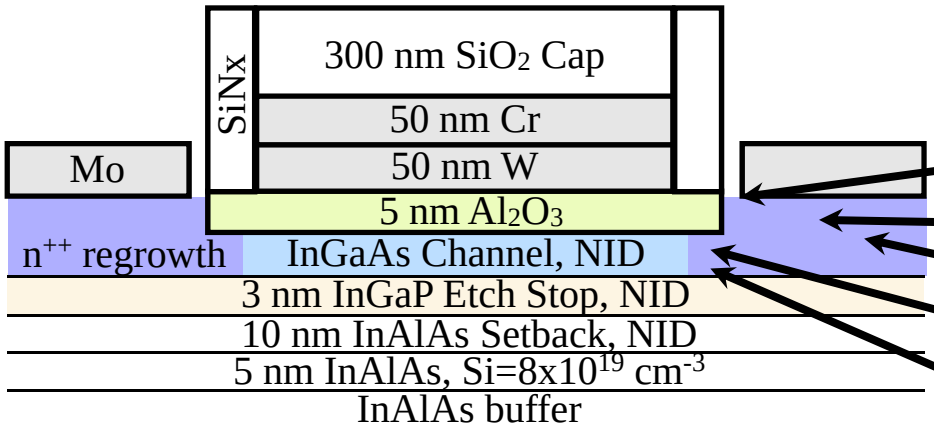




Series Resistance







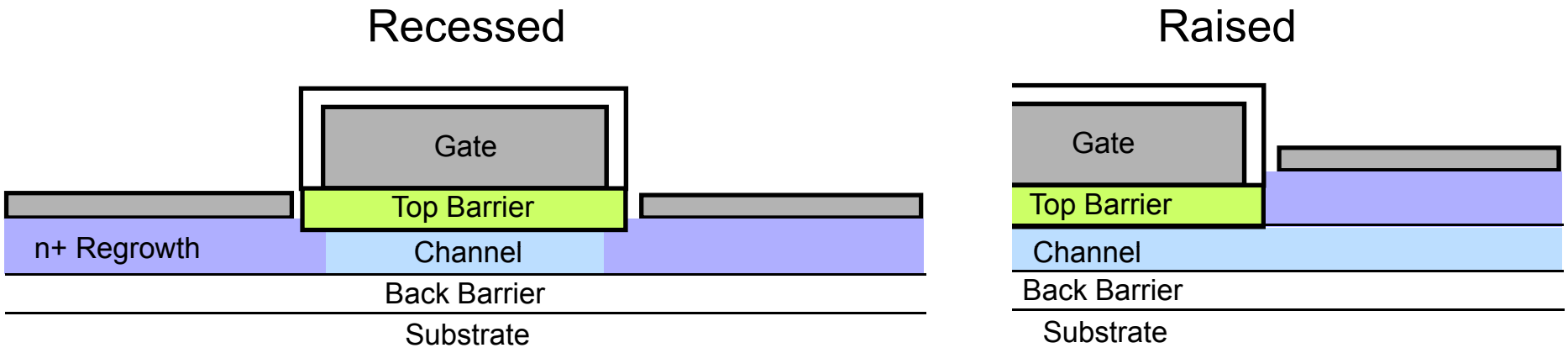
Possible causes:

- Poly nucleation at gate
- Thinning near gate
- Strain-induced dislocations
- Incomplete underfill
- Insufficient doping under sidewall

Now known to be a growth issue. See DRC & EMC 2009 for solution.

The Shape of Things to Come

Generalized Self-Aligned Regrowth Designs:



- **Self-aligned regrowth can also be used for:**
  - **GaN HEMTs (with Mishra group at UCSB)**
  - **GaAs pMOS FETs**
  - **InGaAs HBTs and HEMTs**
  - **All high speed III-V electronics**

Conclusions

- Scaled III-V CMOS requires more than reduced dimensions
- InGaAs offers a high velocity channel, high mobility access
- Self-aligned regrowth: a roadmap for scalable III-V FETs
  - Provides III-V's with a salicide equivalent
  - Can improve GaN and GaAs FETs too
- DFETs show peak g_m = 0.24mS/μm
- High resistance (a growth problem) limited FET performance

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- Palmstrøm Group (UCSB): Erdem Arkun, Chris Palmstrøm
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- UCSB Nanofab: Brian Thibeault, NSF

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