0.37 mS/μm $In_{0.53}Ga_{0.47}As$ MOSFET with 5 nm channel and self-aligned epitaxial raised source/drain

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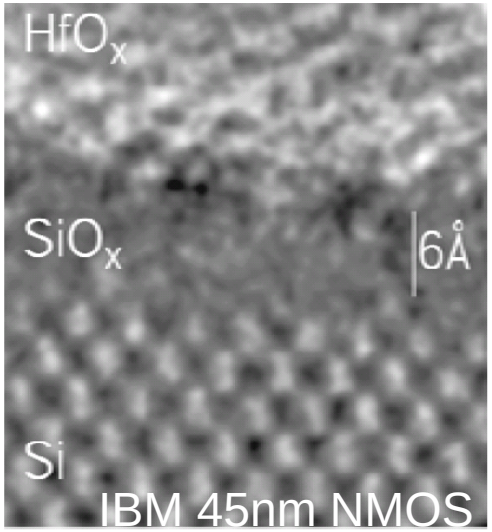
Outline

- **Motivation: III-V MOSFETs**
- **Approach: Self-aligned source/drain by MBE regrowth**
- **FET and contacts Results**
- **Conclusion and future work**

Why III-V MOSFETs

Silicon MOSFETs:

Gate oxide may limit <16 nm scaling



Narayan *et al*, VLSI 2006

$$I_d / W_g \sim c_{ox}(V_g - V_{th})v_{inj}$$

$$I_d / Q_{transit} \sim v_{inj} / L_g$$

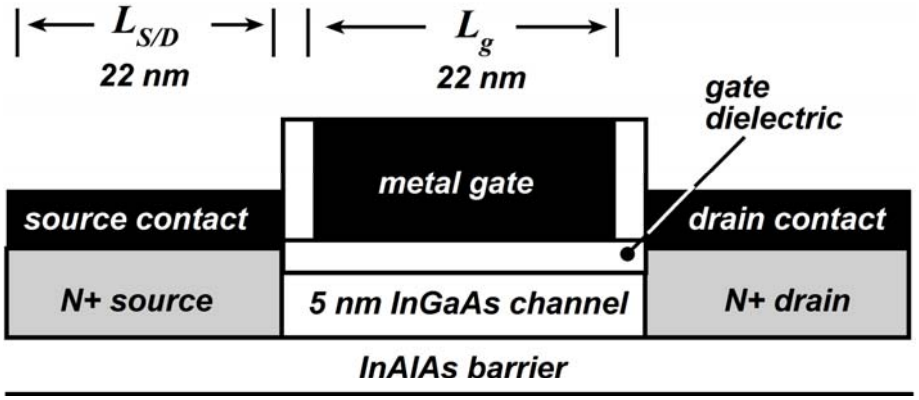
Alternative: $In_{0.53}Ga_{0.47}As$ channel MOSFETs

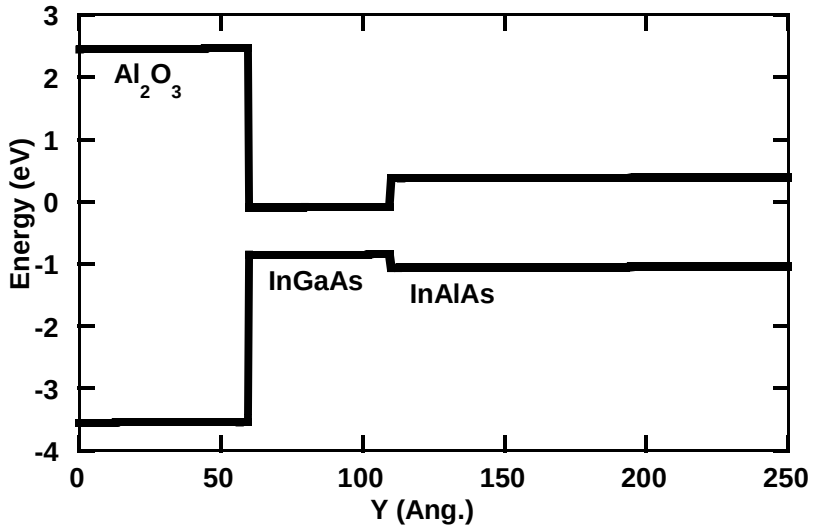
low m* (0.041 m_o) → high injection velocity (~ 2×10^7 cm/s)*

→ increase drive current, decreased CV/I

* Enoki *et al* , EDL 1990

Target device structure



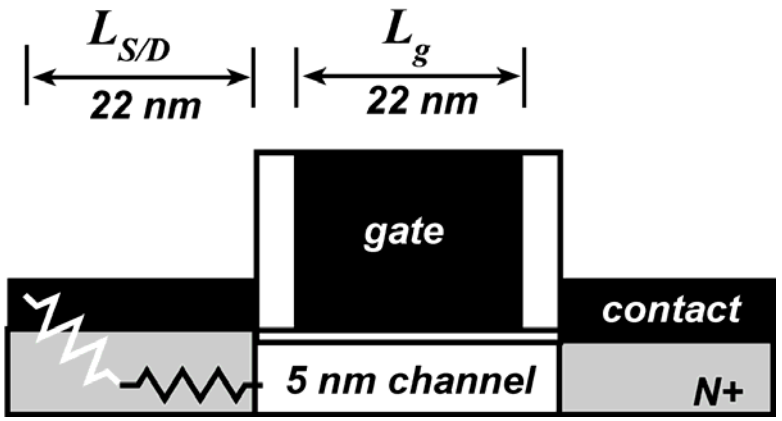


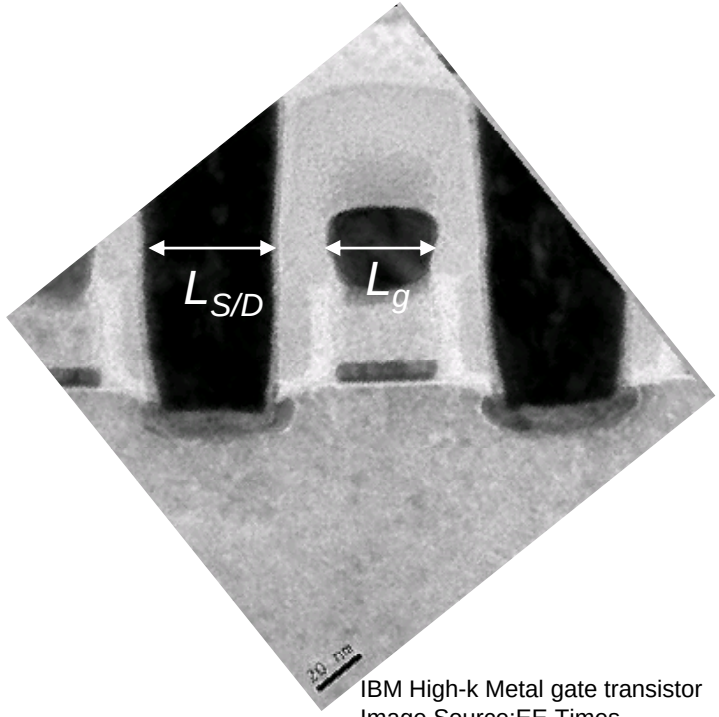
Target 22 nm gate length

Control of short-channel effects → vertical scaling
- *1 nm EOT: thin gate dielectric, surface-channel device*
- *5 nm quantum well thickness*
- *<5 nm deep source / drain regions*

~3 mA/μm target drive current → low access resistance
- *self-aligned, low resisitivity source / drain contacts*
- *self-aligned N+ source / drain regions with high doping*

22 nm InGaAs MOSFET: source resistance



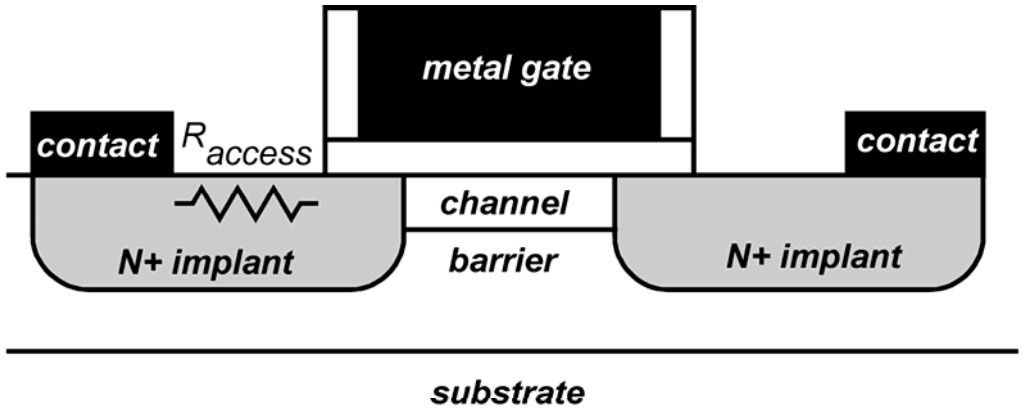


IBM High-k Metal gate transistor
Image Source:EE Times

$$I_d = \frac{I_{di}}{1 + g_{mi} \cdot R_s} \qquad R_s = \frac{\rho_c}{W_g L_{S/D}} + \frac{\rho_{sheet} L_{S/D}}{2W_g}$$

- Source access resistance degrades I_d and g_m
- IC Package density : $L_{S/D} \sim L_g = 22$ nm → ρ_c must be low
- Need low sheet resistance in thin ~5 nm N+ layer
- Design targets: ρ_c ~1 Ω–μm^2, ρ_{sheet} ~ 400 Ω

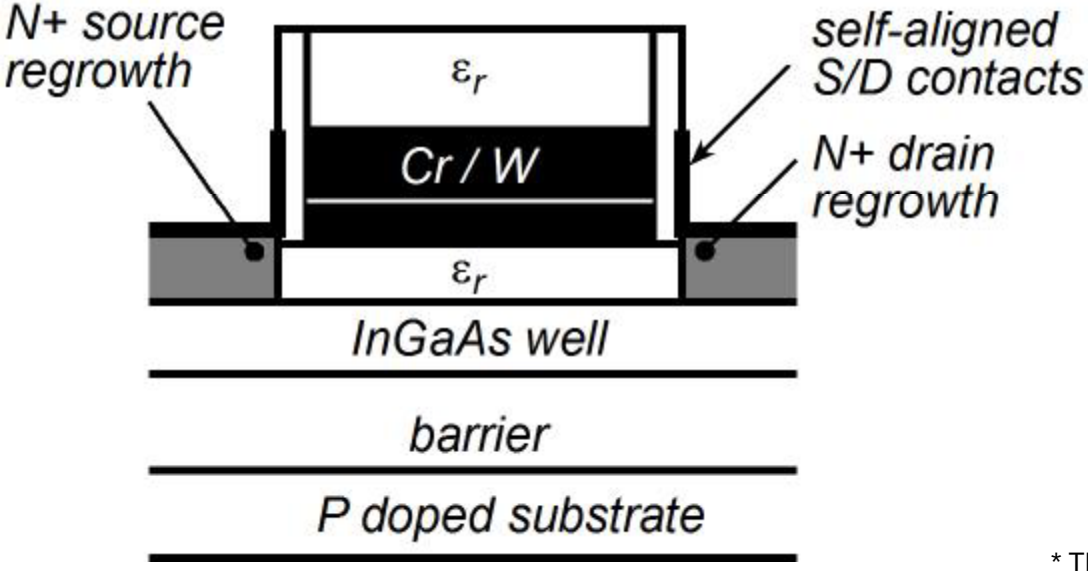
22nm ion implanted InGaAs MOSFET

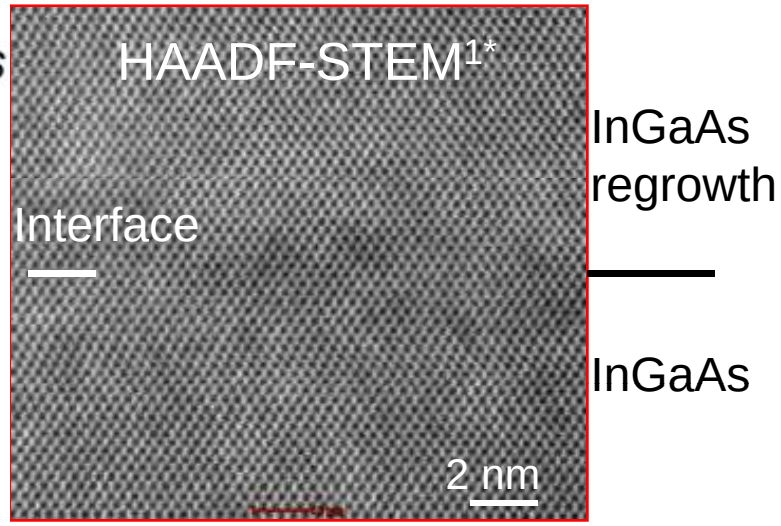


Key Technological Challenges

- Shallow junctions (~ 5 nm), high (~5×10^{19} cm^{-3}) doping
- Doping abruptness (~ 1 nm/decade)
- Lateral Straggle (~ 5 nm)
- Deep junctions would lead to degraded short channel effects

InGaAs MOSFET with raised source/drain by regrowth





* TEM by J. Cagnon, Susanne Stemmer Group, UCSB

Self-aligned source/drain defined by MBE regrowth[1]

Self-aligned in-situ Mo contacts[2]

Process flow & dimensions selected for 22 nm L_g design; present devices @ 200 nm gate length

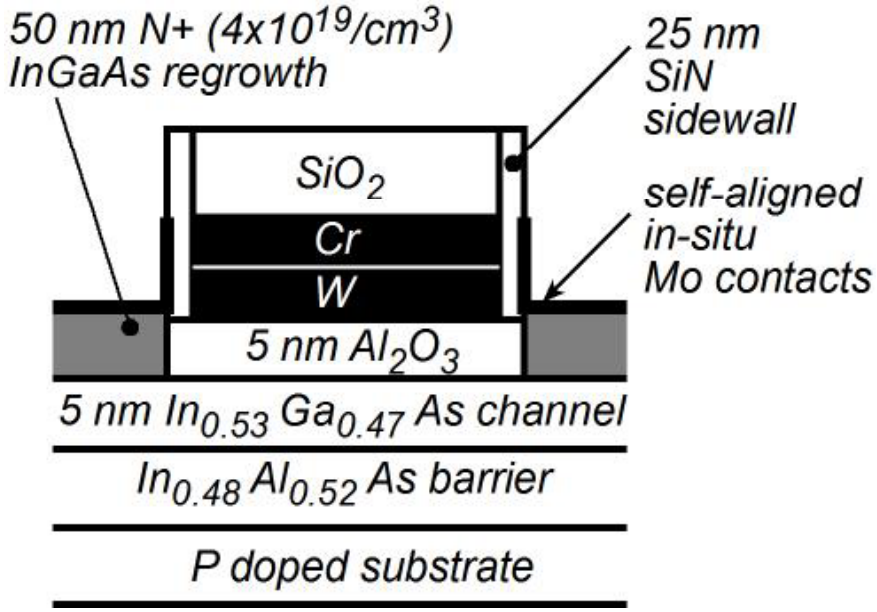
[1]Wistey, EMC 2008
[2]Baraskar, EMC 2009

Regrown S/D process: key features

Self-aligned <u>& low resistivity</u>

...source / drain N+ regions

...source / drain metal contacts



Vertical S/D doping profile set by MBE

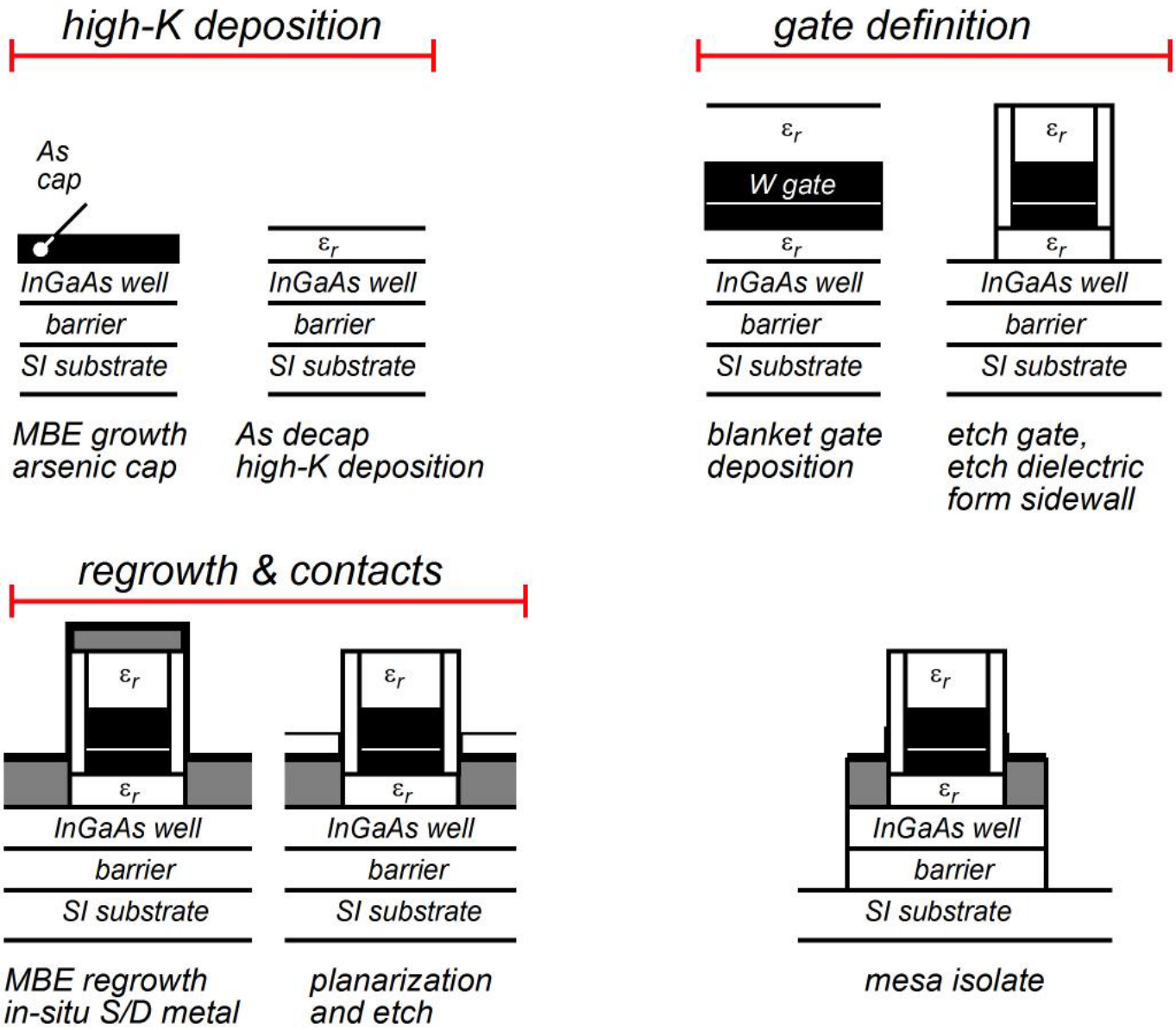
abrupt on ~ 1 nm scale

Gate-first

gate dielectric formed after MBE growth

uncontaminated / undamaged surface

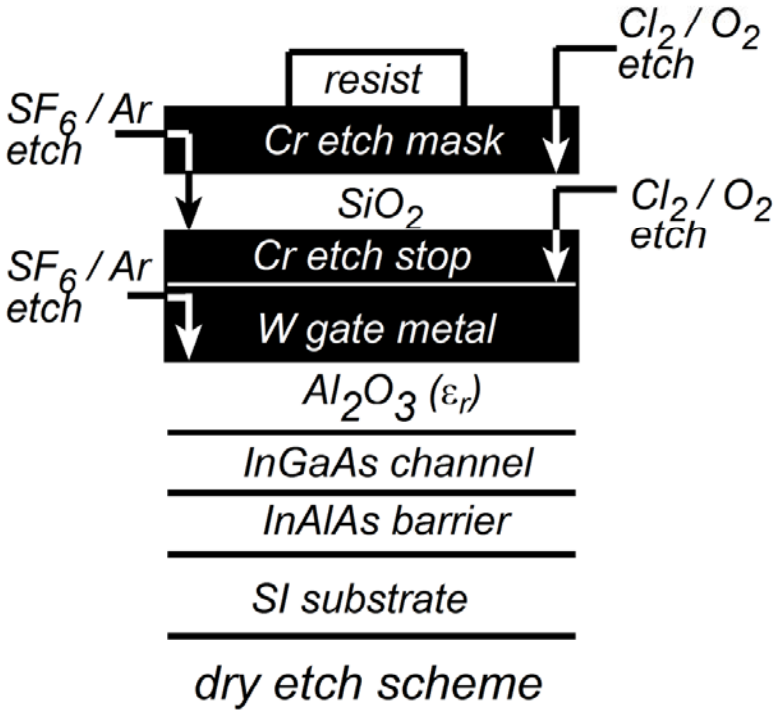
Process flow*

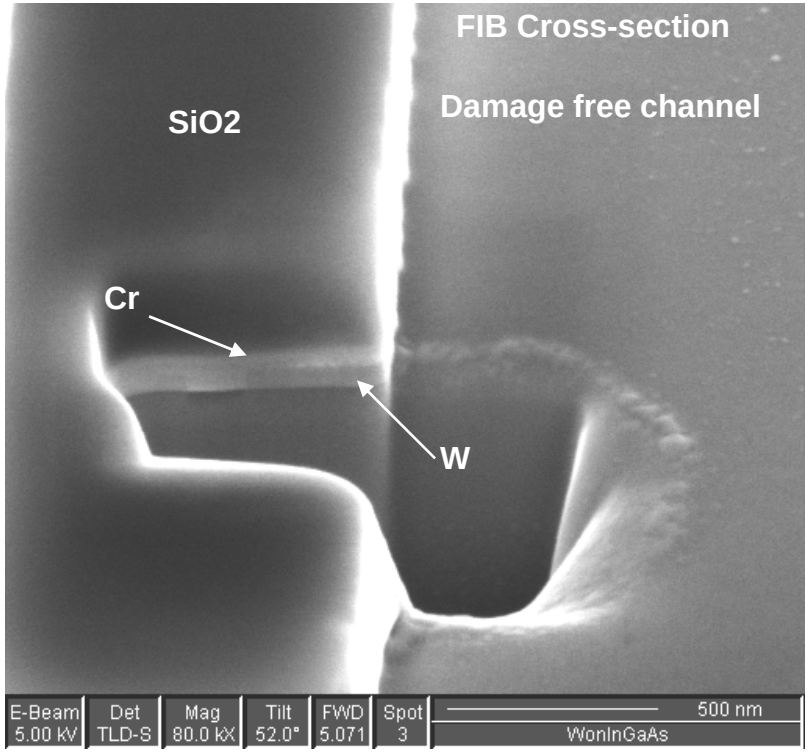


* Singisetti *et al*; Physica Status Solidi C, vol. 6, pp. 1394,2009

Key challenge in S/D process: gate stack etch

Requirement: avoid damaging semiconductor surface:
Approach: Gate stack with multiple selective etches*



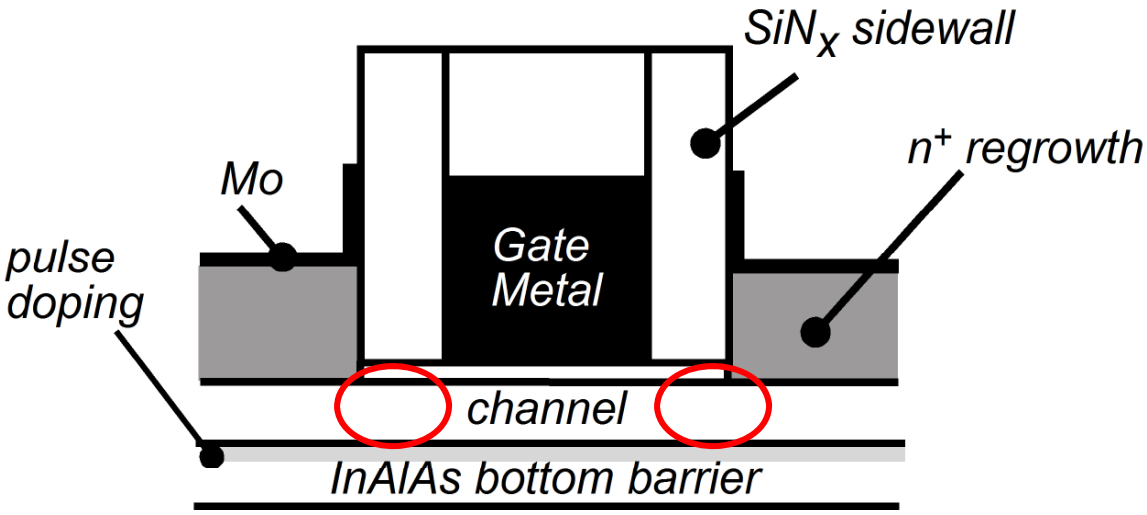


Process scalable to sub-100 nm gate lengths

* Singisetti *et al*; Physica Status Solidi C, vol. 6, pp. 1394,2009

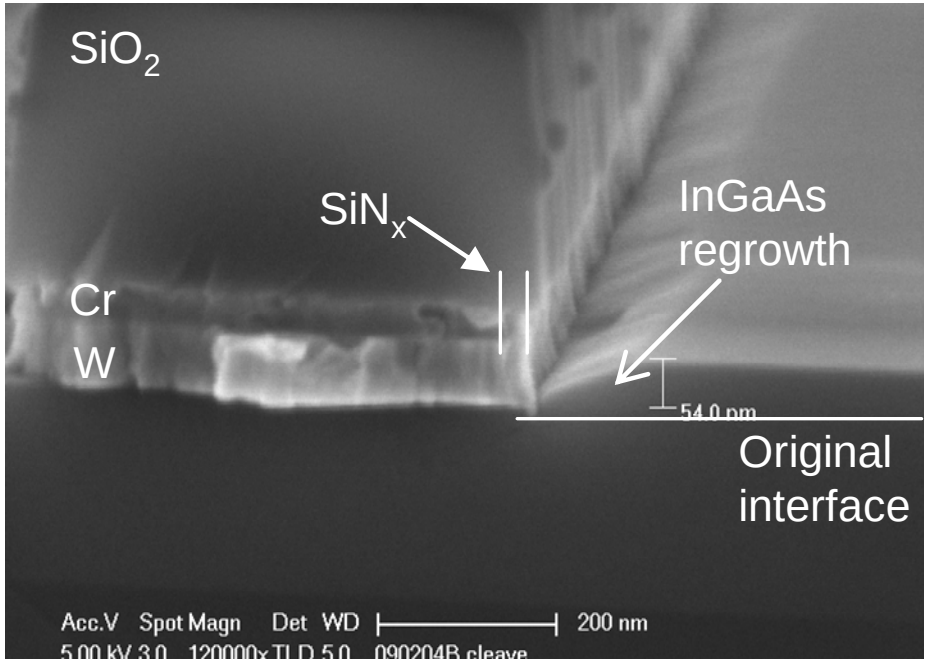
Key challenge in S/D process: dielectric sidewall

Sidewall must be kept thin: avoid carrier depletion, source starvation.

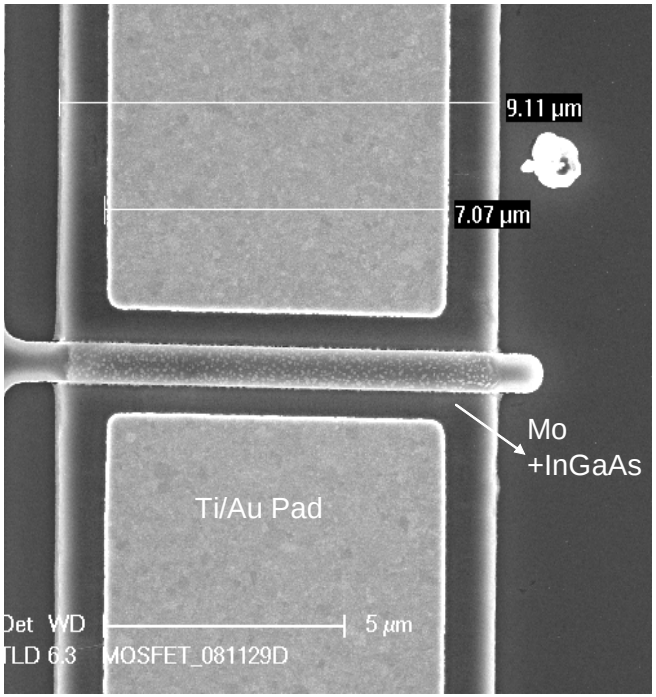


- Target < 15 nm sidewall in 22 nm L_g device
- 20-25 nm SiN_x thick sidewalls in present devices
- Pulse doping in the barrier: compensate for carrier depletion from D_{it}

MOSFET SEMs



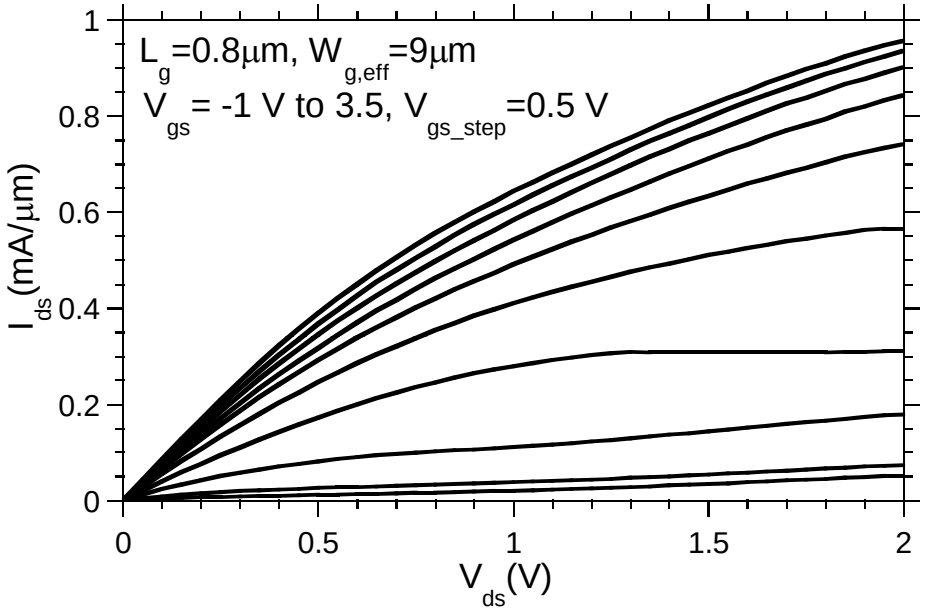
Cross-section after regrowth, but before Mo deposition

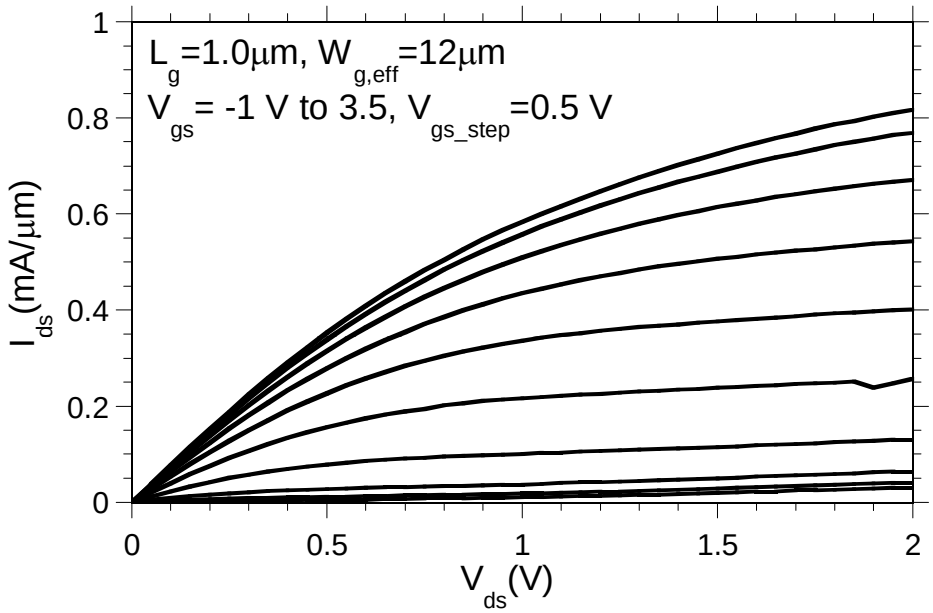


Top view of completed device

MOSFET characteristics

4.7 nm Al_2O_3, 1×10^{13} cm^{-2} pulse doping

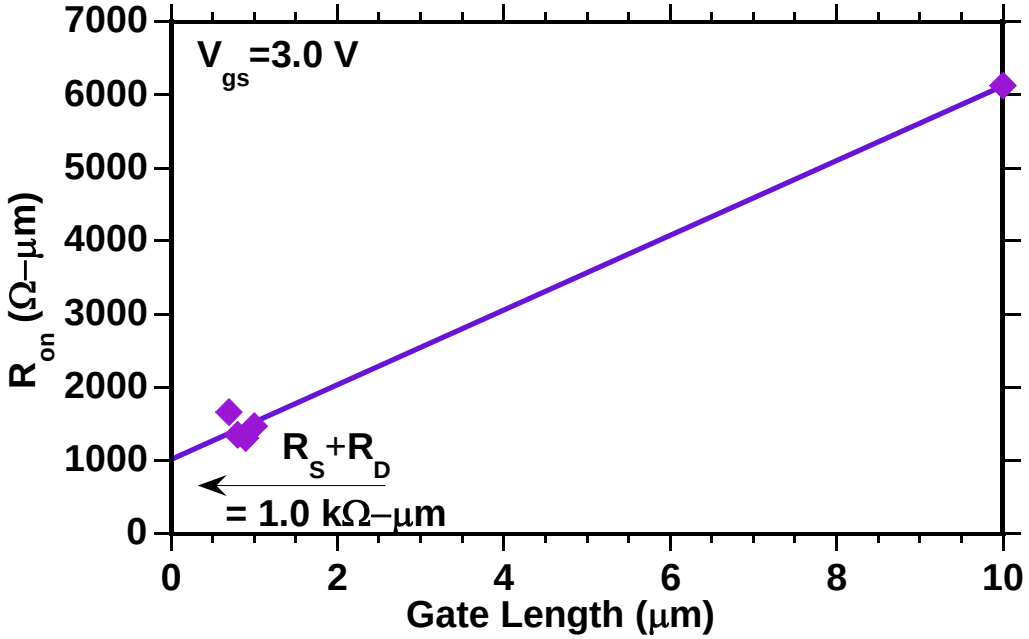




- Maximum Drive current (I_d): 0.95 mA/μm
- Peak transconductance (g_m): 0.37 mS/μm

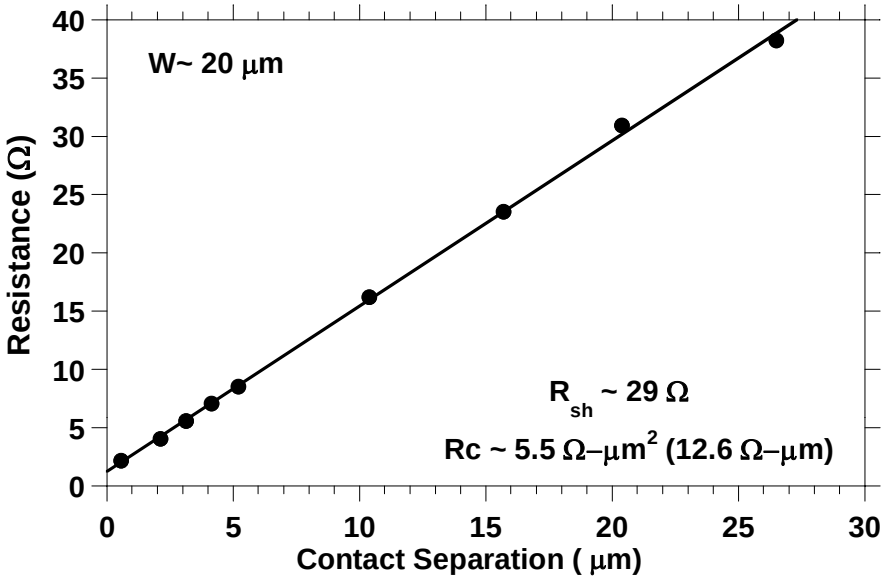
I_d and g_m below expected values

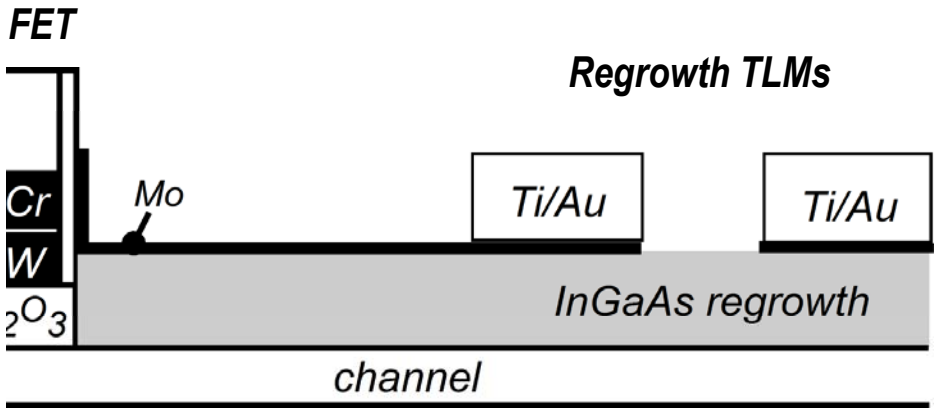
FET source resistance



- *Series resistance estimated by extrapolating R_{on} to zero gate length*
- *Source access resistance ~ 500 Ω–μm*

Source resistance : regrowth TLMs

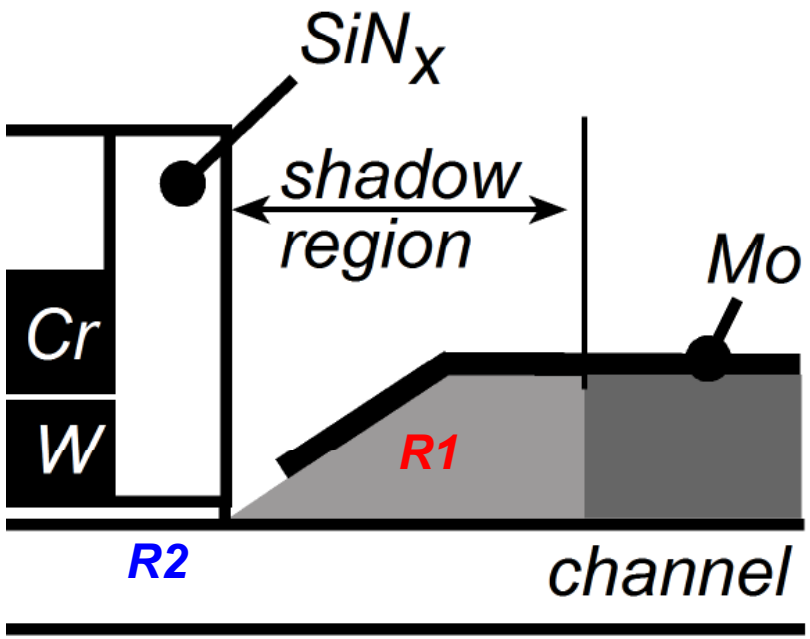


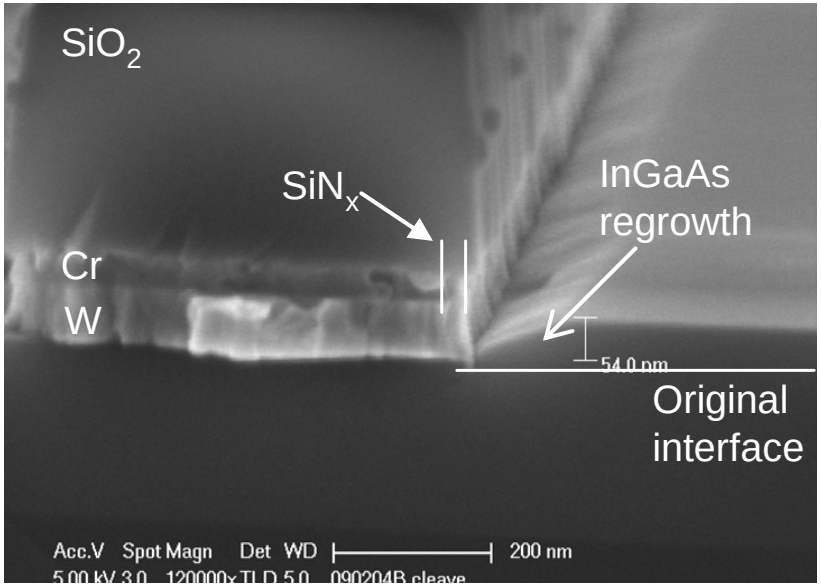


- TLMs fabricated on the regrowth far away from the gate
- Regrowth sheet resistance ~ 29 Ω
- Mo/InGaAs contact resistance ~ 5.5 Ω–μm² (12.6 Ω–μm)

TLM data does not explain 500 Ω–μm observed FET source resistance

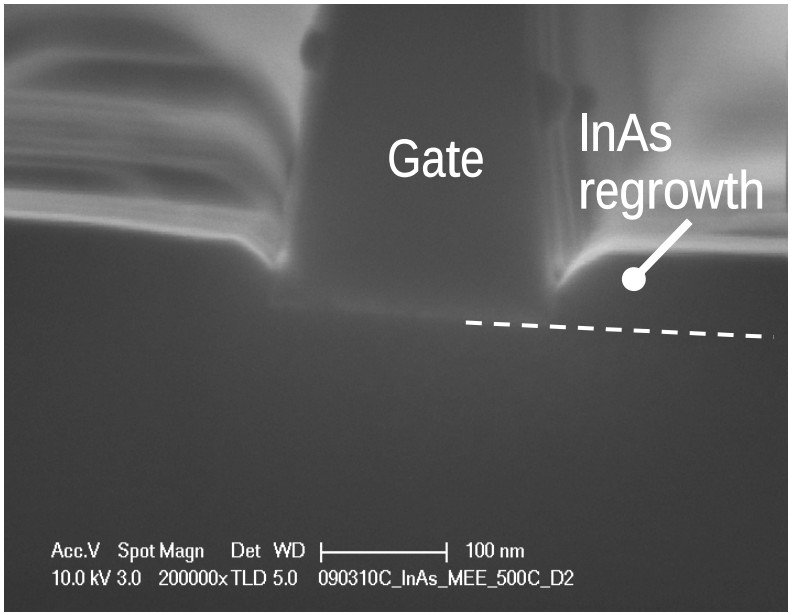
Source resistance: electron depletion near gate

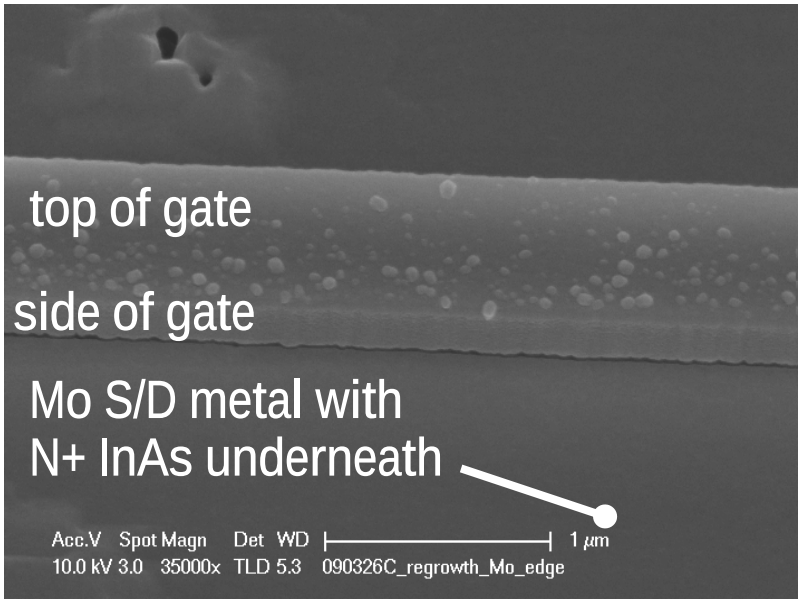




- *Electron depletion in regrowth shadow region (R_1)*
- *Electron depletion in the channel under SiN_x sidewalls (R_2)*

InAs source/drain regrowth





Improved InAs regrowth with low As flux for uniform filling[1]

InAs less susceptible to electron depletion: Fermi pinning above E_c[2]

[1] Wistey *et al*, EMC 2009
Wistey *et al* NAMBE 2009.
[2]Bhargava *et al* , APL 1997

Conclusion

- *Self-aligned raised source/drain for scaled channel (5nm)*
- *D-FETs: peak I_d = 0.95 mA/μm, and peak g_m =0.37 mS/μm*
- *InAs Source/Drain E-FETs*[1]
- *Next:*
  scale to ~50 nm L_g
  gate dielectric quality

This work was supported by Semiconductor Research Corporation under the Non-classical CMOS Research Program

[1]Singisetti *et al,* EDL submitted