Improved Migration-Enhanced Epitaxy for Self-Aligned InGaAs Devices

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Outline: Channels for Future CMOS

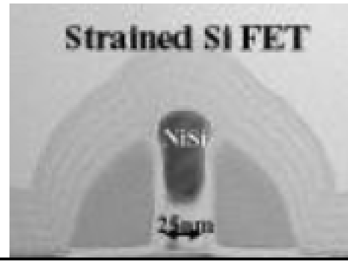
- Motivation for Self-Aligned Regrowth
- Facets, Gaps, Arsenic Flux and MEE
- Si doping and MEE
- Scalable III-V MOSFETs
- The Shape of Things to Come

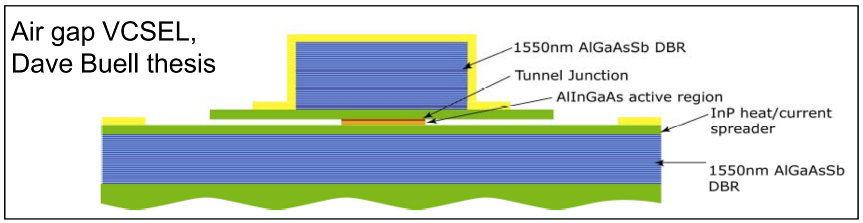
Motivation for Self-Aligned Regrowth

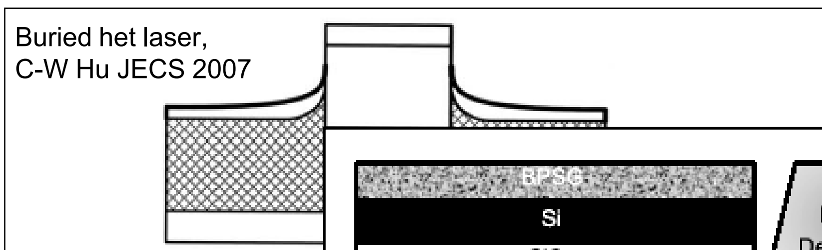
Blanket layers

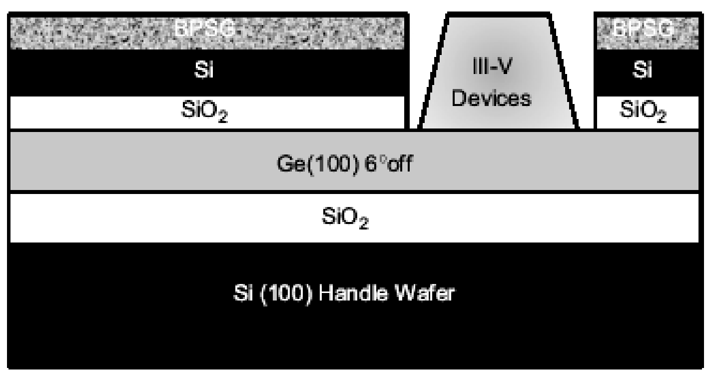
AlGaAs
GaAs
InGaAs
GaAs
AlGaAs
GaAs

?

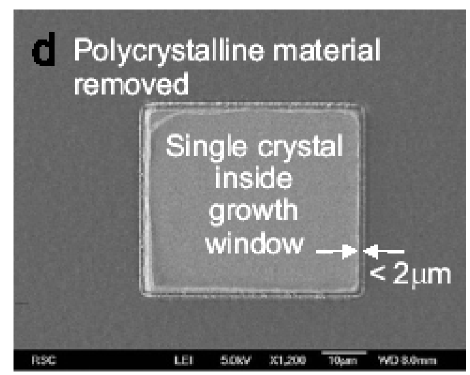








W.K. Liu et al., J. Crystal Growth v. 311, p. 1979 (2009)



- **3D nanofabrication**
- **Device properties**
  - **Heat transfer**
  - **Contacts**
  - **Current blocking**
- **Integration: III-V's on Si**
  - **Heteroepitaxy**
  - **Selective area growth**
- **And III-V MOSFETs...**

Motivation for Regrowth: Scalable III-V FETs

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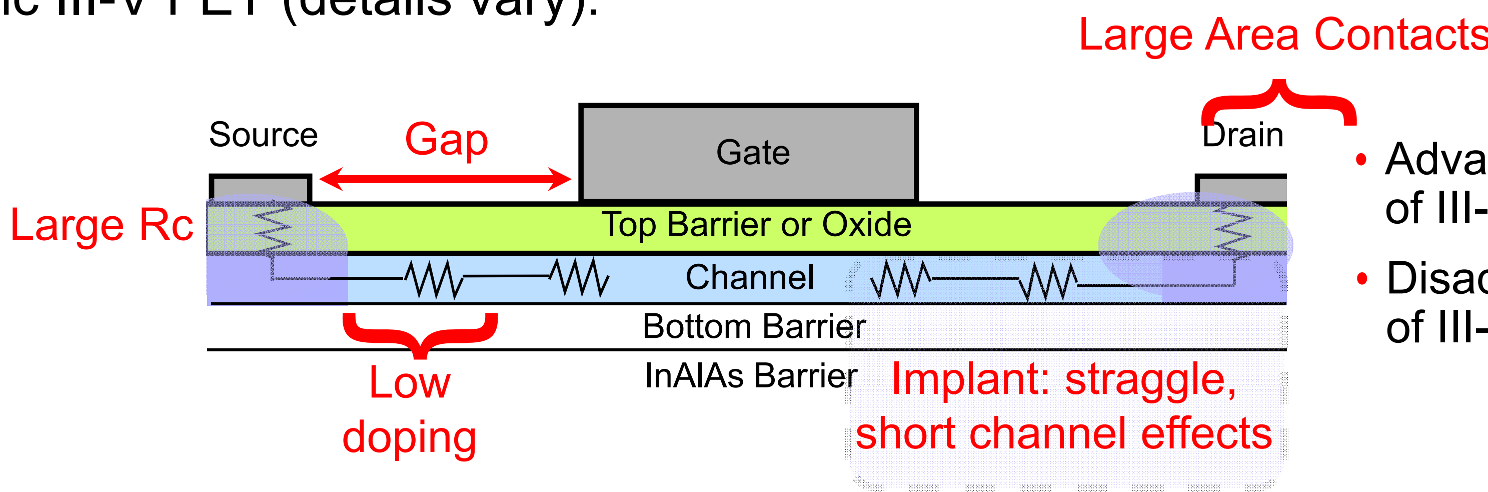
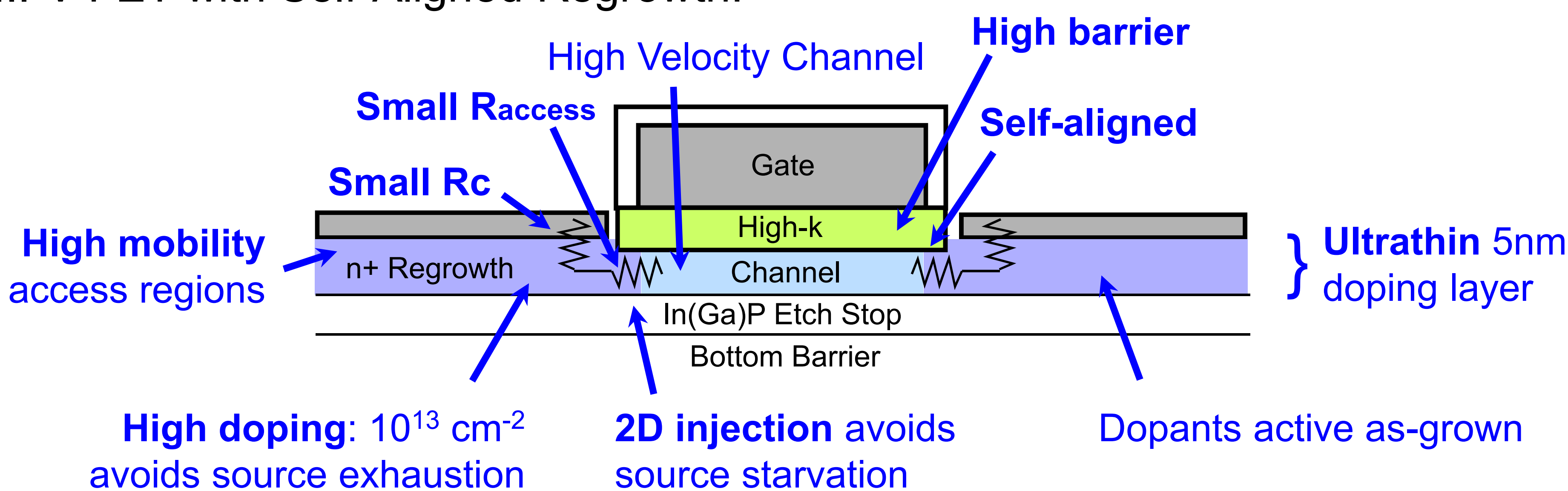
Classic III-V FET (details vary):



- Advantages of III-V's
- Disadvantages of III-V's

III-V FET with Self-Aligned Regrowth:



Process Flow Prior to Regrowth

Pattern gate metal
Selective dry etches

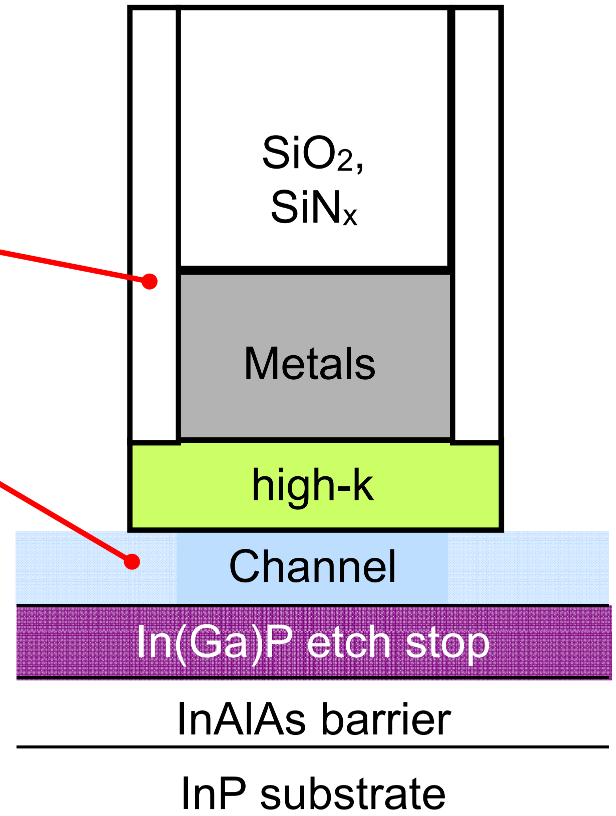
SiN_x or SiO_2 sidewalls
Encapsulate gate metals

Controlled recess etch (optional)
Slow facet planes
Not needed for depletion-mode FETs

Surface clean
UV ozone,
1:10 HCl:water dip & rinse,
UHV deox (hydrogen or thermal)

Regrowth

Fabrication details:
U. Singisetti, PSSC 2009
Rodwell IPRM 2008



MBE Regrowth: Bad at any Temperature?

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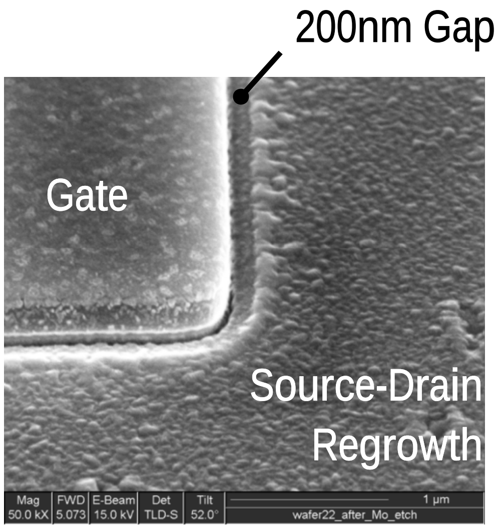
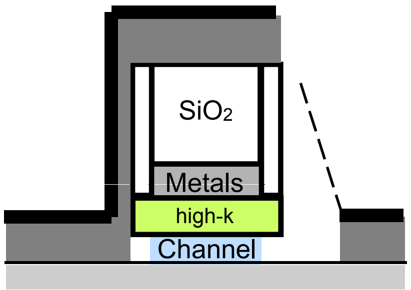
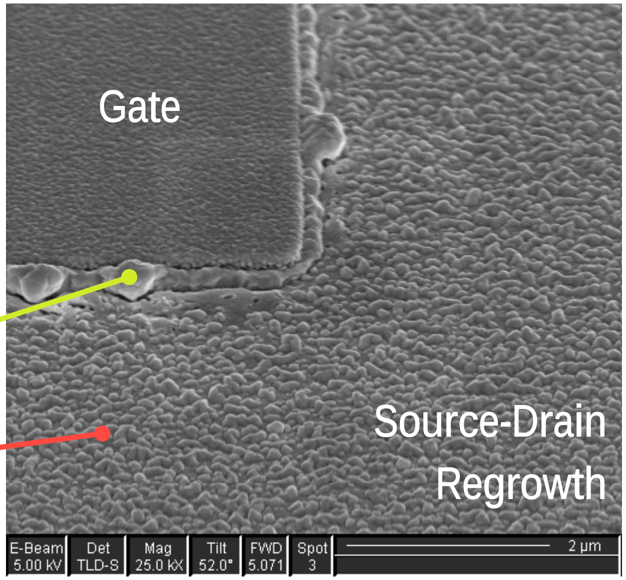
- Low growth temperature (<400°C):
  - Smooth in far field
  - Gap near gate ("shadowing")
  - No contact to channel (bad)





- High growth temperature (>490°C):
  - Selective/preferential epi on InGaAs
    - No gaps near gate
  - Rough far field
    - High resistance



Regrowth: 50nm InGaAs:Si, 5nm InAs:Si. Si=8E19/cm3, 20nm Mo, V/III=35, 0.5 μm/hr.

SEMs: Uttam Singisetti

Gap-free Regrowth by MEE

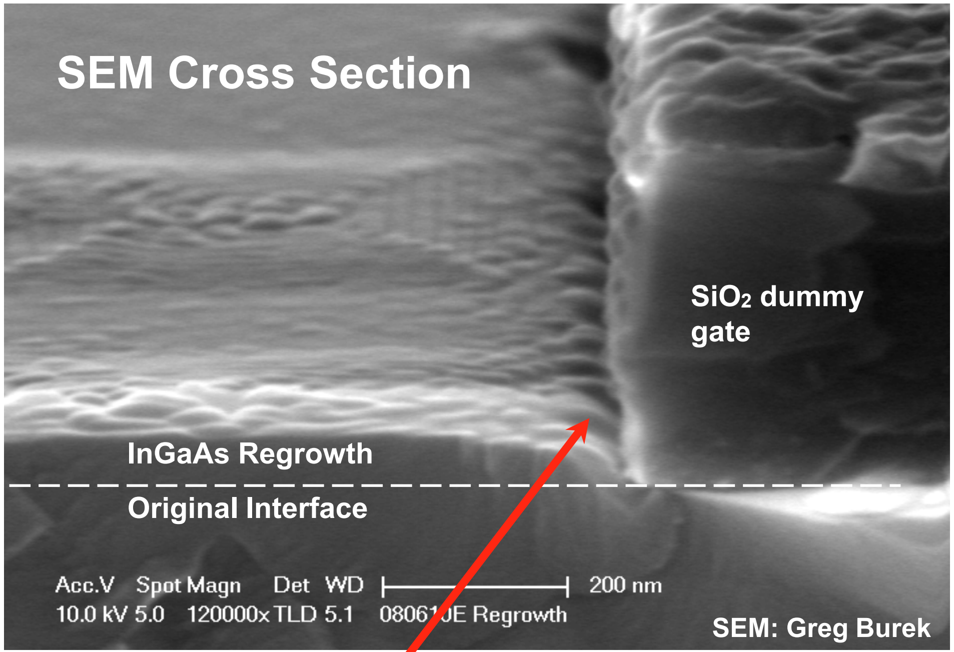
Migration-Enhanced Epitaxy (MEE) conditions: Wistey, MBE 2008

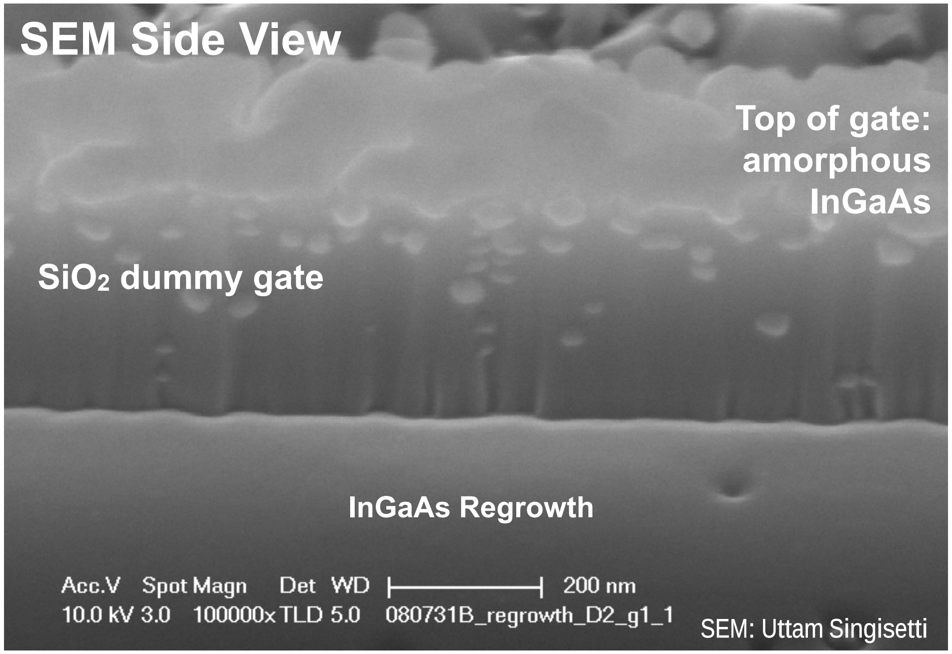
490-560°C (pyrometer)

As flux constant ~ $1x10^{-6}$ Torr: V/III~3, not interrupted.

0.5nm InGaAs:Si pulses (3.7 sec), 10-15 sec As soak

RHEED: 4x2 ==> 1x2 or 2x4 ==> 4x2 with each pulse.

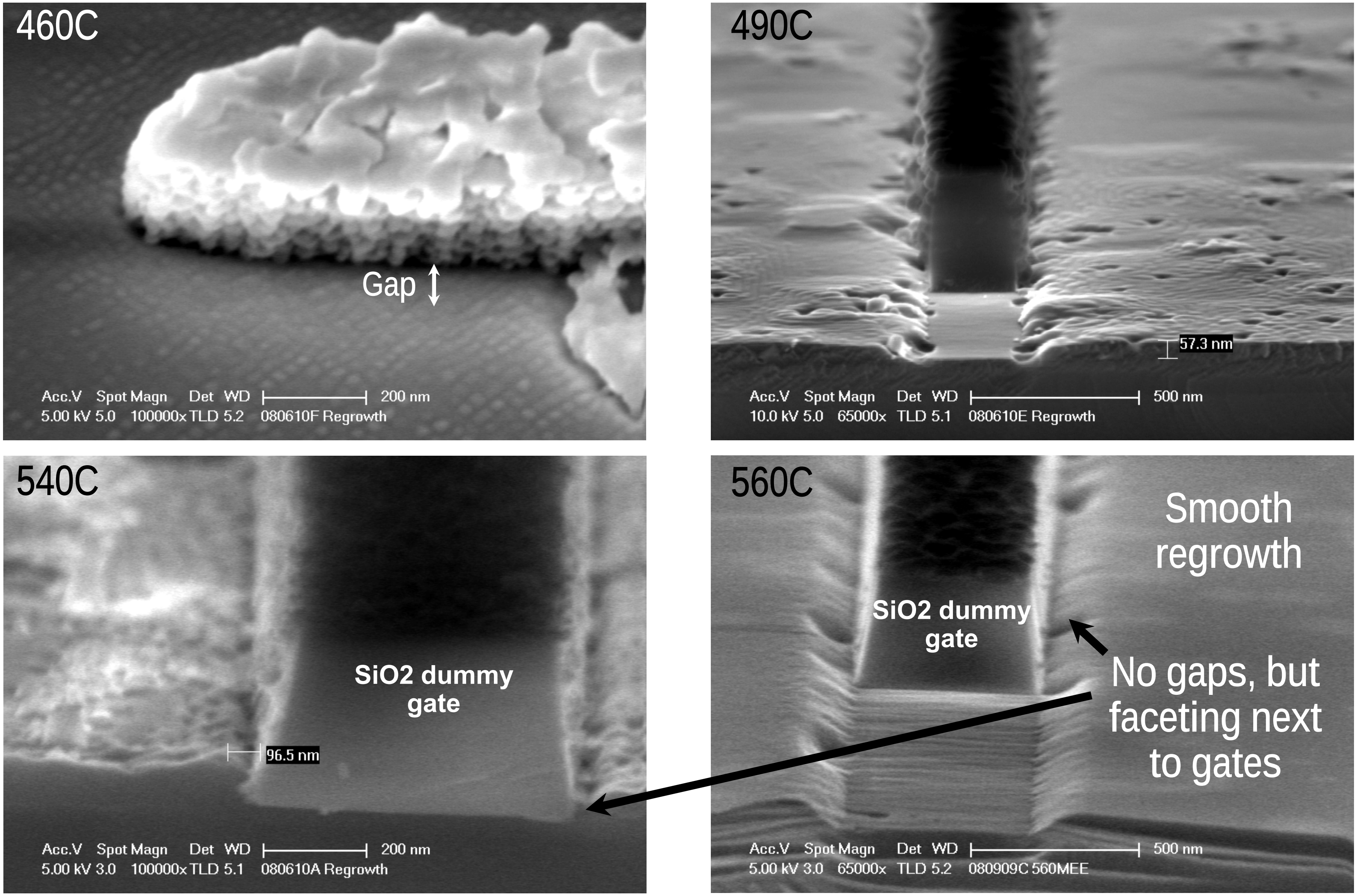




- Smaller gapCrosshatching—relaxation?
- High Si activation ($4x10^{19}$ cm^{-3}).

•Quasi-selective growth

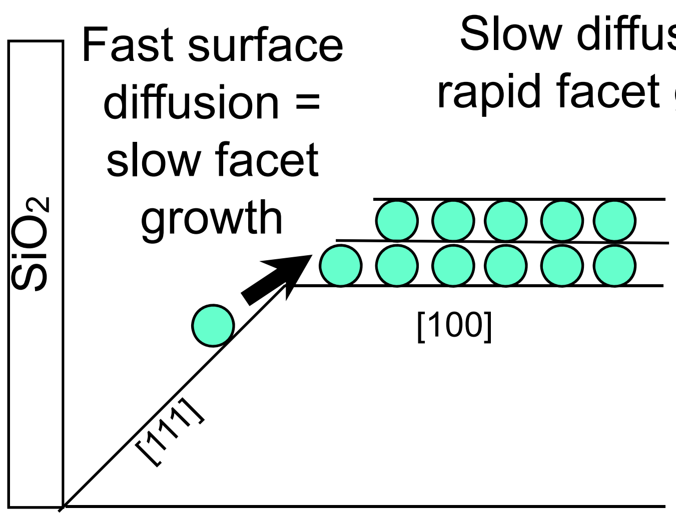
High Temperature MEE: Smooth & No Gaps

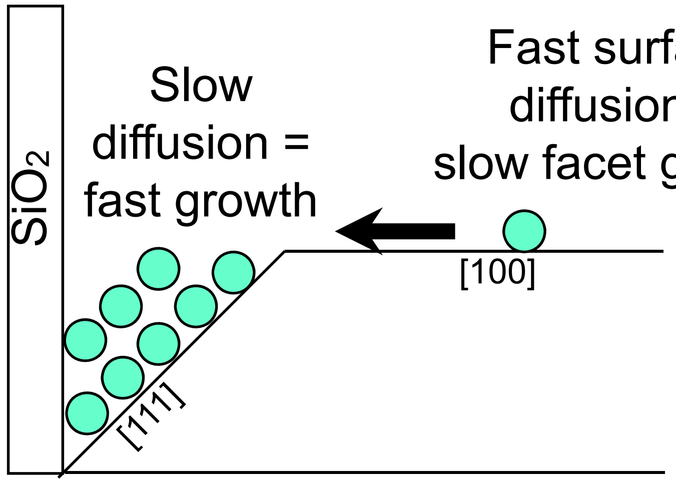


In=9.7E-8, Ga=5.1E-8 Torr

Note faceting: surface kinetics, not shadowing.

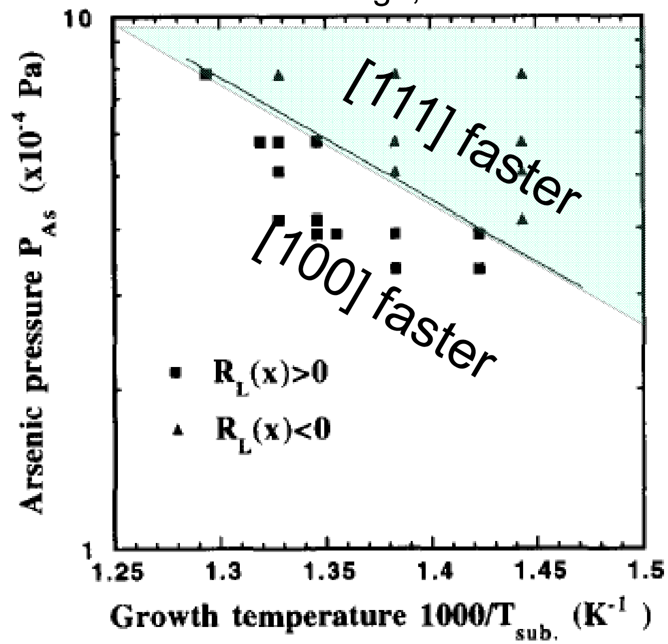
Shadowing and Facet Competition



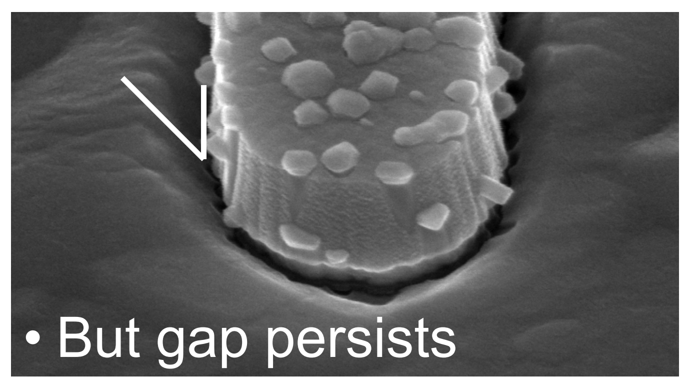


Good fill next to gate.

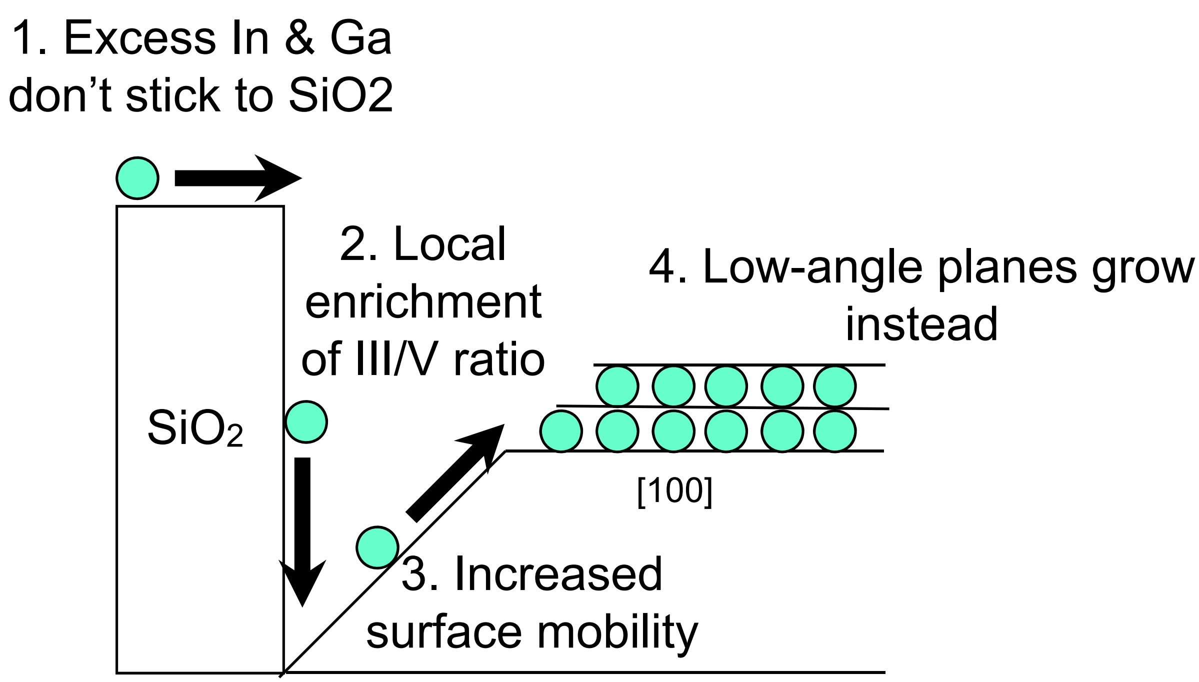
Shen & Nishinaga, JCG 1995



- Shen JCG 1995 says:
  Increased As favors [111] growth



Gate Changes Local Kinetics

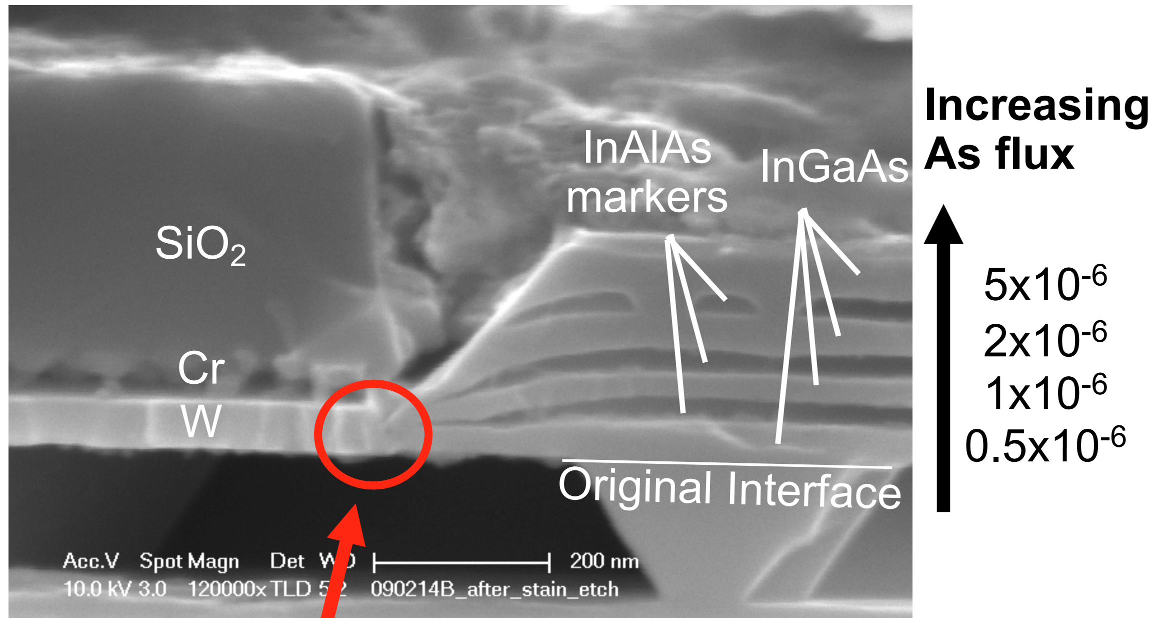


- **Diffusion of Group III's away from gate**
- **Solution: Override local enrichment of Group III's**

Control of Facets by Arsenic Flux

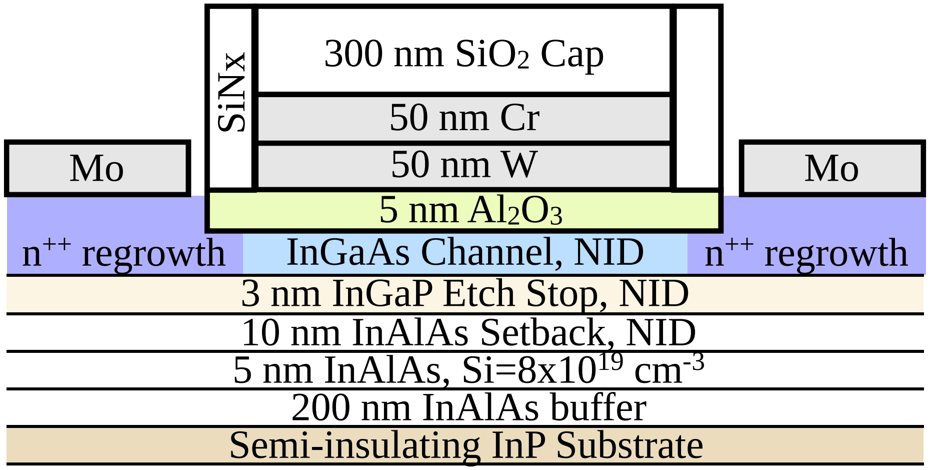
- InGaAs Experiment:
- Vary As flux
- InAlAs marker layers
- Find best fill near gate

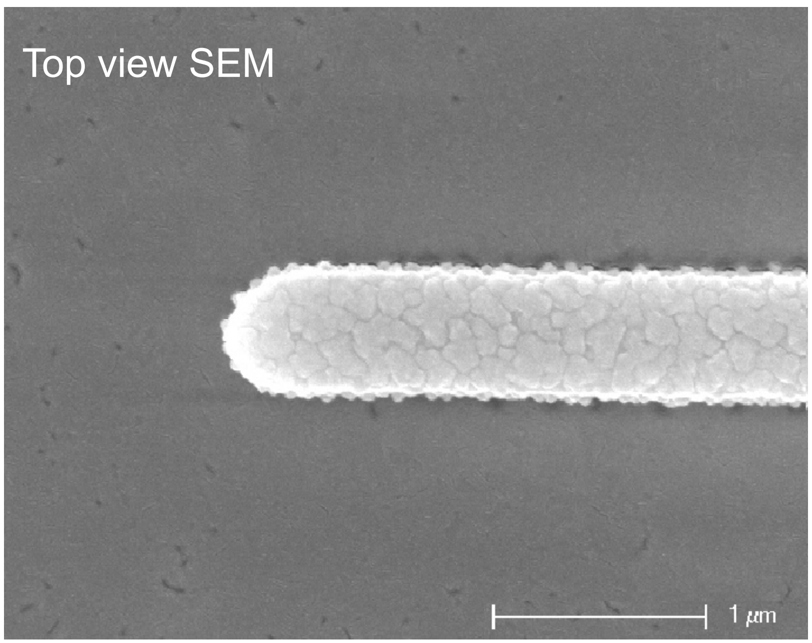
SEM of single-wafer growth series varying As flux

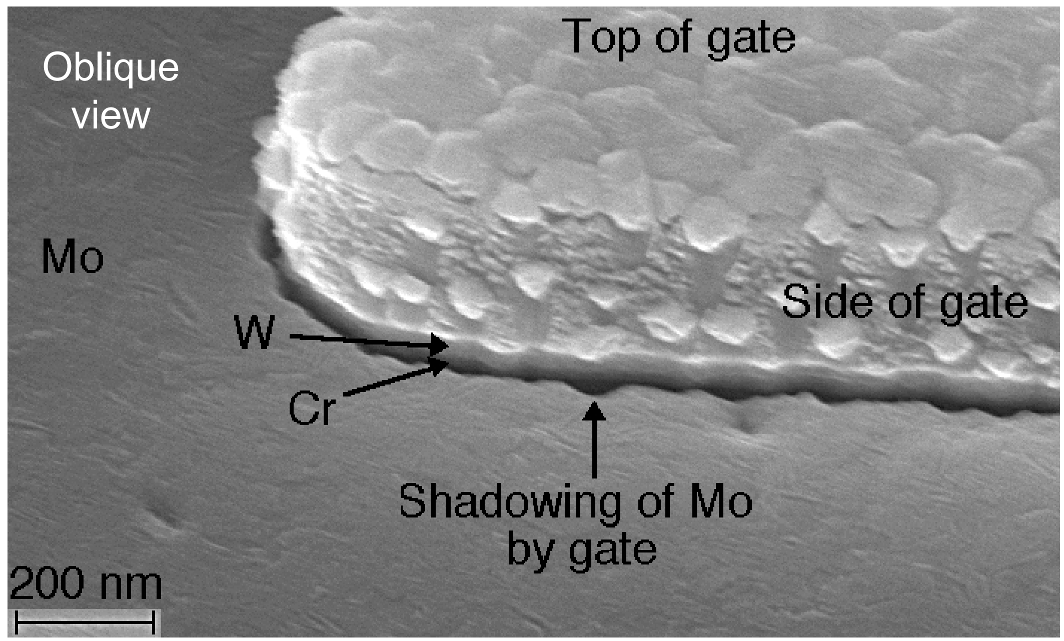


- Lowest arsenic flux → “rising tide fill”
- No gaps near gate or SiO_2/SiNx
- Tunable facet competition

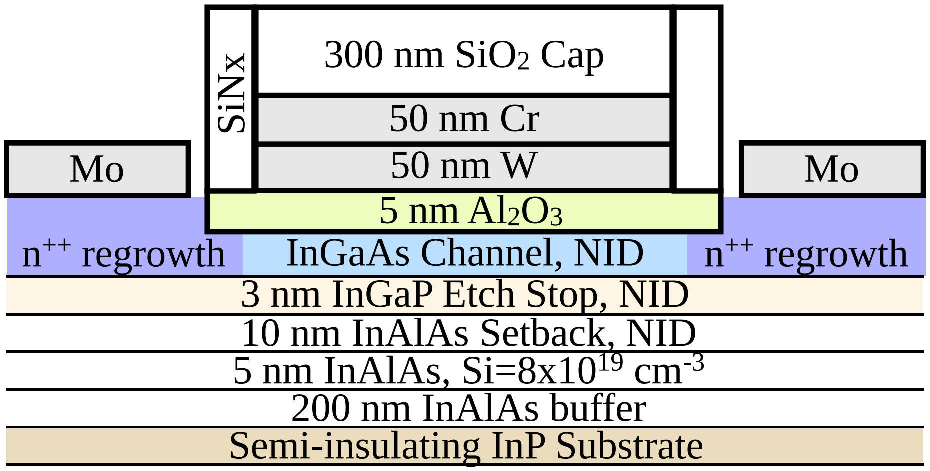
Scalable InGaAs MOSFETs



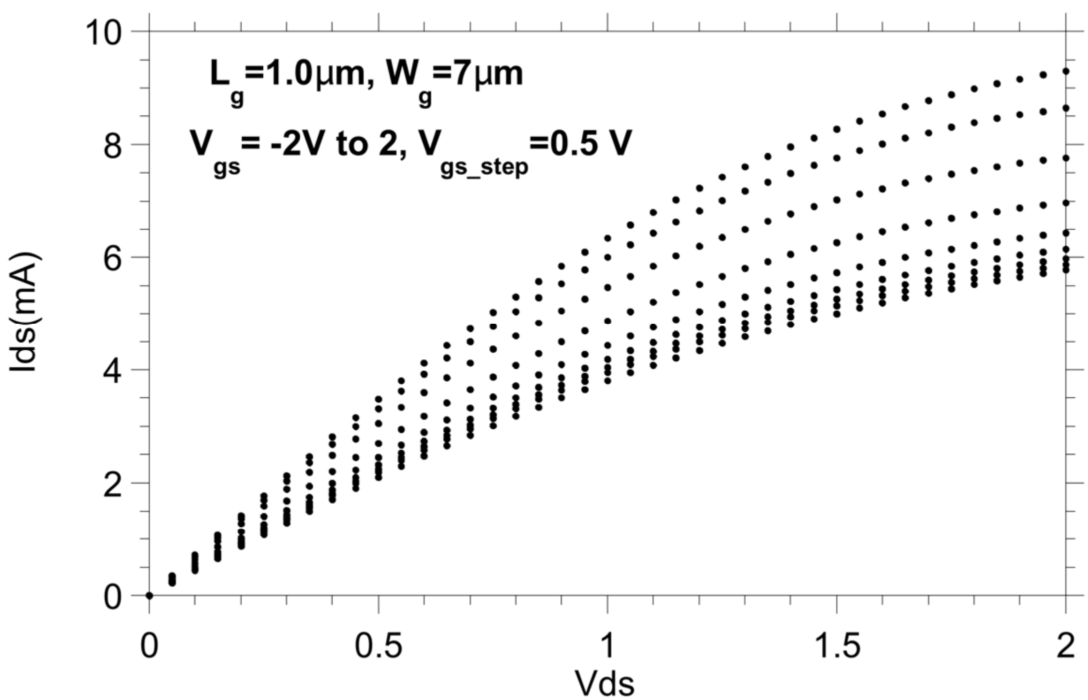


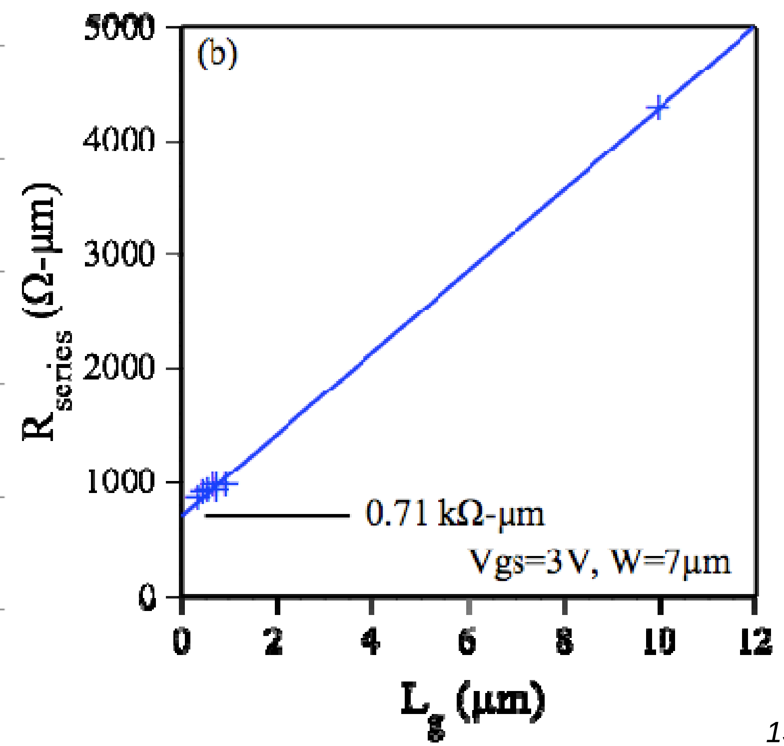


Scalable InGaAs MOSFETs

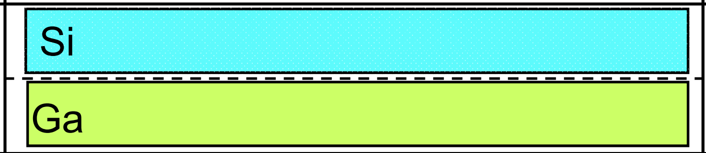
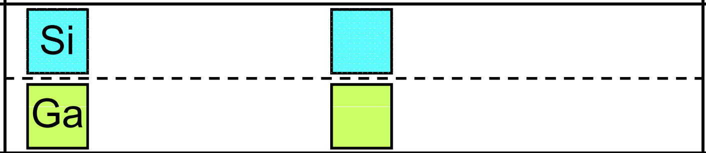
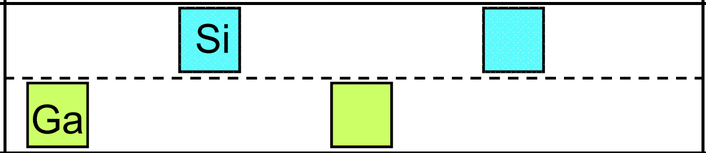
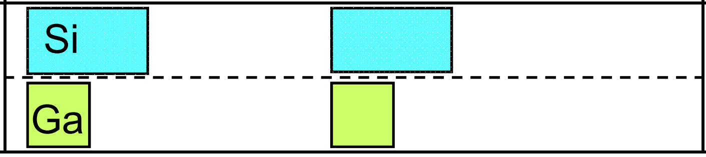


- Conservative doping design:
  - [Si] = 4×10^{13} cm^{-2}
  - Bulk n = 1×10^{13} cm^{-2} >> Dit
- Large setback + high doping = Can't turn off
- High R_{source} > 350 Ω-µm





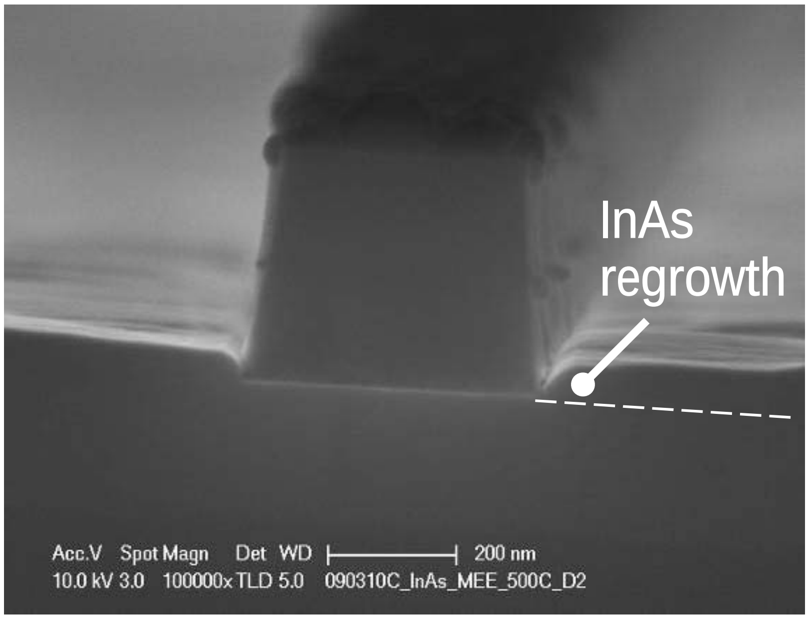
Silicon Doping in MEE

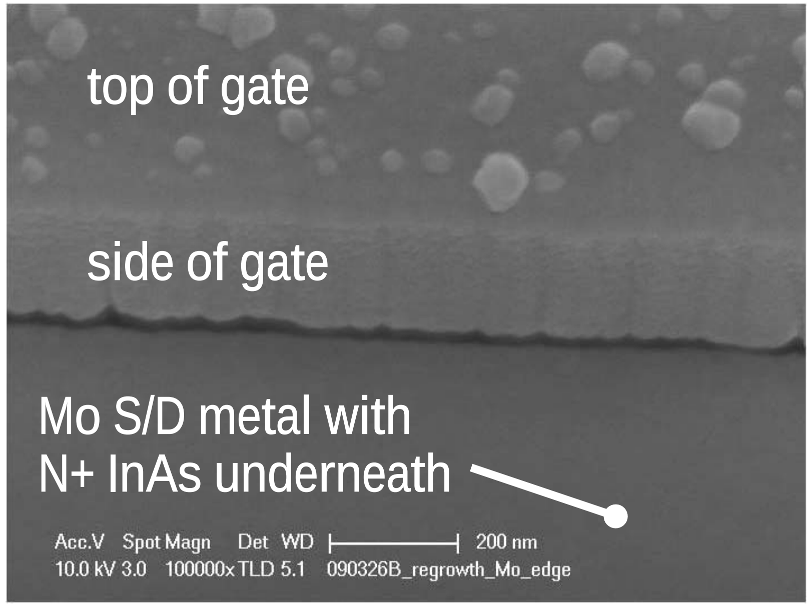
Technique	Shutter Pattern (Arsenic always open)	[Si] (cm^{-3})	n (cm^{-3})	μ ($cm^2V^{-1}s^{-1}$)
Conventional MBE	 Si / Ga	$8x10^{19}$	$4.8x10^{19}$	847
Si during Group III MEE pulse	 Si / Ga	$8x10^{19}$	$4.3x10^{19}$	1258
Si during As soak	 Si / Ga	$8x10^{19}$	$4.2x10^{19}$	1295
Double Si doping	 Si / Ga	$16x10^{19}$	--	--

- **Electron concentration nearly constant**
- **Si prefers Group III site even under As-poor conditions**
- **Increased mobility by MEE**

Regrown InAs S/D FETs

4.7 nm Al_2O_3, 5×10^{12} cm^{-2} pulse doping
In=9.7E-8, Ga=5.1E-8 Torr





- **InAs native defects are donors.[1]**
- **Reduces surface depletion.**
- **Decreased As flux works for InAs too.**

- **Gallium-free**
  = improved selectivity in regrowth

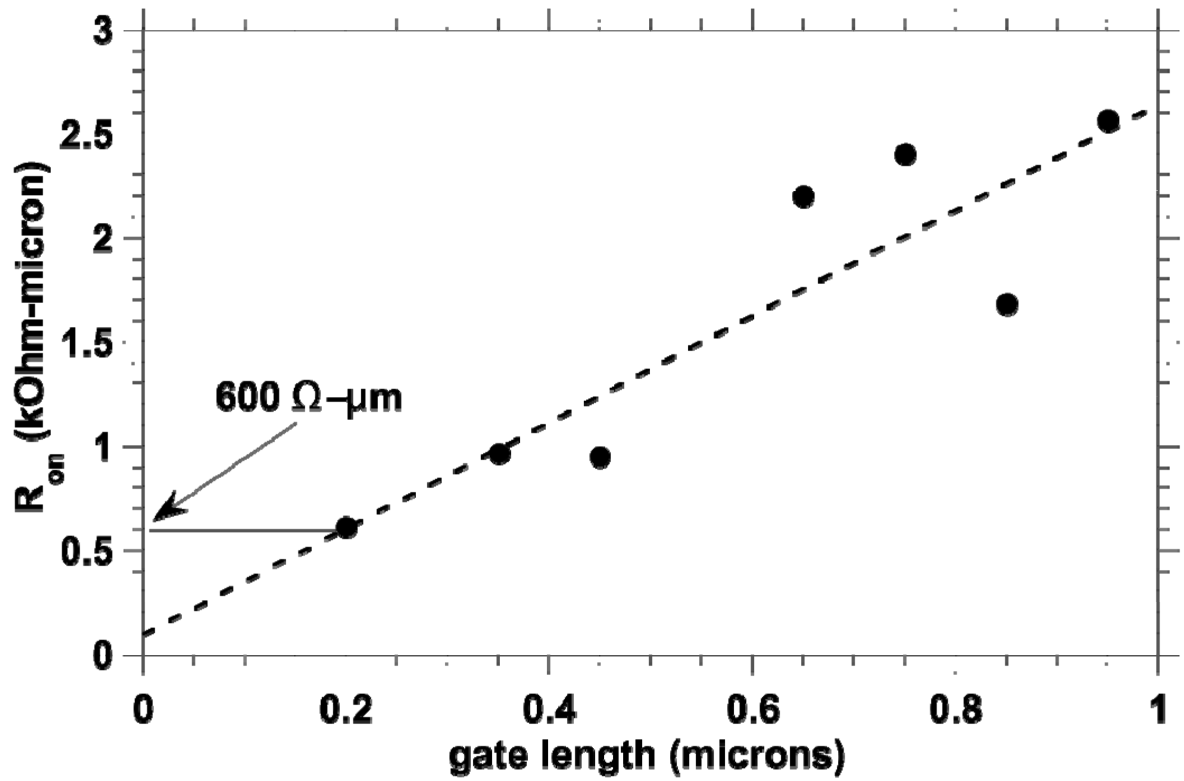
[1] **Bhargava** *et al* **, APL 1997**

SEM: Uttam Singisetti

InAs Source-Drain Access Resistance*

*Wistey *et al*, NAMBE 2009

4.7 nm Al_2O_3, InAs S/D E-FET. TLMs corrected for metal resistance.



- **Total R_{on} = 600 Ω-µm ➡ R_s < 300 Ω−µm.**
- **g_m << 1/R_s ~ 3.3 mS/µm -- Not source-limited.**
- **InAs contacts no longer limit MOSFET performance.**

Slide: Uttam Singisetti, DRC 2009

The Shape of Things to Come

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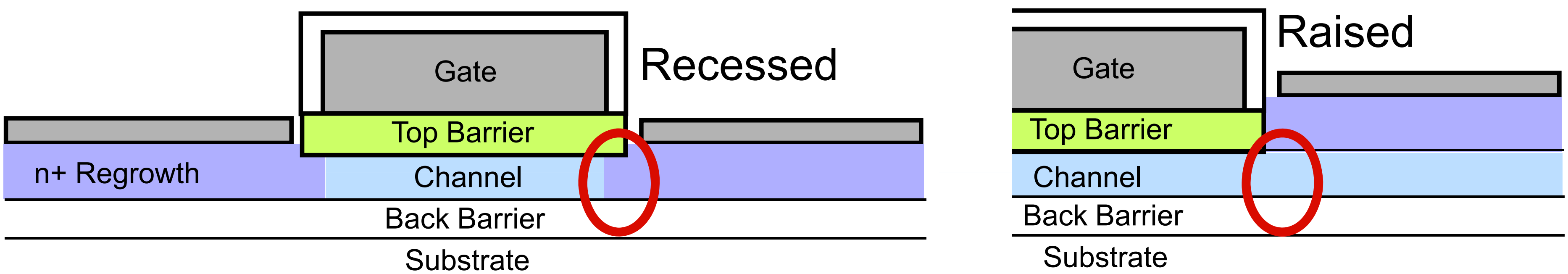
Generalized Self-Aligned Regrowth Designs:



- **Self-aligned regrowth can also be used for:**
  - **GaN HEMTs (with Nidhi in Mishra group, EMC 2009)**
  - **InGaAs HBTs and HEMTs**
  - **Selective III-V on Si — remove gaps**
  - **THz and high speed III-V electronics**

Conclusions

- Reducing As flux improves filling near gate
- Self-aligned regrowth: a roadmap for scalable III-V FETs
  - Provides III-V's with a salicide equivalent
  - Can improve GaN and GaAs FETs too
- Silicon doping impervious to MEE technique
- InAs regrown contacts improve InGaAs MOSFETs...
  - Not limited by source resistance @ 1 mA/μm
  - Comparable to other III-V FETs... but now scalable

Acknowledgements

- Rodwell & Gossard Groups (UCSB): Uttam Singisetti, Greg Burek, Ashish Baraskar, Vibhor Jain...
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