Process Technologies For Sub-100-nm InP HBTs & InGaAs MOSFETs

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III-V transistors of ~10 to 100 nm lithographic dimensions are being developed both for THz applications and for use in large-scale digital integrated circuits. Reducing dimensions increases both IC packing density and transistor bandwidth. Increasing bandwidth of an arbitrary circuit by $\gamma:1$ requires a $\gamma:1$ reduction of transistor capacitances and transit delays while maintaining constant resistances and bias and signal voltages and currents. For bipolar transistors [1], this requires a $\sim\gamma^1:1$ reduction in epitaxial dimensions, a $\gamma^2:1$ reduction in contact resistivities, and a $\gamma^2:1$ reduction in lithographic dimensions. For field-effect transistors [2], such scaling requires again a $\gamma:1$ reduction in epitaxial dimensions (dielectric equivalent thickness, wavefunction depth) and a $\gamma^2:1$ reduction in contact resistivities, but only requires a $\gamma^1:1$ reduction in lithographic dimensions (gate length). Required current densities scale with both transistor types; for HBTs, emitter current density ($\mathrm{mA}/\mu\mathrm{m}^2$) varies as γ^2, though current per unit emitter stripe length remains fixed, while for FETs, current per until gate width ($\mathrm{mA}/\mu\mathrm{m}$) varies as γ^1, but current per unit source and drain Ohmic contact area ($\mathrm{mA}/\mu\mathrm{m}^2$) varies as γ^2. To build multi-THz HBTs and HEMTs, and to build sub-22-nm InGaAs MOSFETs, we must fabricate *self-aligned* contacts and junctions of 10-100 nm dimensions. We must develop Ohmic contacts of $\sim 1\,\Omega-\mu\mathrm{m}^2$ contact resistivity; this resistivity must not increase when operating ~25-250 $\mathrm{mA}/\mu\mathrm{m}^2$ current density, nor can the contact metals diffuse under such high current and thermal stress through device junctions only ~5-10 nm below the surface. We here describe our efforts to develop such fabrication processes for both InP-based FETs and HBTs.

First, consider in more detail FET scaling in the constant-voltage, constant-velocity limit. Vertical dimensions (T_{well} , T_{eq}) must be reduced in proportion to gate length to maintain a constant g_m / G_{ds} ratio and to maintain a constant ratio of the parallel-plate (C_{g-ch}) to the fringing ($C_{gs,f}$, C_{gd}) components of the device input capacitance; in the absence of vertical scaling, drain-induced barrier lowering increases, output conductance degrades, and the input capacitance becomes dominated by gate fringing fields. As a consequence of vertical scaling, on-state current density I_d / W_g increases as γ^1. It is well understood that difficulties in reducing T_{eq} (gate leakage by tunneling) and in increasing C_{DOS} [3] will impede constant-voltage FET scaling; note also that T_{inv} must scale as γ^{-1}, requiring thinner wells or stronger vertical fields, $(R_s + R_d)/W_g$ must scale as γ^{-1}, requiring both lower ρ_c and increased carrier concentrations in access regions, and on-state inversion charge density n_s must scale as γ^1, requiring increased gate barrier height. Further, device self-heating scales as γ^1, a serious concern for normally-on circuits such as sub-mm-wave amplifiers. These scaling considerations apply to equally to InGaAs FETs in development for VLSI and for sub-mm-wave/THz applications; device design goals include low access resistance, high drive current density, thin wells, high sheet carrier density, and gate barriers that are both thin and high in energy. Future sub-mm-wave FETs may well use high-K gate dielectrics to permit small T_{eq} and large n_s; note that moderately high interface charge density D_{it} will not impair device gain at frequencies well above the inverse of the interface trap lifetimes.

Established III-V HEMT structures do not well address these scaling requirements. We have therefore developed a fully self-aligned InGaAs MOSFET process flow [4] (fig. 1). In this flow, 4.7 nm Al_2O_3 gate dielectric is deposited by ALD on a 5 nm $In_{0.53}Ga_{0.47}As$ channel, the gate is formed by blanket W/Cr/SiO_2 deposition and RIE etching, and thin ~25 nm Si_xN_y gate sidewalls formed. After etching the Al_2O_3, self-aligned S/D InAs N+ regions (50 nm thick, 8×10^{19} cm^{-3}, 23 Ω sheet resistance) are formed by migration enhanced epitaxy, and self-aligned S/D contacts formed by in-situ blanket evaporation of Mo ($3.5\,\Omega-\mu\mathrm{m}^2$ contact resistance) and a subsequent height-selective etch [5]. Mesa isolation and back-end metal completes the process. Unlike HEMTs, no gate barrier is present in the S/D regions, the source and drain are fully self-aligned to the gate, and carrier densities in the S/D access regions are high ($\sim1.5\times10^{13}\mathrm{cm}^{-2}$). Figure 3 shows measured I_D for a 200-nm-L_g device.

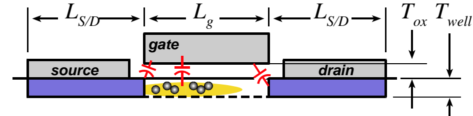
We are developing similar processes to fabricate InP HBTs with 64 nm and 128 nm W_e (fig. 4). In-situ Mo emitter contacts [6] provide $1.1\pm0.4\ \Omega-\mu\mathrm{m}^2$ contact resistivity. The emitter metal is dry-etched Mo or W to withstand high target current densities. Emitter and base contacts are separated by thin Si_xN_y sidewalls, and base contacts are sputter-deposited refractory metals.

1] M. Rodwell *et al*, IEEE Proceedings, February 2008.
2] M. Wistey *et al,* Proceedings, Electrochemical Society Annual Meeting, May 2009.
3] P. M. Solomon, S. E. Laux, 2001 IEEE IEDM
4] U. Singisetti *et al*, Physica Status Solidi (c), Volume 6 Issue 6; M. Rodwell *et al* 2008 IEEE Indium Phosphide and Related Materials Conference; U. Singisetti *et al*, submitted to IEEE EDL; M. Wistey et al, 2009 Electronics Materials Conference. .
5] G.J. Burek *et al,* Journal of Crystal Growth Volume 311, Issue 7, 15 March 2009, Pages 1984-1987
6] A. Baraskar *et al*, 2009 Physics and Chemistry of Surfaces and Interfaces Conference (to be published, JVST)

Table 1: HBT scaling laws: changes required for $\gamma:1$ increased bandwidth in an arbitrary circuit

parameter	law	parameter	law
emitter junction length, L_e (nm)	γ^0	contact resistivities ρ_c ($\Omega-\mu m^2$)	γ^{-2}
emitter junction width, W_e (nm)	γ^{-2}	emitter current density ($mA/\mu m^2$)	γ^2
collector junction width (nm)	γ^{-2}	emitter current density ($mA/\mu m$)	γ^0
collector depletion thickness (nm)	γ^{-1}	temperature rise (one device, K)	$\sim\ln(L_e/W_e)$
base thickness (nm)	$\sim\gamma^{-1/2}$		

Table 2: Constant-voltage / constant-velocity FET scaling laws: changes required for $\gamma:1$ increased bandwidth in an arbitrary circuit



parameter	law	parameter	law
gate length L_g, source-drain contact lengths $L_{S/D}$ (nm)	γ^{-1}	gate-channel capacitance $C_{g-ch}=[1/C_{ox}+1/C_{semi}+1/C_{DOS}]^{-1}$ (fF)	γ^{-1}
gate width W_g (nm)	γ^{-1}	transconductance $g_m\sim C_{g-ch}v_{injection}/L_g$ (mS)	γ^0
equivalent oxide thickness $T_{eq}=T_{ox}\varepsilon_{SiO_2}/\varepsilon_{oxide}$ (nm)	γ^{-1}	gate-source, gate-drain fringing capacitances $C_{gs,f}\propto\varepsilon W_g$, $C_{gd}\propto\varepsilon W_g$ (fF)	γ^{-1}
dielectric capacitance $C_{ox}=\varepsilon_{SiO_2}L_gW_g/T_{eq}$ (fF)	γ^{-1}	S/D access resistances R_s, R_d (Ω)	γ^0
		S/D contact resistivity R_s/W_g, R_d/W_g ($\Omega-\mu m$)	γ^{-1}
inversion thickness $T_{inv}\sim T_{well}/2$ (nm)	γ^{-1}	S/D contact resistivity ρ_c ($\Omega-\mu m^2$)	γ^{-2}
semiconductor capacitance $C_{semi}=\varepsilon_{semi}L_gW_g/T_{inv}$ (fF)	γ^{-1}	drain current $I_d\sim g_m(V_{gs}-V_{th})$ (mA)	γ^0
DOS capacitance $C_{DOS}=q^2nm^*/2\pi\hbar^2$ (fF)	γ^{-1}	drain current density ($mA/\mu m$)	γ^1
electron density n_s (cm^{-2})	γ^1	temperature rise (one device, K)	$\sim W_g^{-1}$

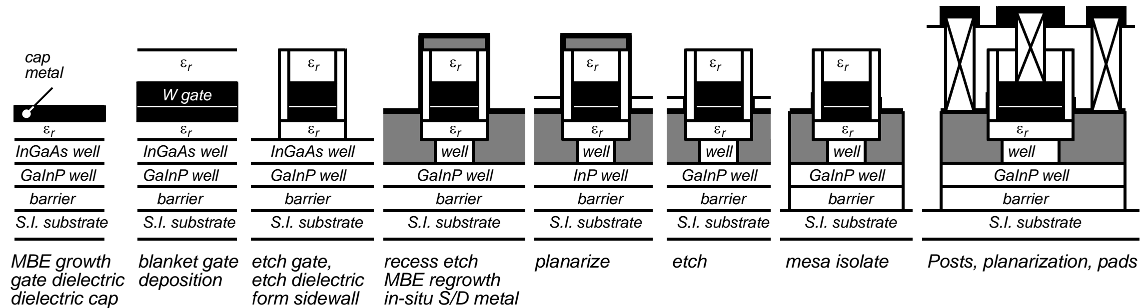


Figure 1: Process flow for III-V FETs with source/drain regrowth by MEE.

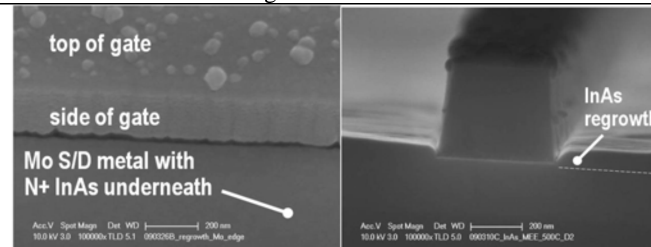


Figure 2: Regrown S/D InGaAs FET, oblique view & cross-section.

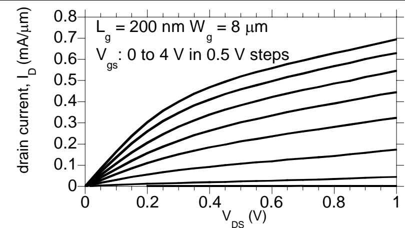


Figure 3: Common-source characteristics .

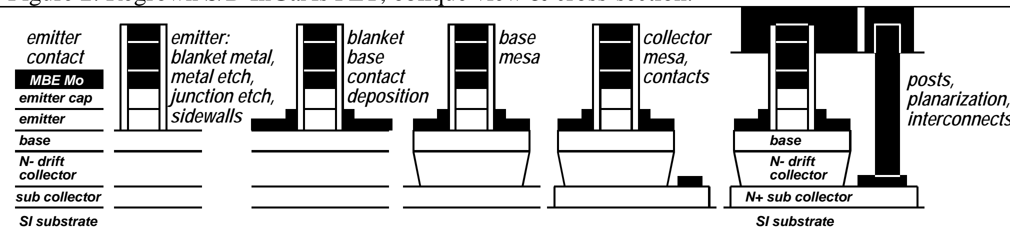


Figure 4: Refractory-contact /dry-etched process flow for 128 nm /64 nm InP HBTs.