Improved Regrowth of Self-Aligned Ohmic Contacts for III-V FETs

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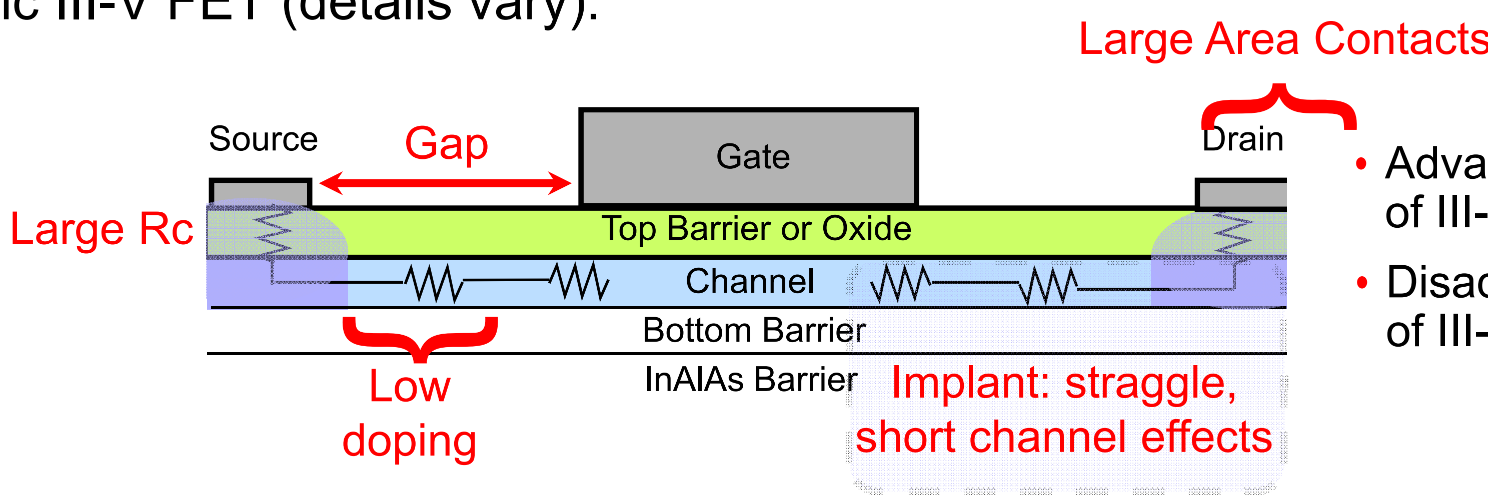
Outline: Regrown III-V FET Contacts

- Motivation for Self-Aligned Regrowth
- Facets, Gaps, Arsenic Flux and MEE
- MOSFET Results
- Conclusion

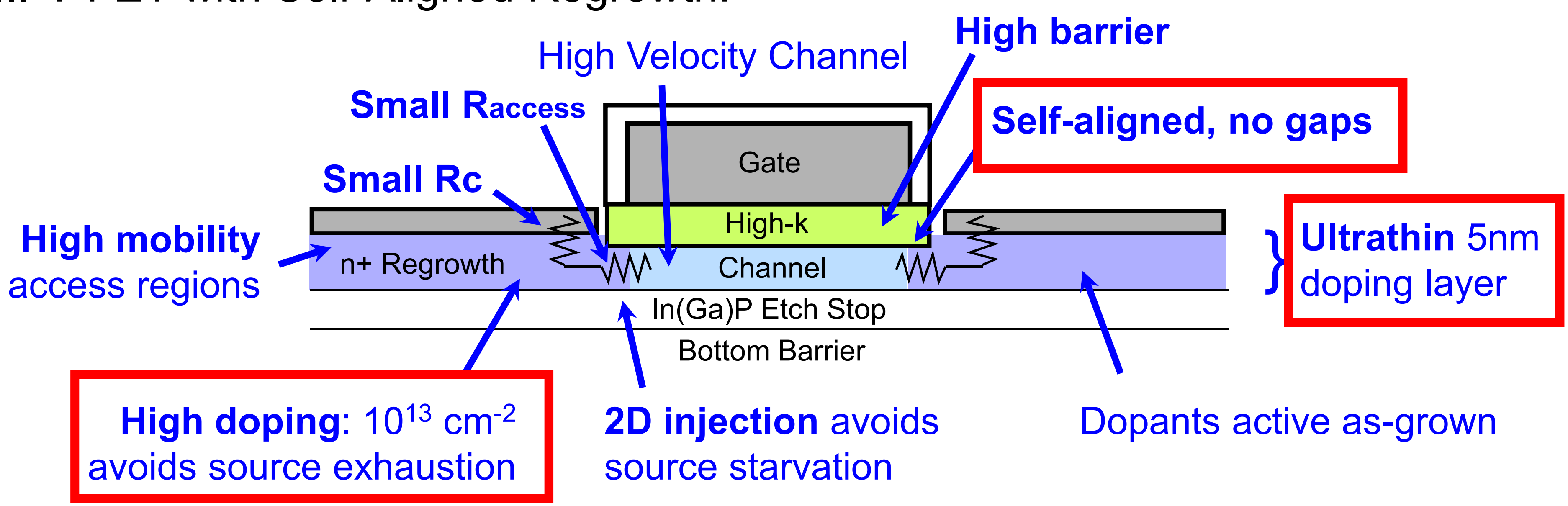
Motivation for Regrowth: Scalable III-V FETs

Classic III-V FET (details vary):



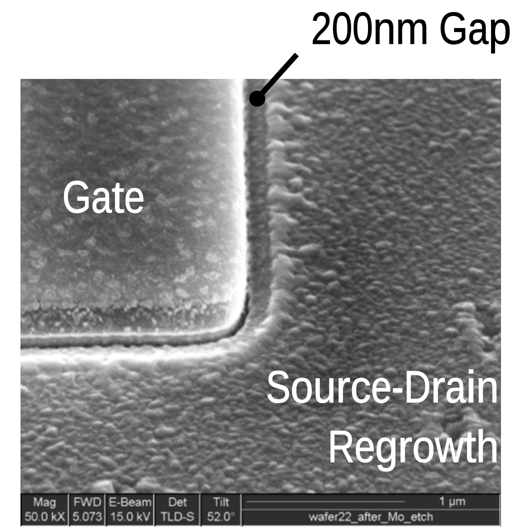
- Advantages of III-V's
- Disadvantages of III-V's

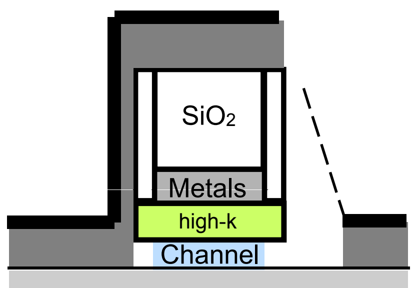
III-V FET with Self-Aligned Regrowth:



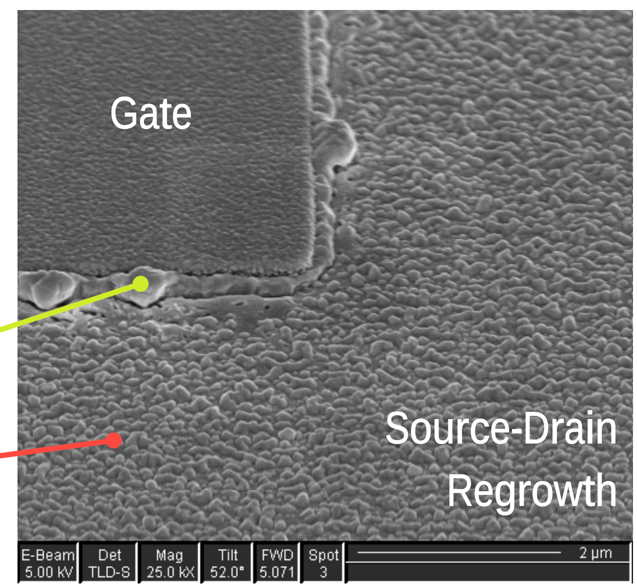
MBE Regrowth: Bad at any Temperature?

- **Low growth temperature (<400°C):**
  - **Smooth in far field**
  - **Gap near gate ("shadowing")**
  - **No contact to channel (bad)**





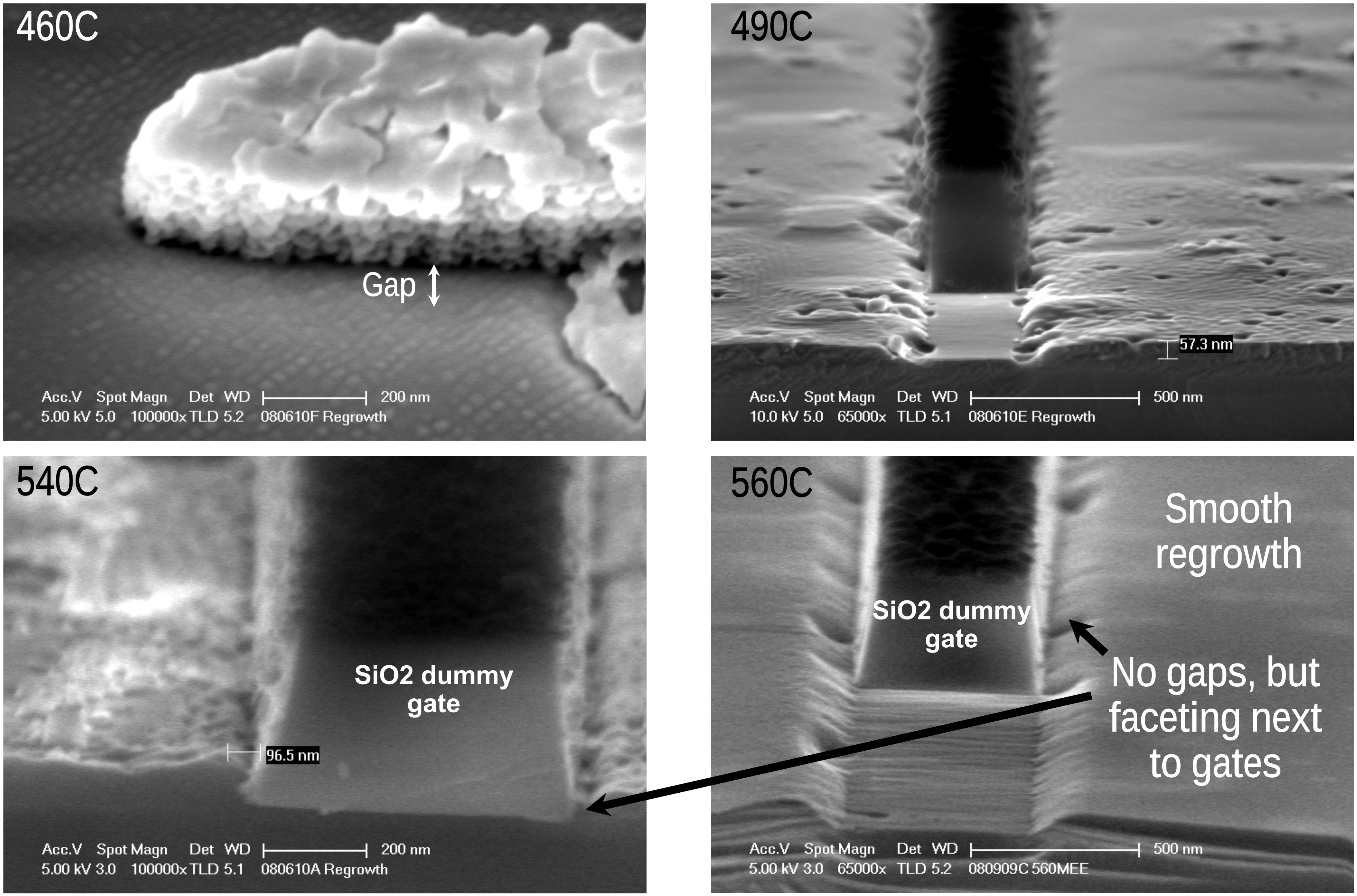
- **High growth temperature (>490°C):**
  - **Selective/preferential epi on InGaAs**
    - **No gaps near gate**
  - **Rough far field**
    - **High resistance**



Regrowth: 50nm InGaAs:Si, 5nm InAs:Si. Si=8E19/cm3, 20nm Mo, V/III=35, 0.5 µm/hr.

SEMs: Uttam Singisetti

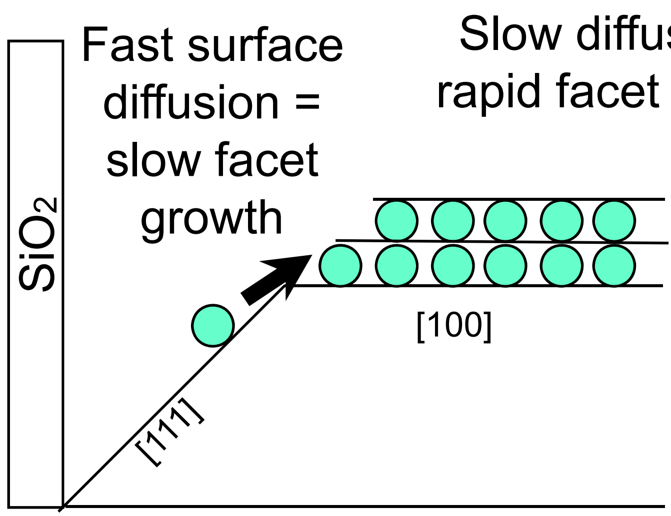
High Temperature MEE: Smooth & No Gaps

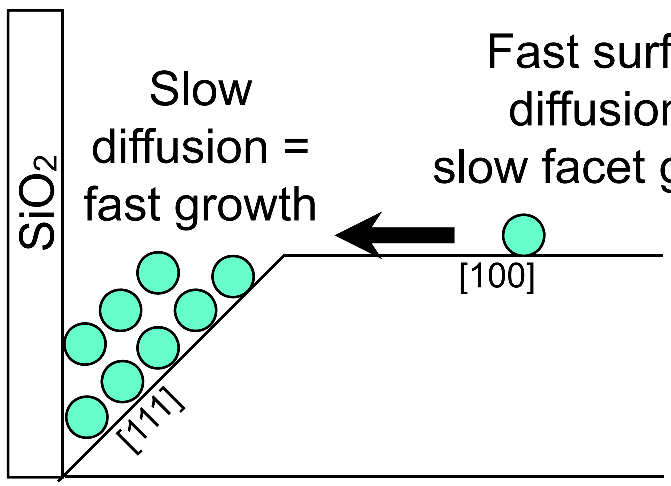


In=9.7E-8, Ga=5.1E-8 Torr

Note faceting: surface kinetics, not shadowing.

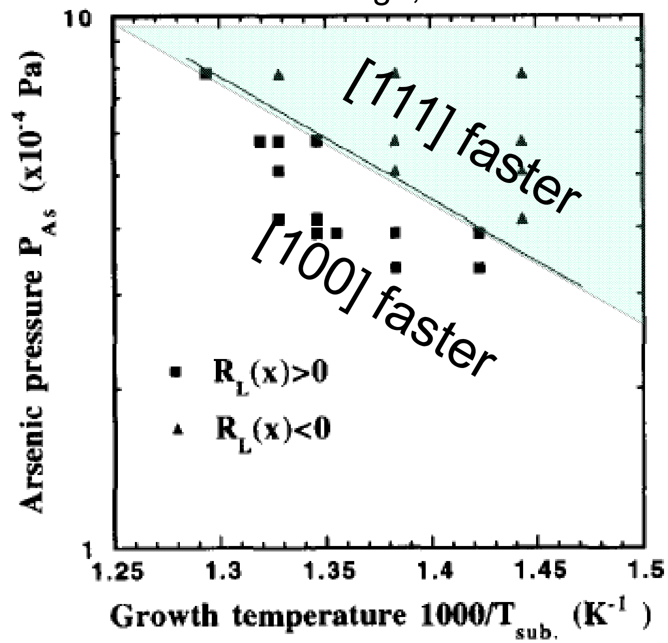
Shadowing and Facet Competition



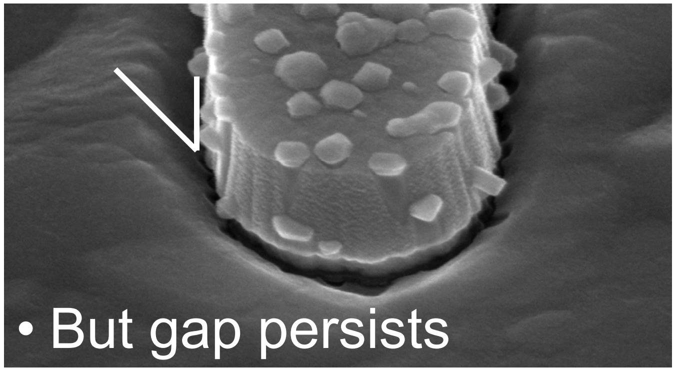


Good fill next to gate.

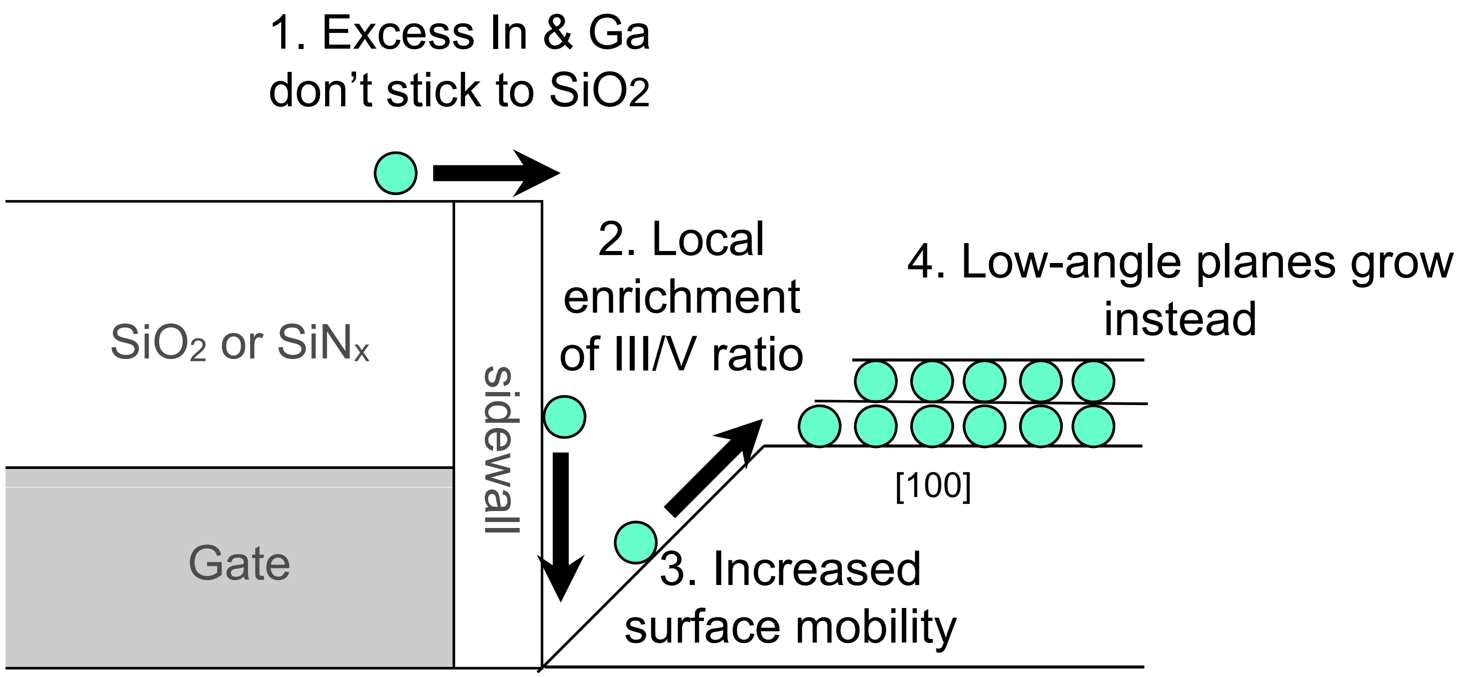
Shen & Nishinaga, JCG 1995



- Shen JCG 1995 says: Increased As favors [111] growth



Gate Changes Local Kinetics

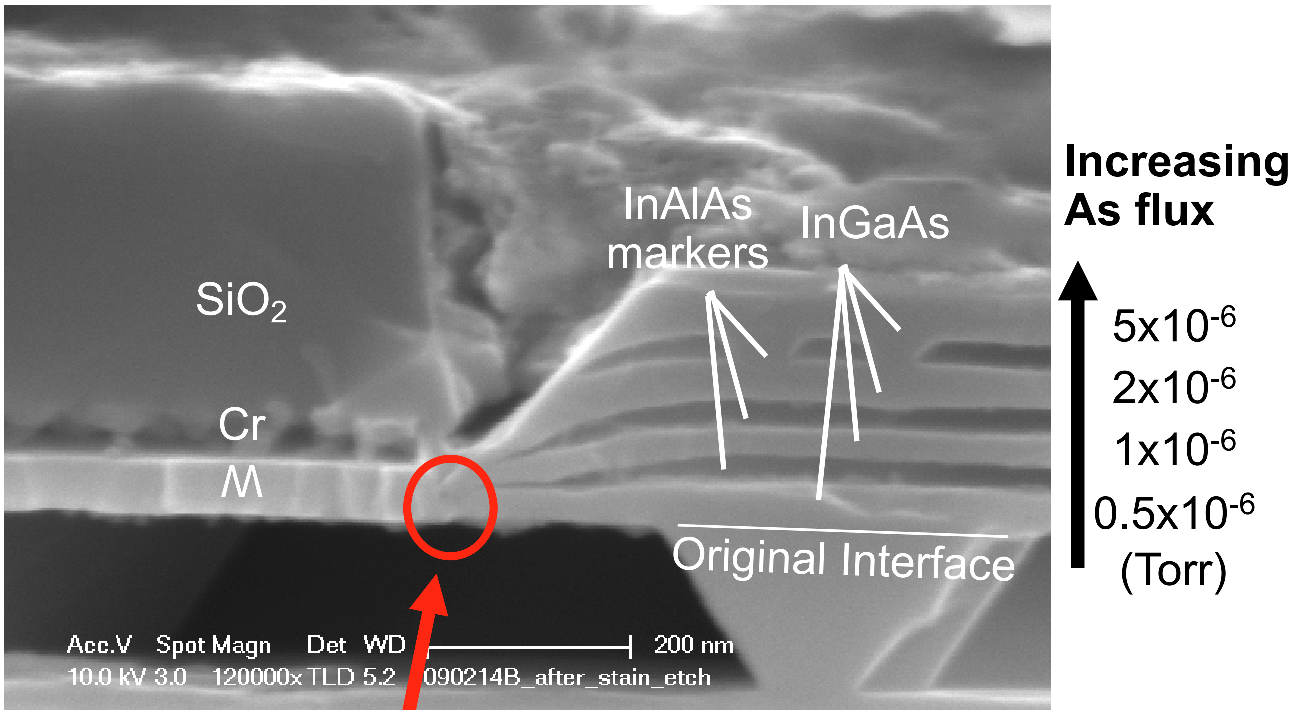


- **Diffusion of Group III's away from gate**

Change of Faceting by Arsenic Flux

UCSB

- InGaAs layers with increasing As fluxes, separated by InAlAs.

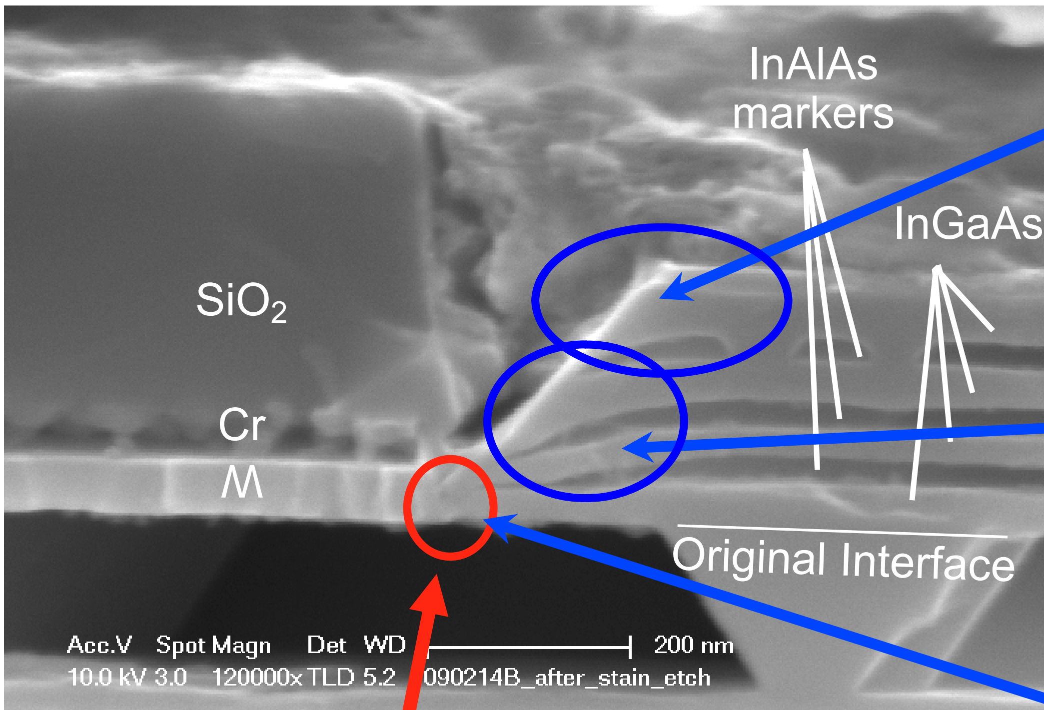


- Lowest arsenic flux → “rising tide fill”
- No gaps near gate or SiO_2/SiNx
- Tunable facet competition

Growth conditions: MEE, 540*C, Ga+In BEP=1.5x10^{-7} Torr, InAlAs 500-540°C MBE.

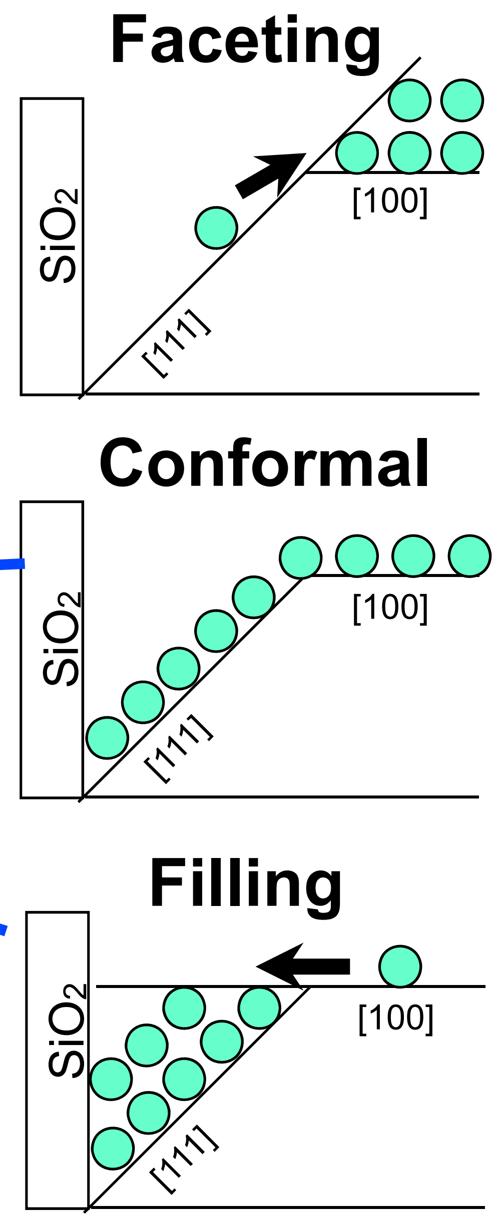
Control of Facets by Arsenic Flux

- InGaAs:Si layers with increasing As fluxes, separated by InAlAs.



Increasing As flux

5x10^{-6}
2x10^{-6}
1x10^{-6}
0.5x10^{-6}
(Torr)



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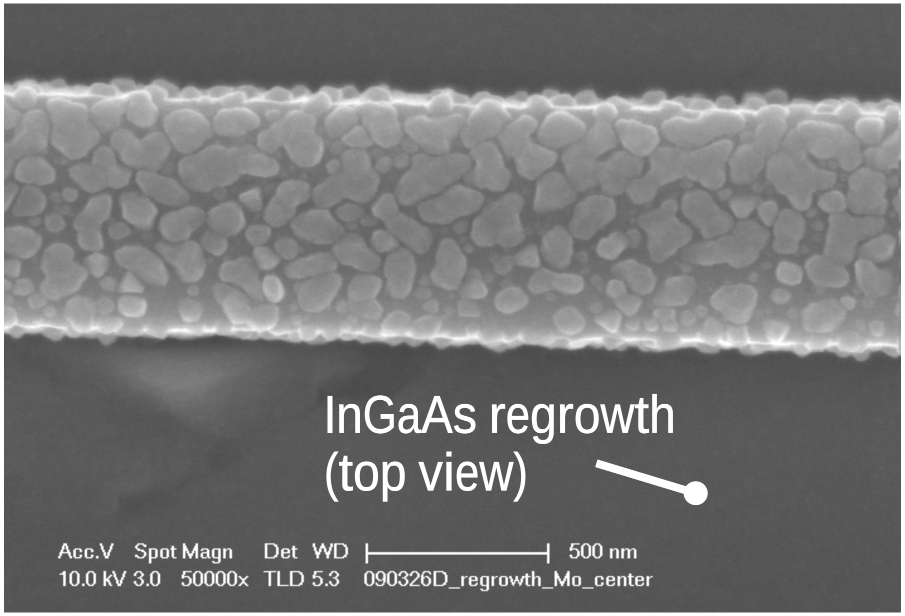
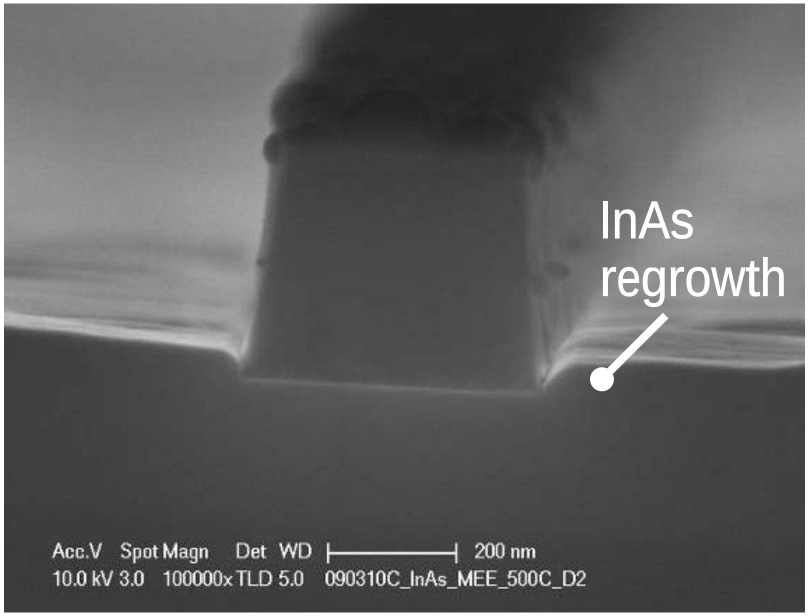
Low-As Regrowth of InGaAs and InAs

InGaAs



- No faceting near gate
- Smooth far-field too

InAs



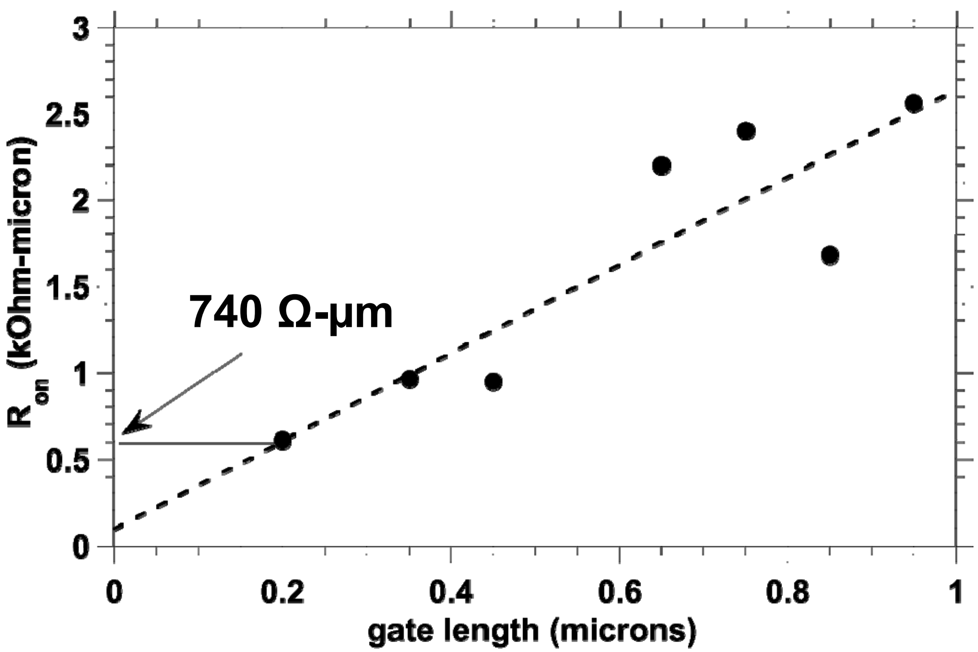
- Low As flux good for InAs too.
- InAs native defects are donors.
  Bhargava *et al* , APL 1997
- Reduces surface depletion.

4.7 nm $Al_2 0_3$, 5×10^{12} cm^{-2} pulse doping
In=9.7E-8, Ga=5.1E-8 Torr

SEMs: Uttam Singisetti

InAs Source-Drain Access Resistance

4.7 nm Al_2O_3, InAs S/D E-FET.



- **Upper limit: $R_{s,max}$ = $R_{d,max}$ = 370 Ω−μm.**
- Intrinsic g_{mi} = 0.53 mS/μm
- **g_m << $1/R_s$ ~ 3.3 mS/μm (source-limited case)**

$$g_m = \frac{g_{mi}}{1 + g_{mi} \times R_s}$$

➡ **Ohmic contacts no longer limit MOSFET performance.**

Conclusions

- Reducing As flux improves filling near gate
- Self-aligned regrowth: a roadmap for scalable III-V FETs
  - Provides III-V's with a salicide equivalent
- InGaAs and relaxed InAs regrown contacts
  - Not limited by source resistance @ 1 mA/μm
  - Results comparable to other III-V FETs... but now scalable

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