A 204.8GHz Static Divide-by-8 Frequency Divider in 250nm InP HBT

Zach Griffith, Miguel Urteaga, Richard Pierson, Petra Rowell,

Mark Rodwell*, and Bobby Brar

Teledyne Scientific Company, Thousand Oaks, CA 91360, USA

***Department of Electrical and Computer Eng., UC Santa Barbara**

e-mail: zgriffith@teledyne.com, phone: 805-373-4104

Why Static Frequency Dividers ?

MS flip-flops are very widely-used high speed digital circuits:

- Dividers are master-slave flip-flop with inverting feedback
- Connection as 2:1 frequency divider provides simple test method

Standard benchmark of logic speed:

- Performance comparisons across technologies

Dynamic, super-dynamic, frequency dividers:

- Higher maximum frequency than true static dividers
- Narrow-band operation → applications are limited

High speed technology performance for static dividers:

- 250nm InP HBT: NGAS **200.6GHz** (2009), TSC/UCSB **204.8GHz** (2010)
- Advanced SiGe HBT: Infinion **110^{+}GHz**

Fast divider design – identifying dominant gate delays

Gate Delay Determined by :

Depletion capacitance charging through the logic swing

$$\left(\frac{\Delta V_{LOGIC}}{I_C}\right)\left(C_{cb}+C_{be,\text{depletion}}\right)$$

Depletion capacitance charging through the base resistance

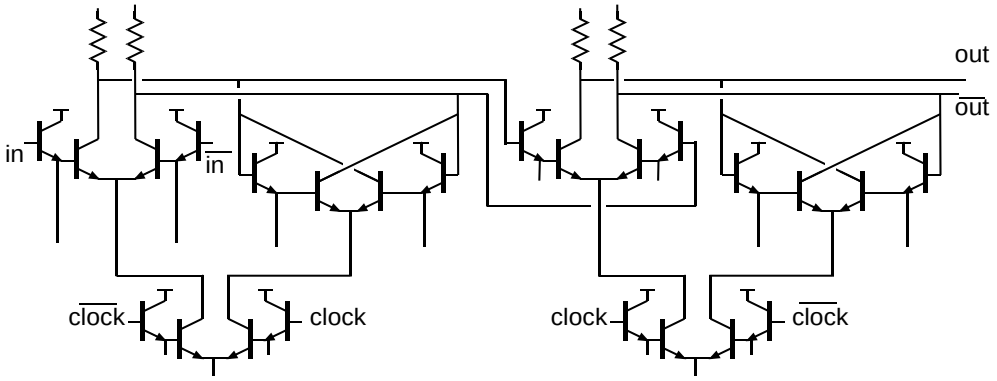
$$R_{\text{bb}}\left(C_{cb}+C_{be,\text{depletion}}\right)$$

Supplying base + collector stored charge through the base resistance

$$R_{\text{bb}}\left(\tau_b+\tau_c\right)\left(\frac{I_C}{\Delta V_{LOGIC}}\right)$$

The logic swing must be at least

$$\Delta V_{LOGIC} > 6\left(\frac{kT}{q}+R_{ex}I_c\right)$$



Delay not well correlated with HBT delay $1/(2\pi f_\tau)$.

$\left(\Delta V_{LOGIC}/I_C\right)\left(C_{cb}+C_{be,\text{depl}}\right)$ is 60% - 80% of total.

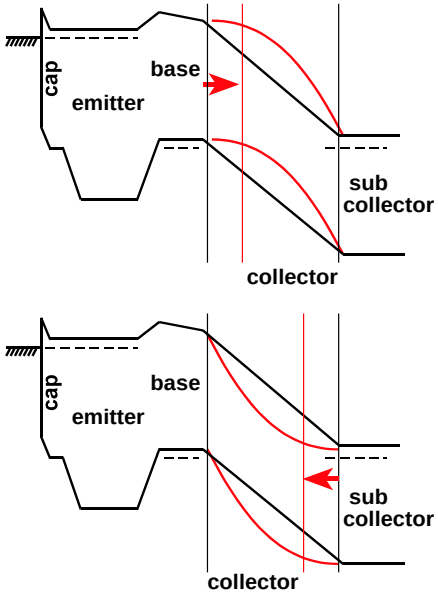
Low $\left(C_{cb}/I_c\right)$ is a key HBT design objective.

$$\frac{C_{cb}\Delta V_{LOGIC}}{I_C}=\frac{\Delta V_{LOGIC}}{2V_{CE,\min}}\left(\frac{A_{\text{collector}}}{A_{\text{emitter}}}\right)\left(\frac{T_C}{2v_{effective}}\right)$$

R_{ex} must be very low for low ΔV_{logic} at high J_e

...Need to design for clock speed, not f_τ & f_{max}

200GHz dividers – collector design for 250nm HBTs



Collector Field Collapse (Kirk Effect)

$$V_{cb} + \phi > +(J / v_{sat} - qN_d)(T_c^2 / 2\varepsilon)$$

Collector Depletion Layer Collapse

$$V_{cb,\min} + \phi > +(qN_d)(T_c^2 / 2\varepsilon)$$

$$\Rightarrow \quad J_{\max} = 2\varepsilon v_{sat}(V_{ce} + V_{ce,\min}) / T_c^2$$

(1-D collector current flow)

0.5um HBT, 150GHz divider, J_e = 5mA/um²

$$C_{cb,1}\frac{\Delta V_{logic}}{I_C} = \frac{\varepsilon_o \varepsilon_r A_{c,1}}{T_{C,1}} \frac{\Delta V_{logic}}{J_{e,1} A_{e,1}}$$

0.25um HBT, 200GHz divider – vertical, lateral scaling for J_e = 10mA/um²

$$C_{cb,2}\frac{\Delta V_{logic}}{I_C} = \frac{\varepsilon_o \varepsilon_r \frac{1}{2} A_{c,1}}{\frac{2}{3} T_{C,1}} \frac{\Delta V_{logic}}{2J_{e,1} \cdot \frac{1}{2} A_{e,1}} = \frac{3}{4} C_{cb,1}\frac{\Delta V_{logic}}{I_C}$$

33% reduction

$$C_{cb,2}\frac{\Delta V_{logic}}{I_C} = \frac{\varepsilon_o \varepsilon_r \frac{1}{2} A_{c,1}}{T_{C,1}} \frac{\Delta V_{logic}}{2J_{e,1} \cdot \frac{1}{2} A_{e,1}} = \frac{1}{2} C_{cb,1}\frac{\Delta V_{logic}}{I_C}$$

Lateral scaling, current spreading for J_e = 10mA/um²

Key HBT Scaling Limit → Emitter Resistance

ECL delay not well correlated with f_τ or f_{max}

Largest delay is charging C_{cb}

$$C_{cb}\frac{\Delta V_{logic}}{I_C} = \frac{\varepsilon_o \varepsilon_r A_{collector}}{T_C}\frac{\Delta V_{logic}}{J_e A_{emitter}} \quad ; \text{ where } J_{e,max} \propto 1/T_c^2.$$

→ $J_e \cong 10$ mA/μm^2 needed for 200 GHz clock rate

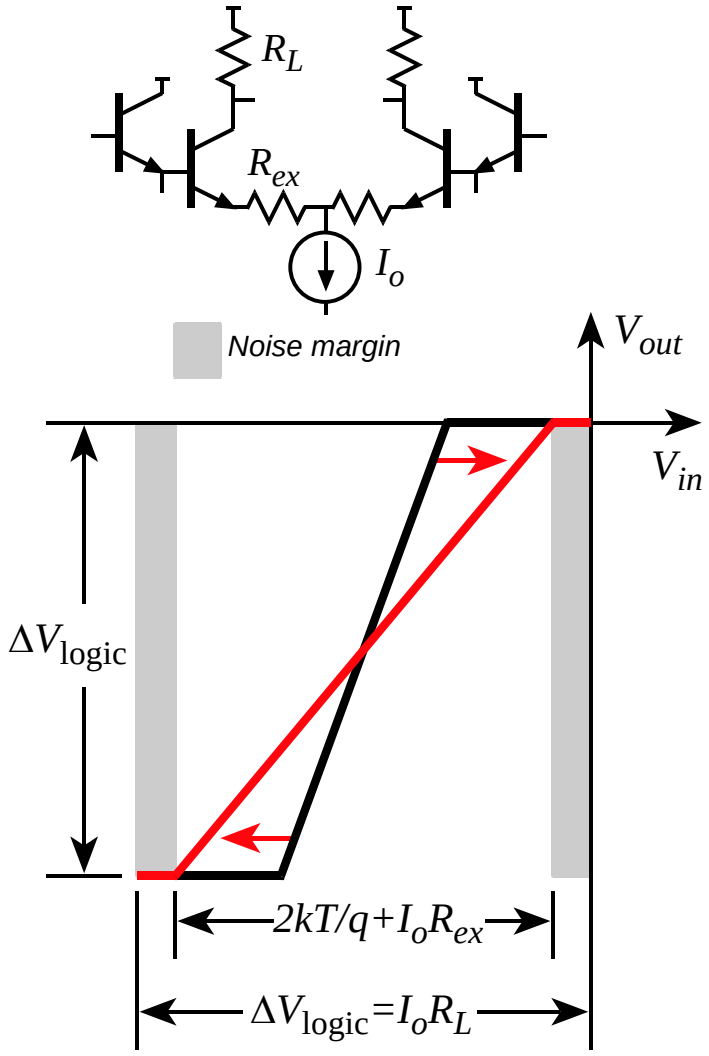
Voltage drop of emitter resistance becomes excessive

$R_{ex}I_c = \rho_{ex}J_e = (15\ \Omega\cdot\mu m^2) \cdot (10\ mA/\mu m^2) =$ ***150 mV***

→ considerable fraction of $\Delta V_{logic} \cong 300$ mV

Degrades logic noise margin

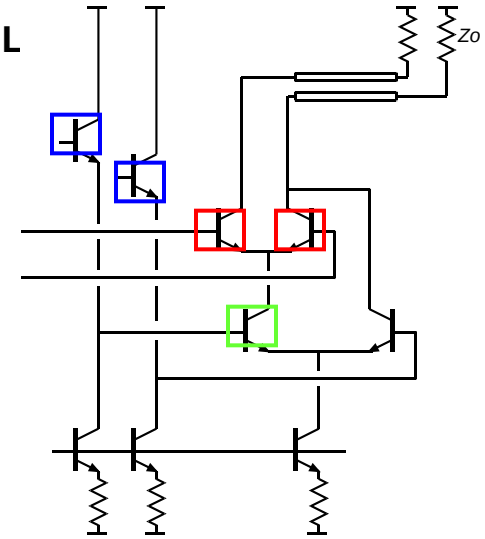
→ $\rho_{ex} \leq 7\ \Omega\cdot\mu m^2$ needed for 200 GHz clock rate



This slide presented at BCTM 2004 for phase-I 150GHz divider.
HBT metrics here invoked to demonstrate the phase-III 200GHz divider.

C_{cb}/I_c Charging Rate: ECL delays lower than CML

CML



ECL

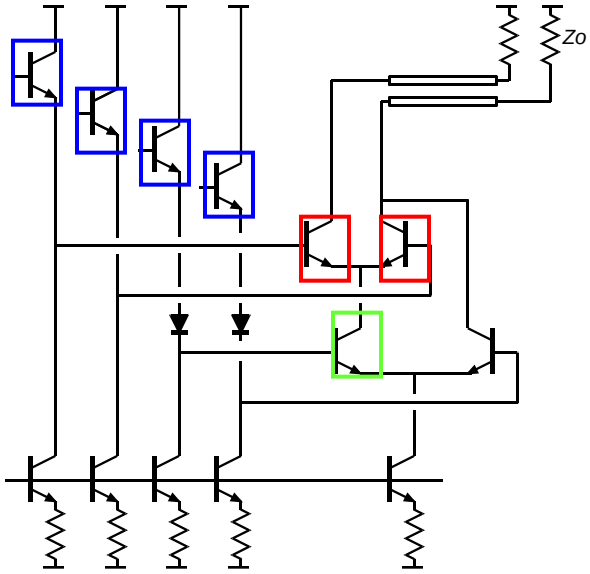
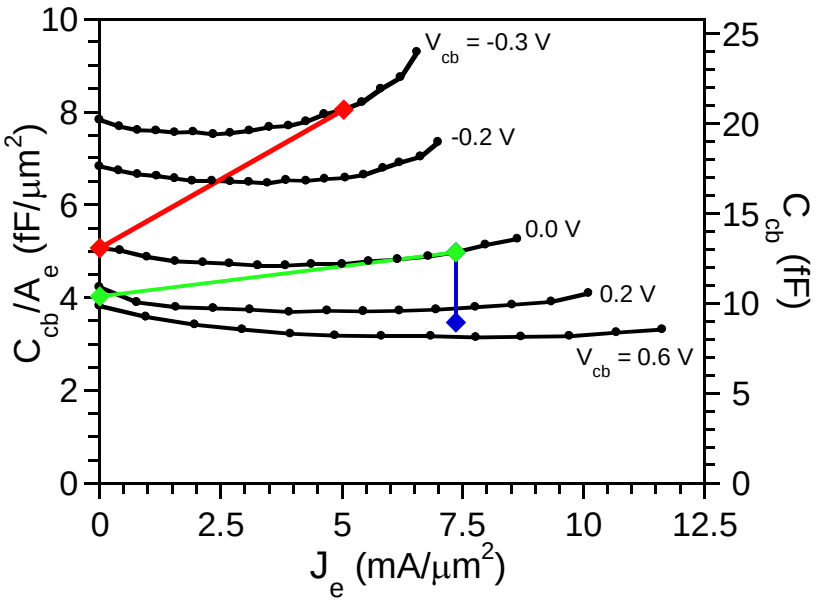
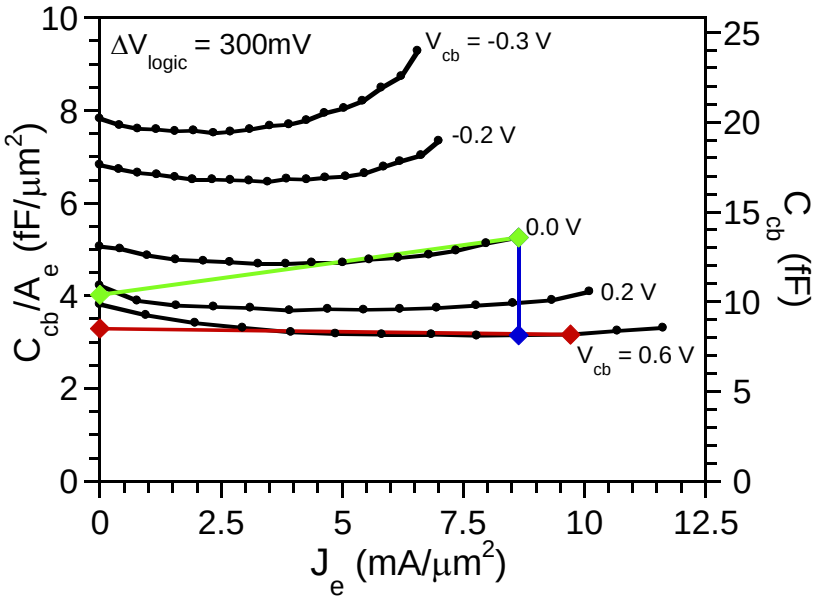


Chart 6

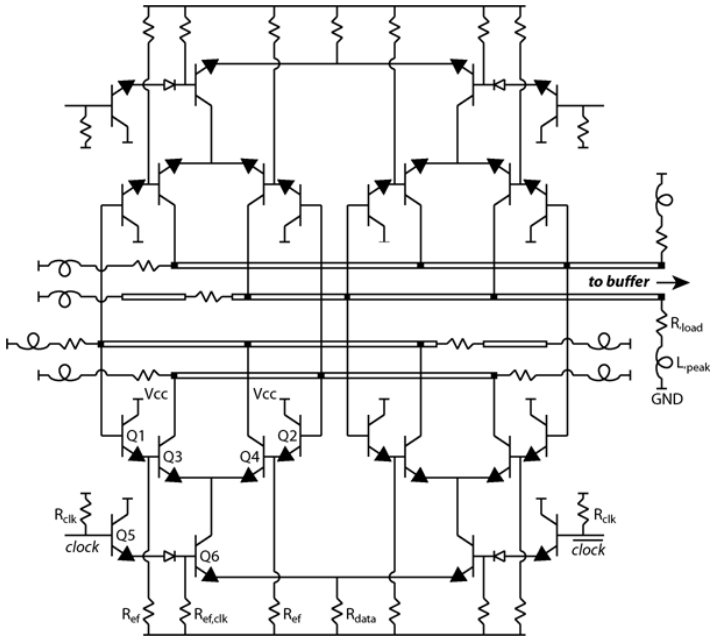




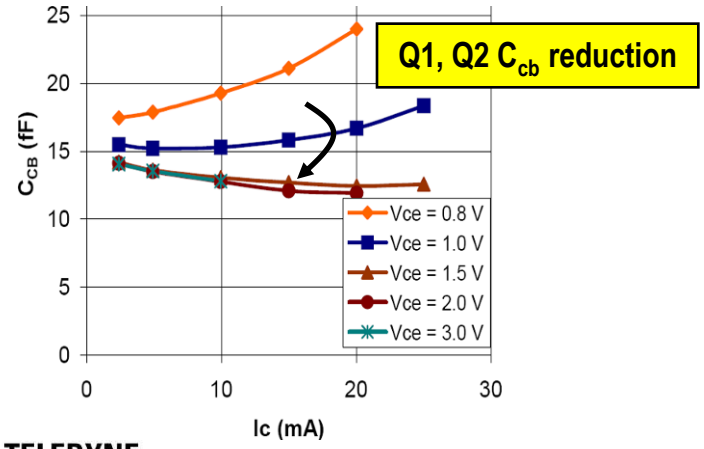
Design approach for 200GHz logic

Approach: (new design elements presented **in bold**)

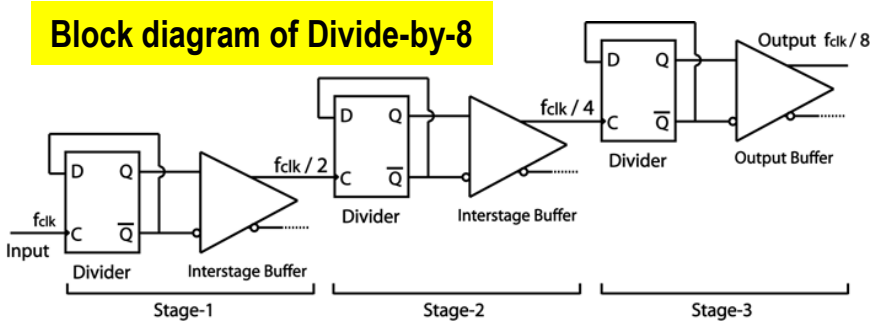
- Emitter coupled logic (ECL) topology
- Faster HBTs with lower C_{cb} and lower R_{ex} (Ω-um^2)
  - **Scaled device from 0.5um to 0.25um**
  - 150nm collector, 30nm base (400GHz f_t, 650GHz f_{max})
- Reduce signal bus and loading delays
  - **Decreased device-to-device spacing**
- Thin-film microstrip with low loss ε_r = 2.7
- Resistive pulldown voltage biasing
- Small peaking inductance L_{peak}
- **Emitter-follower HBTs having reduced C_{cb} (Q1, Q2)**
  - **Collector-base DC voltage V_{cb} increased**



Schematic of a flip-flop configured as a static divider

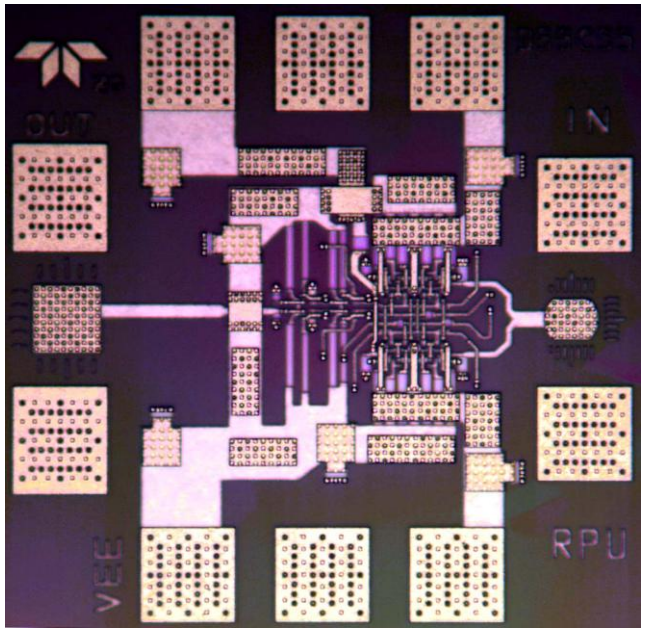


Block diagram of Divide-by-8

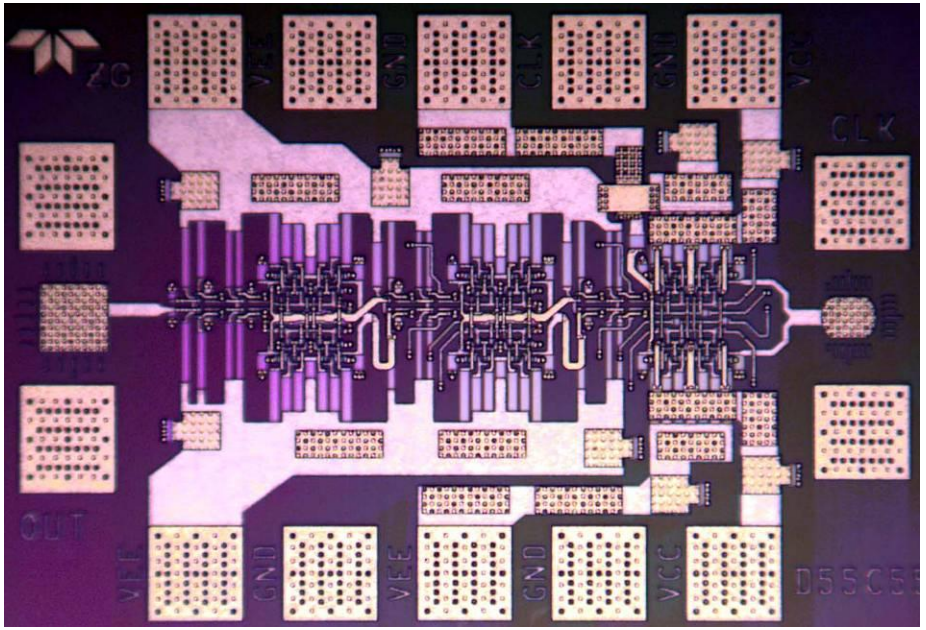


IC micrographs of the TSC 200GHz Static Frequency Dividers

Final fabrication, top-metal ground plane omitted

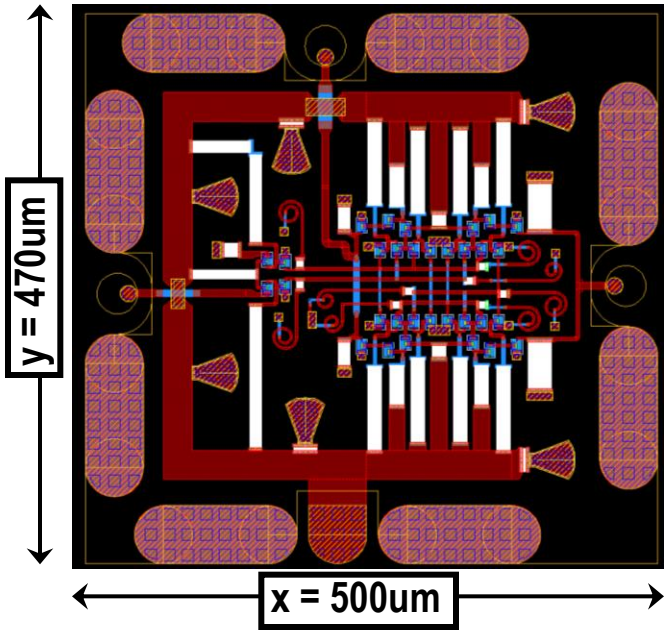


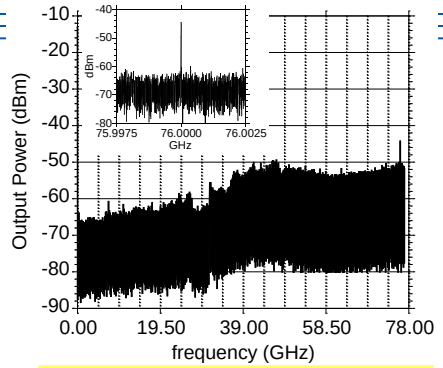
Divide-by-2 circuit, 36 HBTs (0.42×0.41-mm^2)



Divide-by-8 circuit, 108 HBTs (0.68×0.45-mm^2)

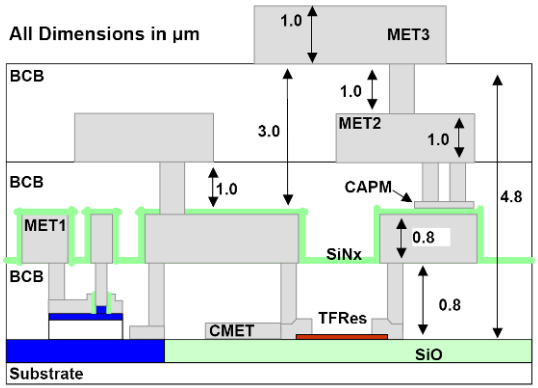
TSC/UCSB/GSC 150GHz divider (September 2004)





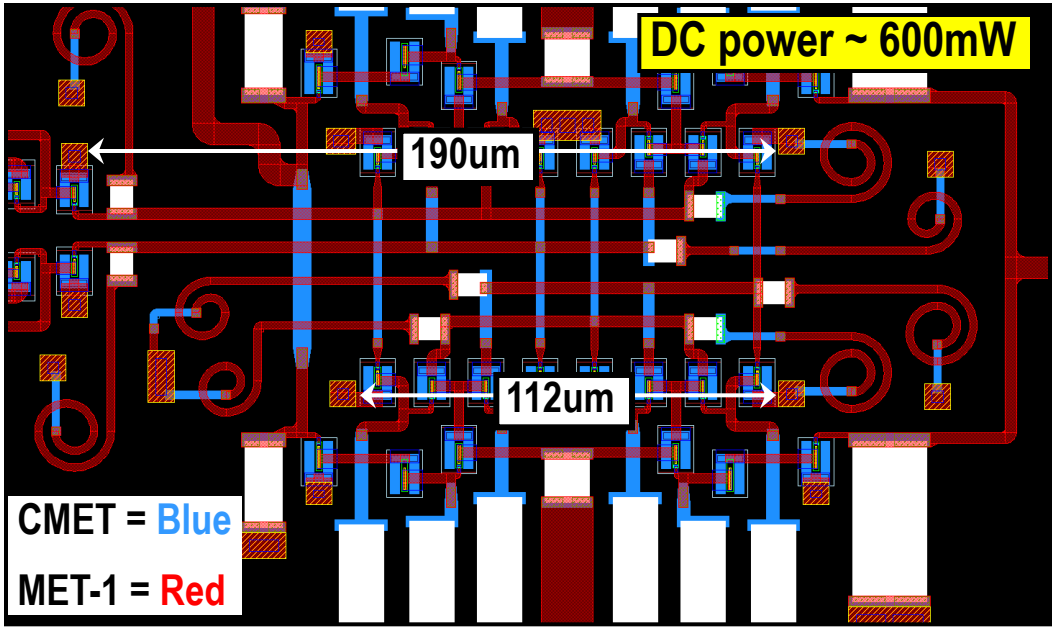
Phase-I divider @ 152GHz

Technology cross-section, phase-I



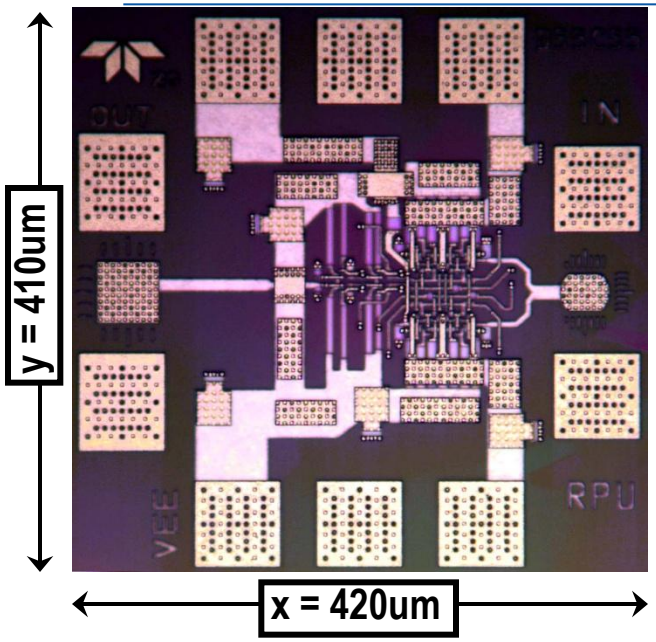
Summary of divider physical size:

- 5um device-to-device spacing
- Two-sided collector HBT
- Latch width = 112um
- Latch-to-buffer signal distance = 190um

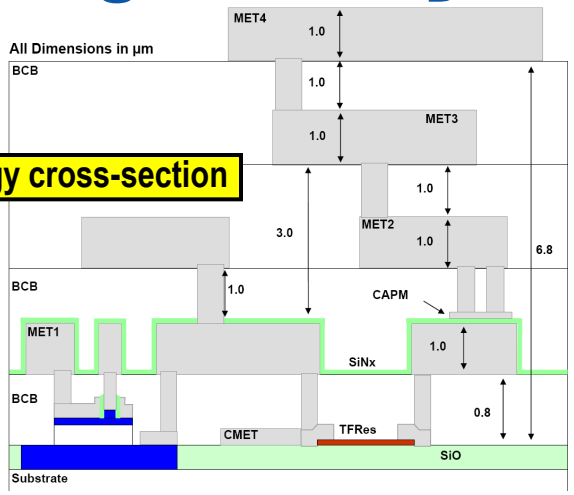


Close-up view of flip-flop interconnect, configured for divide-by-2

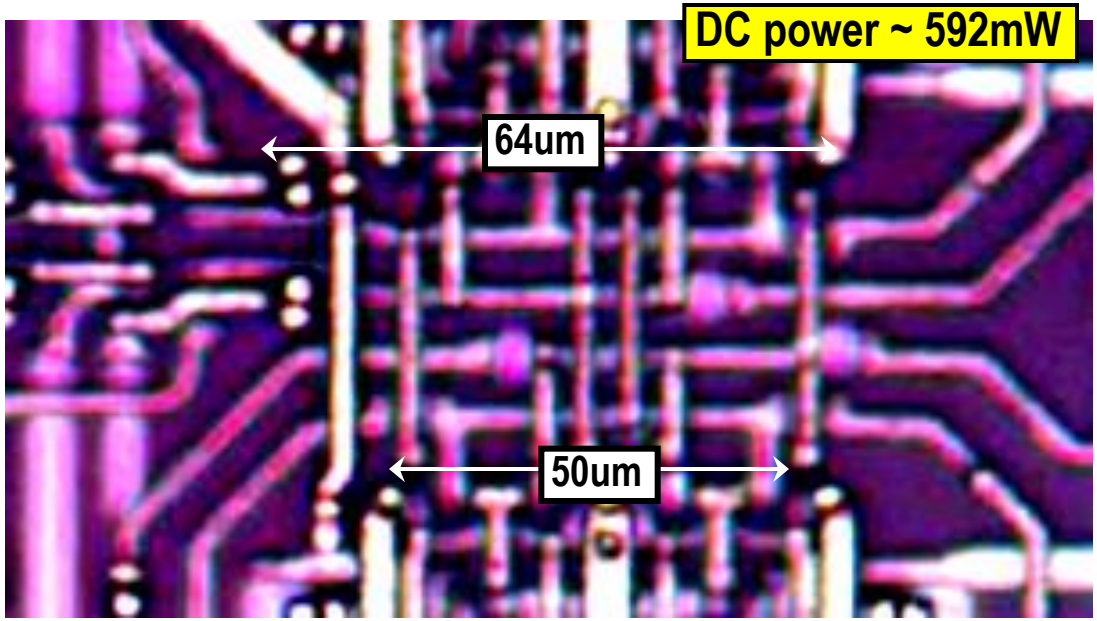
TSC/UCSB 200GHz divider – scaling summary



TSC mixed-signal technology cross-section



DC power ~ 592mW



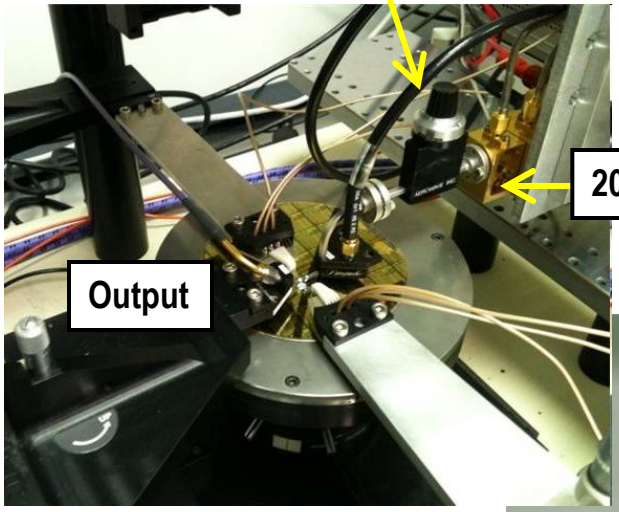
Close-up view of flip-flop interconnect, configured for divide-by-2

Summary of divider physical size:

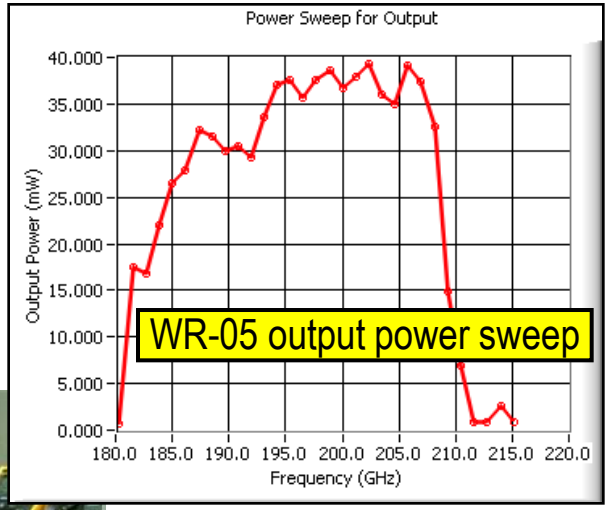
- 2um device-to-device spacing
- One-sided narrower collector HBT
- Latch width = 50um (55% reduction)
- Latch-to-buffer signal distance = 64um
  - 66% reduction

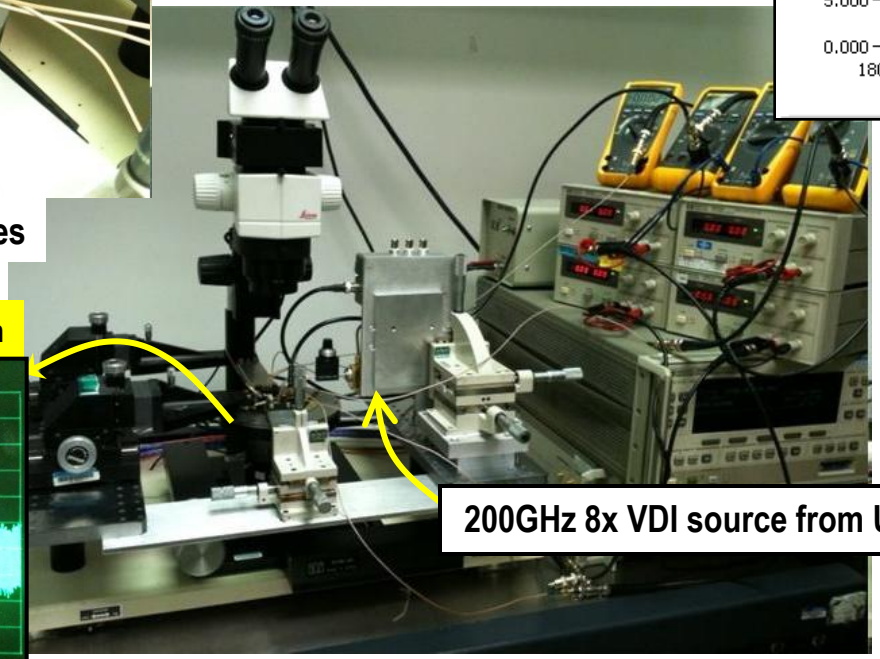
Simulated CLK rate, 213GHz

Probe-station for 200GHz divider testing

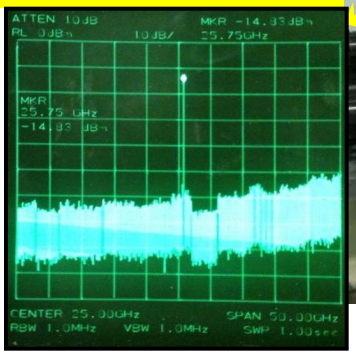


Close-up showing wafer probes



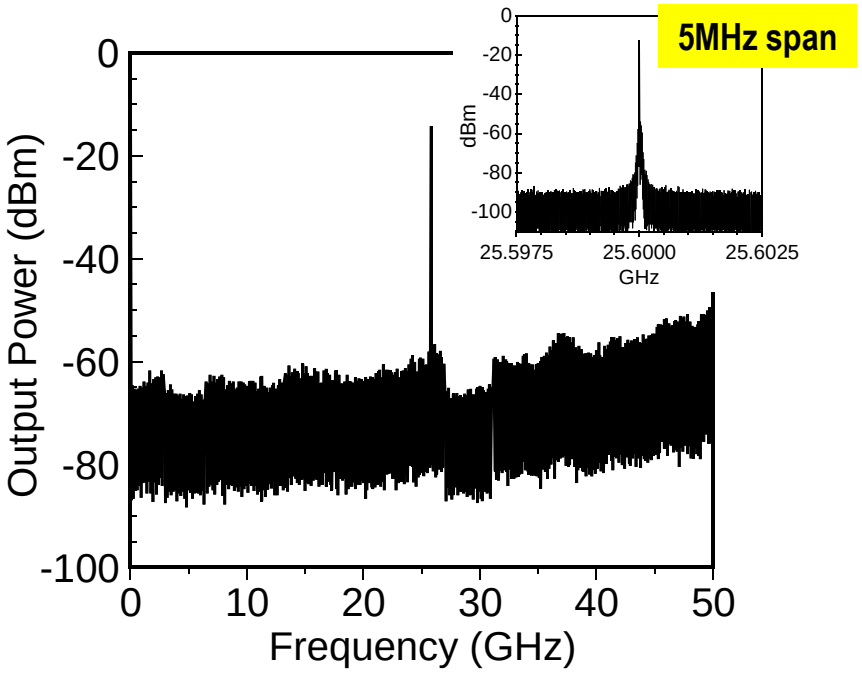


Output at 204.8GHz operation

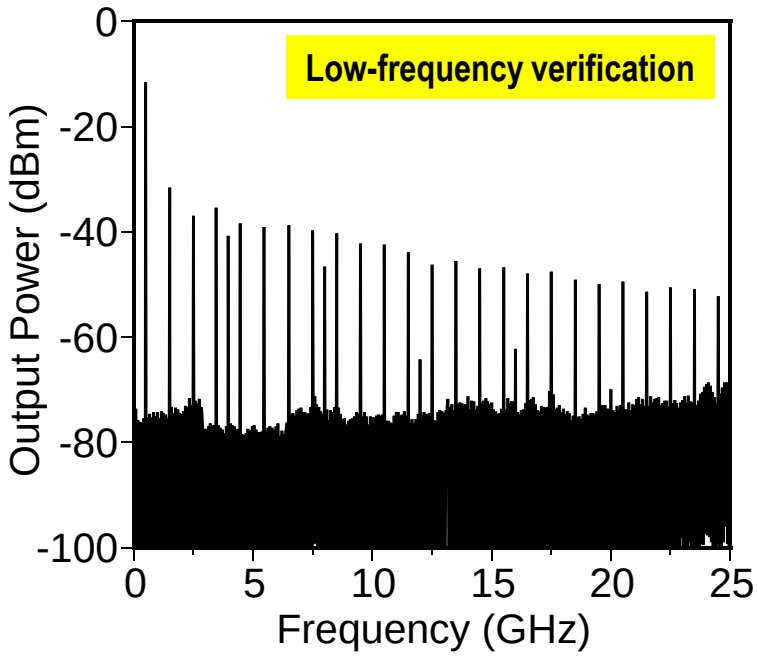


Probe station for 200GHz testing

Divide-by-8 static divider operating to 204.8GHz



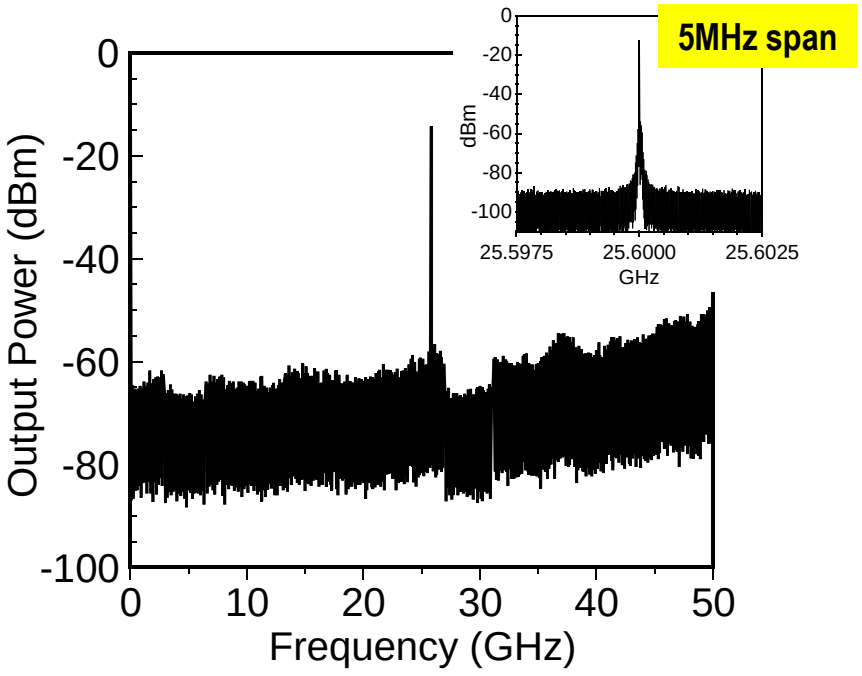
Divider output – f_{clk} = 204.8GHz, f_{out} = 25.60GHz



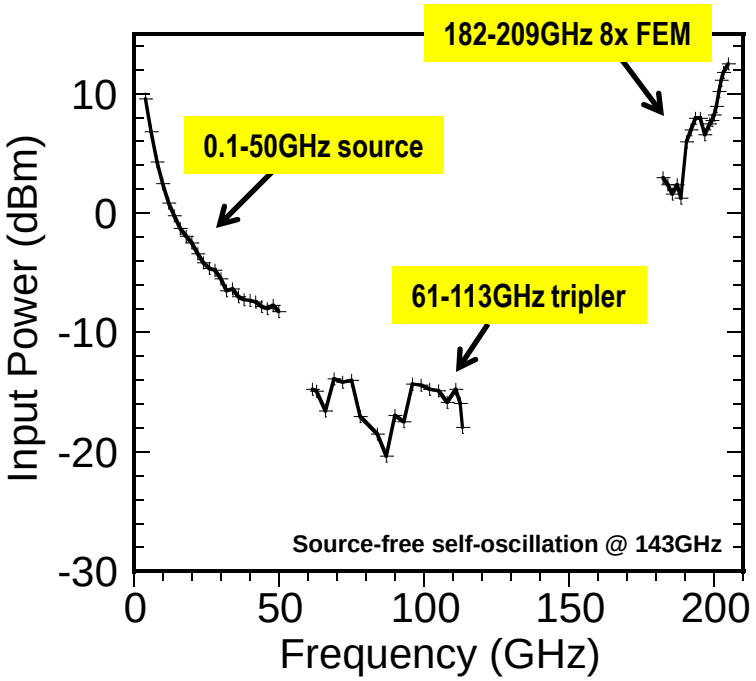
Divider output – f_{clk} = 4.0GHz, f_{out} = 500MHz

- Peak divider toggle rate is 204.8GHz
  - Expected output at 25.60GHz, no spectral content at lower frequencies
- Input divider operational down to 4.0GHz to confirm static operation at all frequencies
  - 3rd-stage divider is operating at 1.0GHz clock (differential 350mV$_{p-p}$), 500MHz final output
- P_{DC} of divide-by-8 circuit = 1.82W
  - Input divider operating at 204.8GHz, P_{DC} = 592mW

Sensitivity plot of the 204.8GHz static divider



Divider output – f_{clk} = 204.8GHz, f_{out} = 25.60GHz



Sensitivity plot, 204.8GHz static divider

- Sensitivity plot of the divider: 0.1-50GHz, 61.5-113.25GHz, 182.4-204.8GHz
- Expected trends of input power sensitivity versus frequency observed
- Source-free self oscillation (no input signal) reference to the input is 143GHz

Summary

- A record static divide-by-8 frequency divider has been demonstrated
  - 108 HBTs, all having 250nm features
  - TSC 4-metal layer, mixed-signal interconnect
  - Operational from 4.0GHz to 204.8GHz
  - Total P_{DC} = 1.82W, input divider only (no buffers) = 592mW

SUMMARY OF THE FASTEST REPORTED STATIC FREQUENCY DIVIDERS

Max. Clock Freq. (GHz)	Division Rate	Technology	Scale (nm)	Reference
110	4	SiGe HBT	140	Infinion [3]
151.6	4	InP HBT	400	HRL [4]
152.0	2	InP HBT	500	Teledyne [1]
152	4	InP HBT	500	Lucent [5]
200.6	2	InP HBT	250	NGAS [6]
204.8	8	InP HBT	250	Teledyne, this work

- Continued increases to static divider toggle rate require balanced reductions to HBT base R_{bb} and emitter resistance R_{ex}, and junction capacitances C_{je}, C_{cb}.
  - Presentation (Tues-F1) by M. Urteaga discusses recent HBT developments

Acknowledgement

- This work was supported under the DARPA TFAST program, Sanjay Raman program manager.

Thank you!!