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100+ GHz Transistor Electronics: Present and Projected Capabilities

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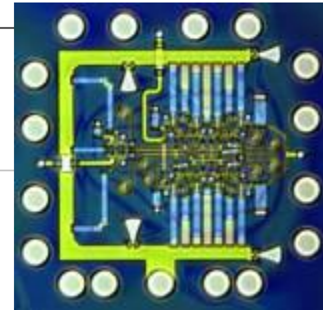
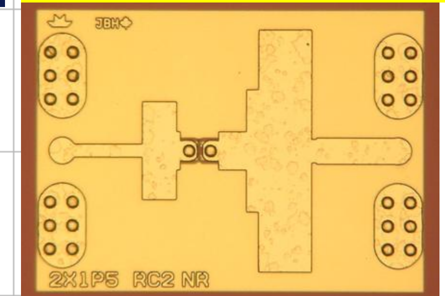
THz Transistors

Why Build THz Transistors ?

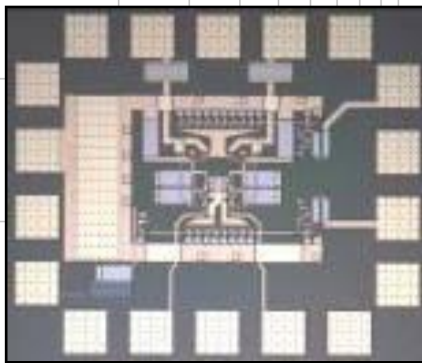
500 GHz digital logic → fiber optics



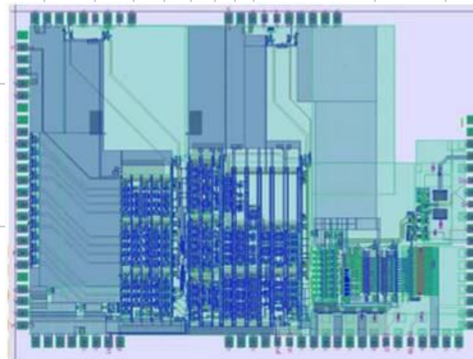
THz amplifiers→ THz radios → imaging, sensing, communications



precision analog design at microwave frequencies → high-performance receivers

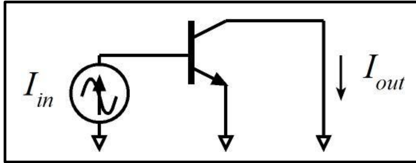


Higher-Resolution Microwave ADCs, DACs, DDSs

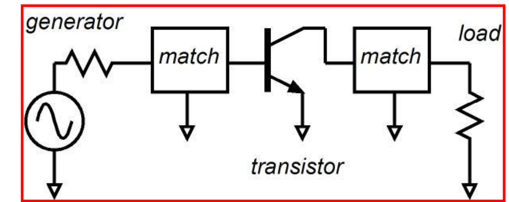


Transistor figures of Merit / Cutoff Frequencies

H_{21}=short-circuit current gain



MAG = maximum available power gain: impedance-matched



35
30
25
20
15
10
5
0

gains, dB

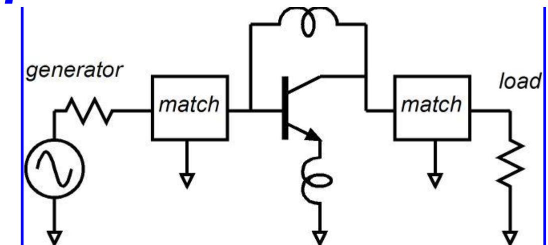
1E10
1E11
1E12
2E12

freq, Hz

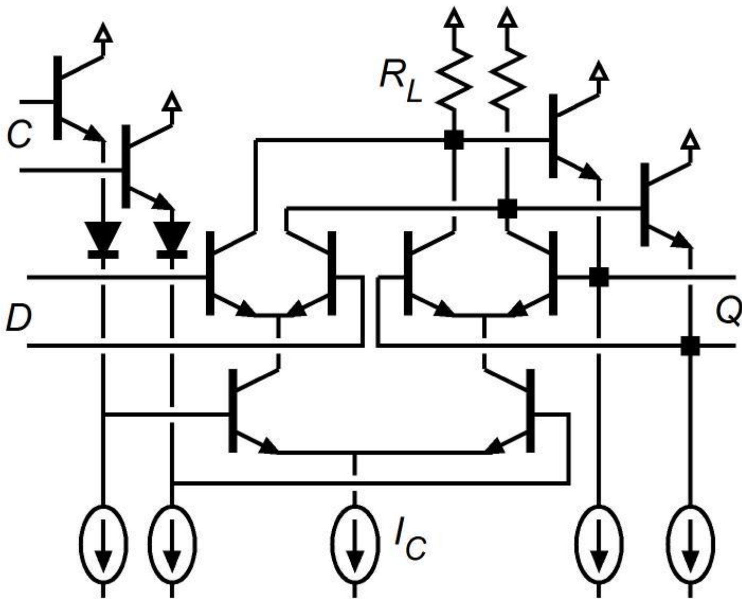
f_{max}
power-gain cutoff frequency

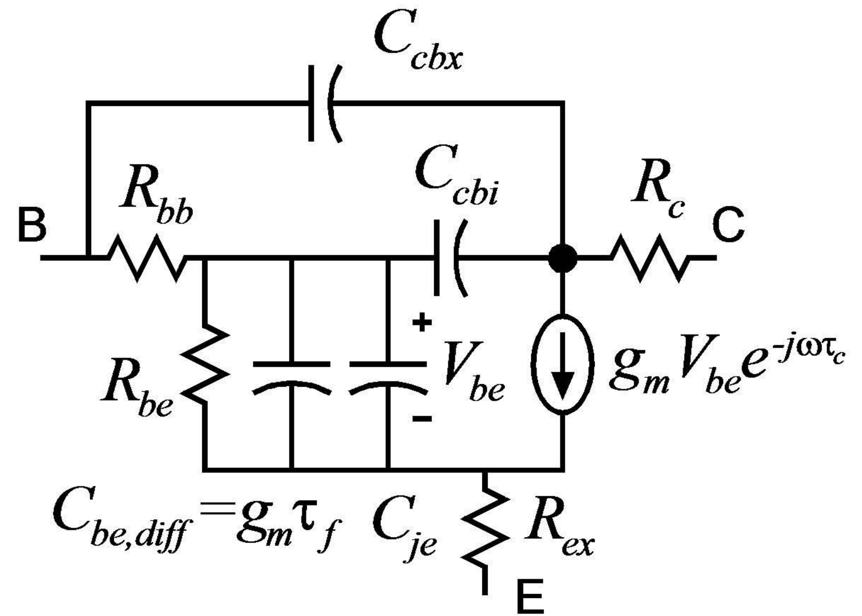
f_τ
current-gain cutoff frequency

U= unilateral power gain: feedback nulled, impedance-matched



What Determines Digital Gate Delay ?





$$
\begin{aligned}
T_{gate} \approx \tau_f &+ (\Delta V_L / I_C)(C_{je} + 6C_{cbx} + 6C_{cbi} + C_{wire}) \\
&+ (kT/qI_C)(0.5C_{je} + C_{cbx} + C_{cbi} + 0.5\tau_f I_C/\Delta V_L) \\
&+ R_{ex}(0.5C_{cbx} + 0.5C_{cbi} + 0.5\tau_f I_C/\Delta V_L) \\
&+ R_{bb}(0.5C_{je} + C_{cbi} + 0.5\tau_f I_C/\Delta V_L).
\end{aligned}
$$

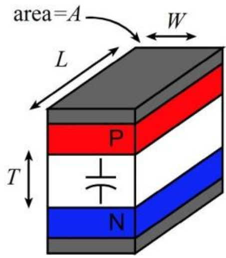
←CV/I terms dominate

analog ICs have somewhat similar bandwidth considerations...

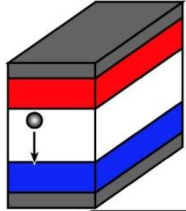
How to Make
THz Transistors

High-Speed Transistor Design

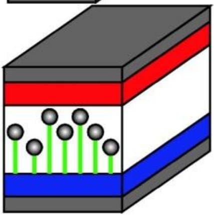
Depletion Layers



$$C = \varepsilon \cdot \frac{A}{T}$$

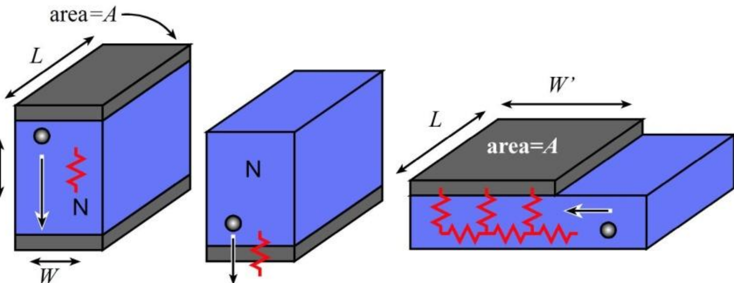


$$\tau = \frac{T}{2v}$$



$$\frac{I_{\max}}{A} = \frac{4\varepsilon v_{sat}(V_{appl} + \phi)}{T^2}$$

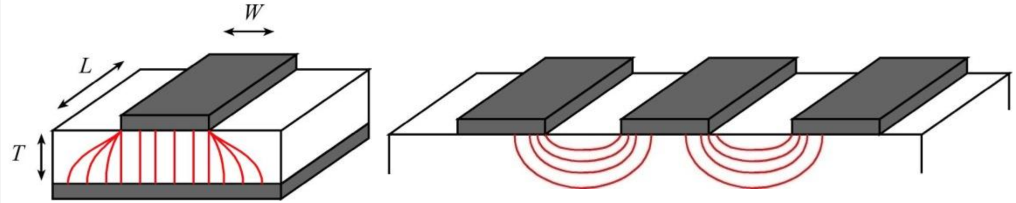
Bulk and Contact Resistances



$$R \cong \rho_{contact} / A$$

contact terms dominate

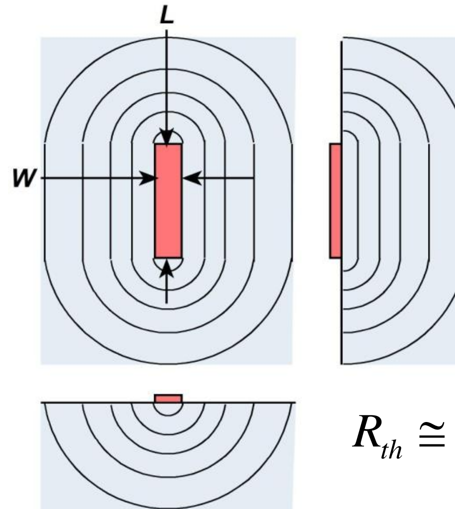
Fringing Capacitances



$$C_{finging} / L \sim \varepsilon$$

$$C_{finging} / L \sim \varepsilon$$

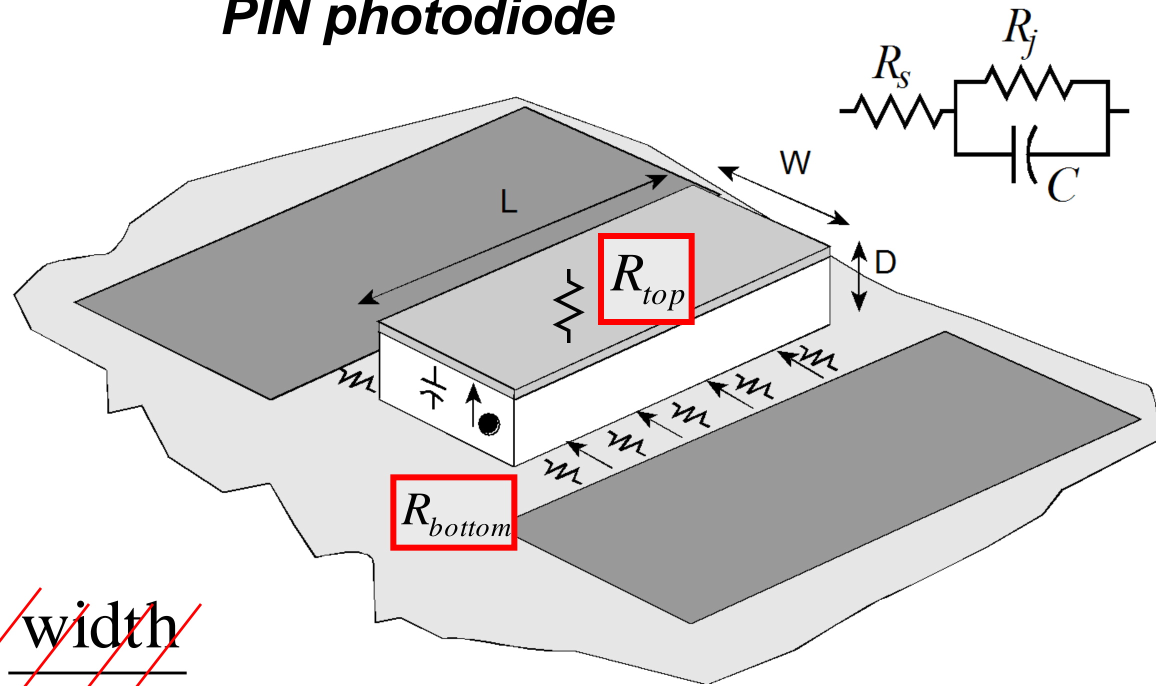
Thermal Resistance



$$R_{th} \cong \frac{1}{\pi K_{th} L} \ln\left(\frac{L}{W}\right) + \frac{1}{\pi K_{th} L}$$

Frequency Limits and Scaling Laws of (most) Electron Devices

PIN photodiode



$$\tau \propto \text{thickness}$$

$$C \propto \text{area} / \text{thickness}$$

$$R_{top} \propto \rho_{contact} / \text{area}$$

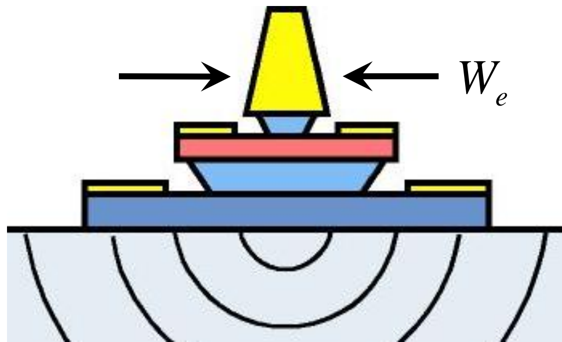
$$R_{bottom} \propto \frac{\rho_{contact}}{\text{area}} + \frac{\rho_{sheet}}{4} \cdot \frac{\text{width}}{\text{length}}$$

$$I_{\text{max, space-charge-limit}} \propto \text{area} / (\text{thickness})^2$$

$$\Delta T \propto \frac{\text{power}}{\text{length}} \times \log\left(\frac{\text{length}}{\text{width}}\right)$$

To double bandwidth,
- ***reduce thicknesses 2:1*** ***Improve contacts 4:1***
- ***reduce width 4:1, keep constant length***
- ***increase current density 4:1***

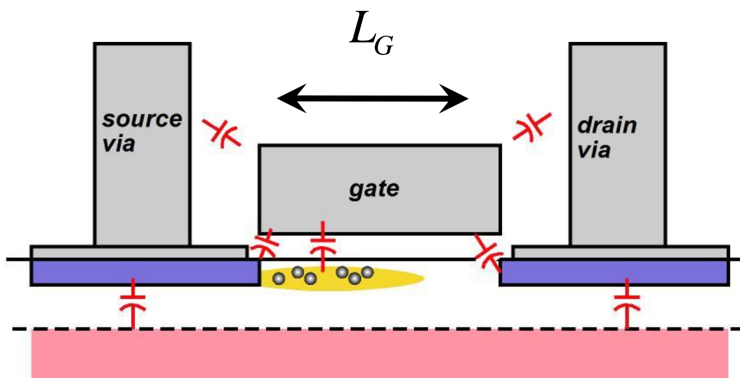
Changes required to double transistor bandwidth



(emitter length L_E)

HBT parameter	change
emitter & collector junction widths	decrease 4:1
current density (mA/μm²)	increase 4:1
current density (mA/μm)	constant
collector depletion thickness	decrease 2:1
base thickness	decrease 1.4:1
emitter & base contact resistivities	decrease 4:1

nearly constant junction temperature → linewidths vary as (1 / bandwidth)²



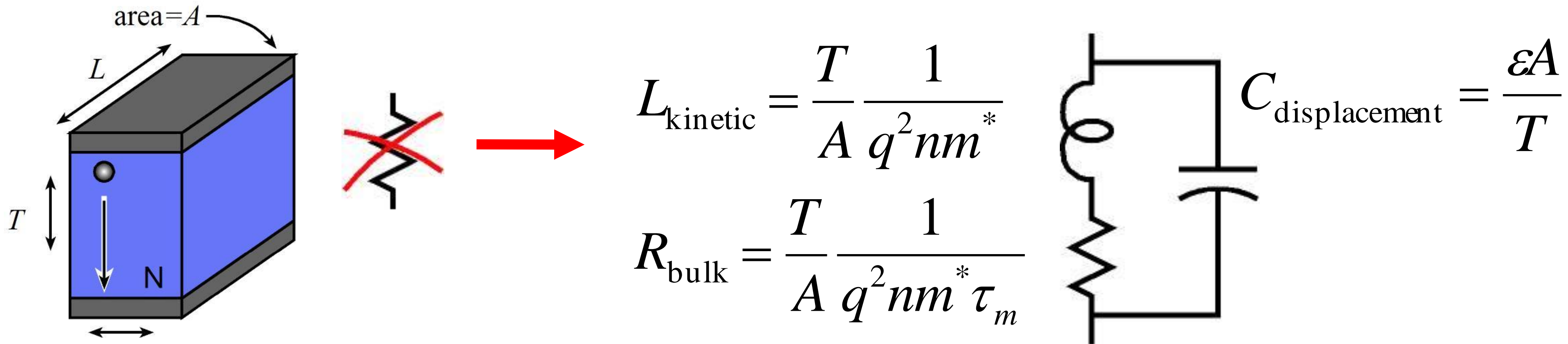
(gate width W_G)

FET parameter	change
gate length	decrease 2:1
current density (mA/μm), g_m (mS/μm)	increase 2:1
channel 2DEG electron density	increase 2:1
gate-channel capacitance density	increase 2:1
dielectric equivalent thickness	decrease 2:1
channel thickness	decrease 2:1
channel density of states	increase 2:1
source & drain contact resistivities	decrease 4:1

constant voltage, constant velocity scaling

fringing capacitance does not scale → linewidths scale as (1 / bandwidth)

Electron Plasma Resonance: Not a Dominant Limit



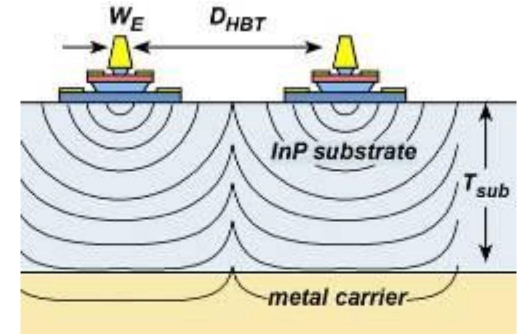
	dielectric relaxation frequency $f_{dielectric} = \frac{1/2\pi}{C_{displacement} R_{bulk}}$ $= \frac{1}{2\pi} \frac{\sigma}{\varepsilon}$	scattering frequency $f_{scattering} = \frac{1}{2\pi} \frac{R_{bulk}}{L_{kinetic}}$ $= \frac{1}{2\pi\tau_m}$	plasma frequency $f_{plasma} = \frac{1/2\pi}{\sqrt{L_{kinetic} C_{displacement}}}$
n - InGaAs $3.5 \cdot 10^{19} / \mathrm{cm}^3$	800 THz	7 THz	74 THz
p - InGaAs $7 \cdot 10^{19} / \mathrm{cm}^3$	80 THz	12 THz	31 THz

Thermal Resistance Scaling : Transistor, Substrate, Package

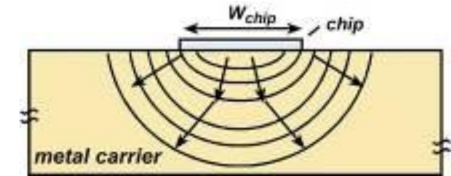
cylindrical heat flow near junction — spherical flow for $r > L_e$ — planar flow for $r > D_{HBT}/2$

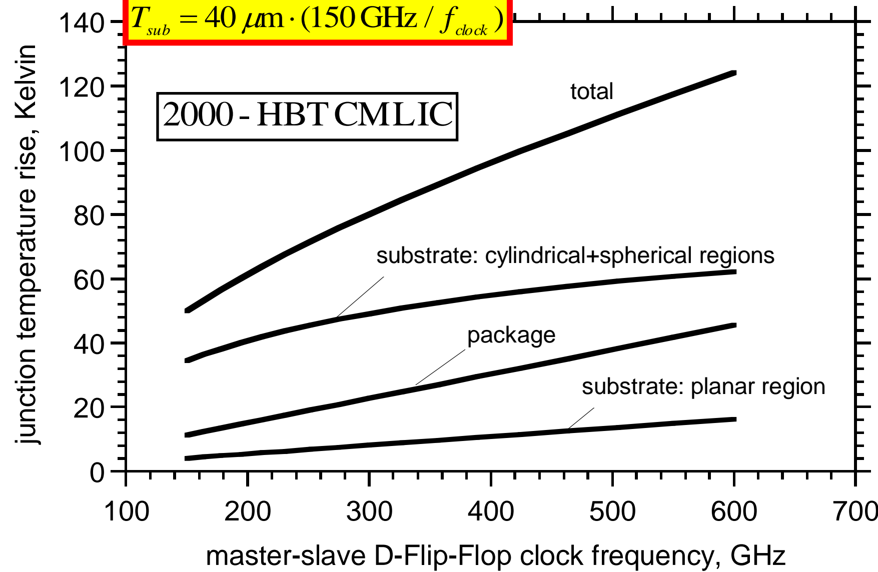
$$\Delta T_{\text{substrate}} \cong \frac{P}{\pi K_{InP} L_E} \ln\left(\frac{L_e}{W_e}\right) + \frac{P}{\pi K_{InP}}\left(\frac{1}{L_E} - \frac{1}{D}\right) + \frac{P}{K_{InP}} \cdot \left(\frac{T_{sub} - D/2}{D^2}\right)$$

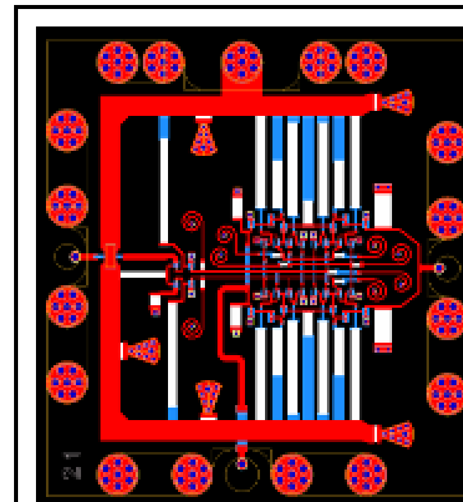
increases logarithmically — insignificant variation — increases quadratically if T_{sub} is constant



$$\Delta T_{package} \cong \left(\frac{1}{4} + \frac{1}{\pi}\right)\frac{P_{chip}}{K_{Cu} W_{chip}}$$





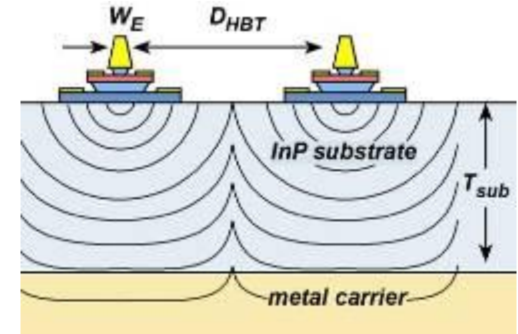


Wiring lenghts scale as 1/bandwidth. Power density, scales as $(\text{bandwidth})^2$.

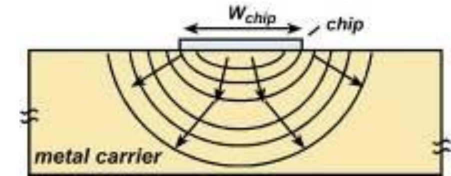
Thermal Resistance Scaling : Transistor, Substrate, Package

$$\Delta T_{\text{substrate}} \cong \underbrace{\frac{P}{\pi K_{InP} L_E} \ln\left(\frac{L_e}{W_e}\right)}_{\text{cylindrical heat flow near junction}} + \underbrace{\frac{P}{\pi K_{InP}}\left(\frac{1}{L_E} - \frac{1}{D}\right)}_{\text{spherical flow for } r > L_e} + \underbrace{\frac{P}{K_{InP}} \cdot \left(\frac{T_{sub} - D/2}{D^2}\right)}_{\text{planar flow for } r > D_{HBT}/2}$$

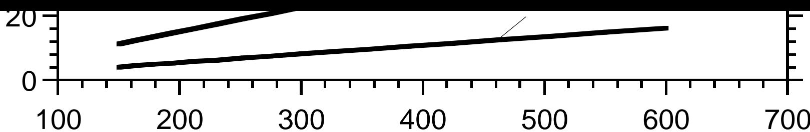
increases logarithmically | insignificant variation | increases quadratically if T_{sub} is constant

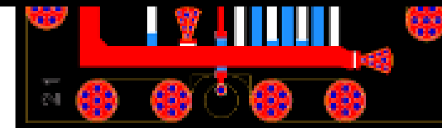


$$\Delta T_{package} \cong \left(\frac{1}{4} + \frac{1}{\pi}\right) \frac{P_{chip}}{K_{Cu} W_{chip}}$$



$T_{sub} = 40\ \mu m \cdot (150\ \text{GHz} / f_{clock})$





$(\text{bandwidth})^2$.

Probable best solution:

Thermal Vias ~500 nm below InP subcollector

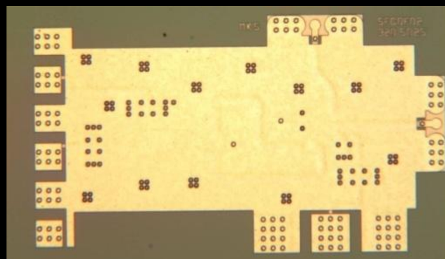
...over full active IC area.

Bipolar Transistors

256 nm InP HBT

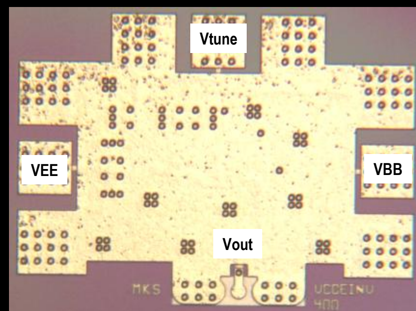
340 GHz dynamic frequency divider

M. Seo, UCSB/TSC



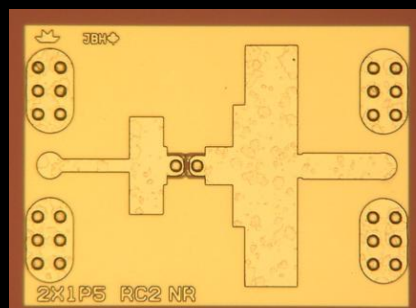
340 GHz VCO

M. Seo, UCSB/TSC
IMS 2010



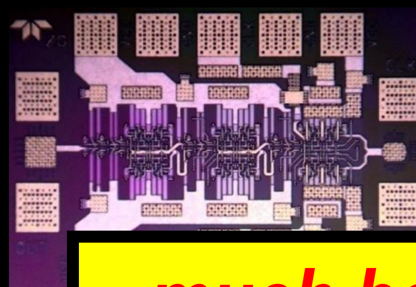
324 GHz amplifier

J. Hacker, TSC
IMS 2010

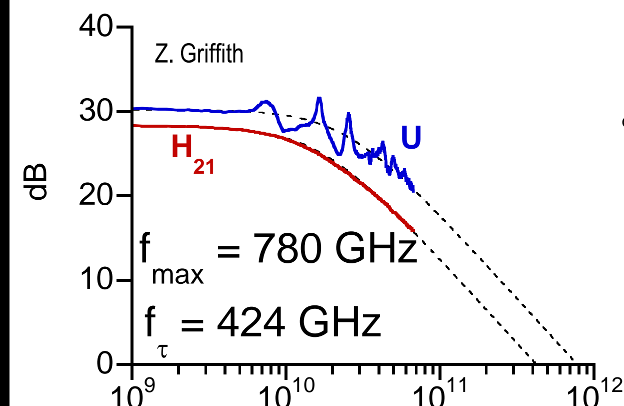


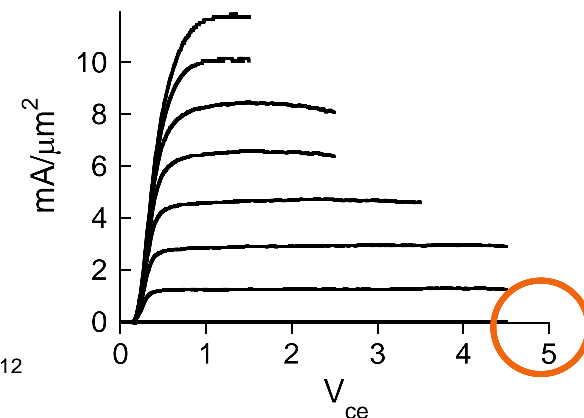
204 GHz static frequency divider

Z. Griffith, TSC
CSIC 2010:
to be presented

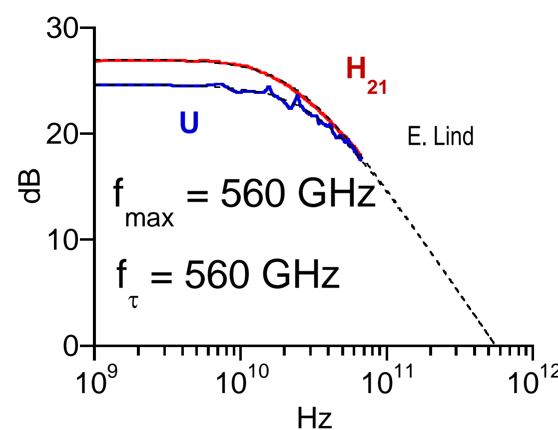


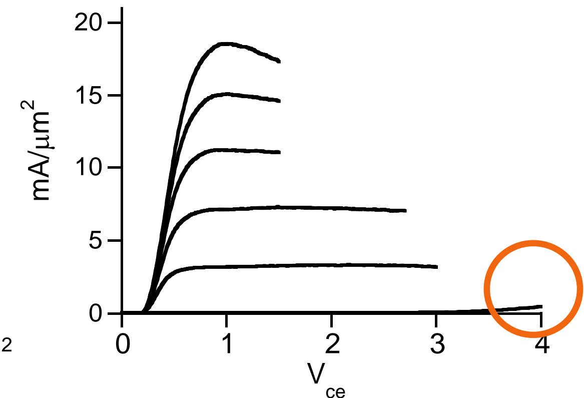
150 nm thick collector

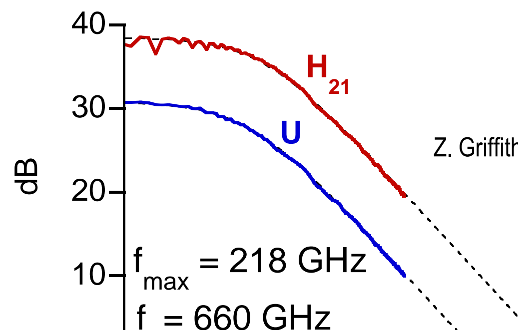


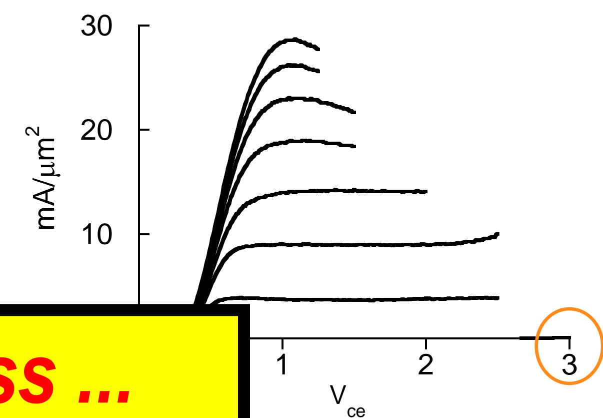


70 nm thick collector





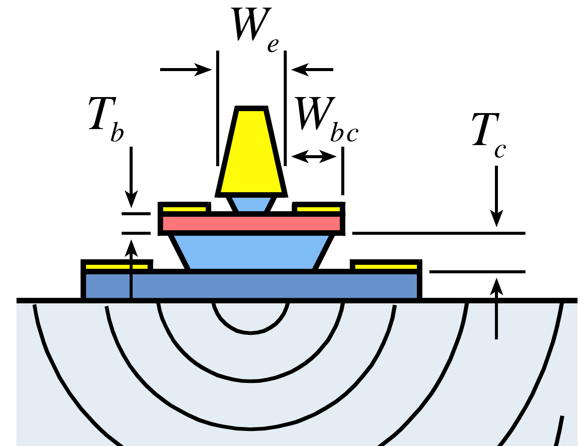




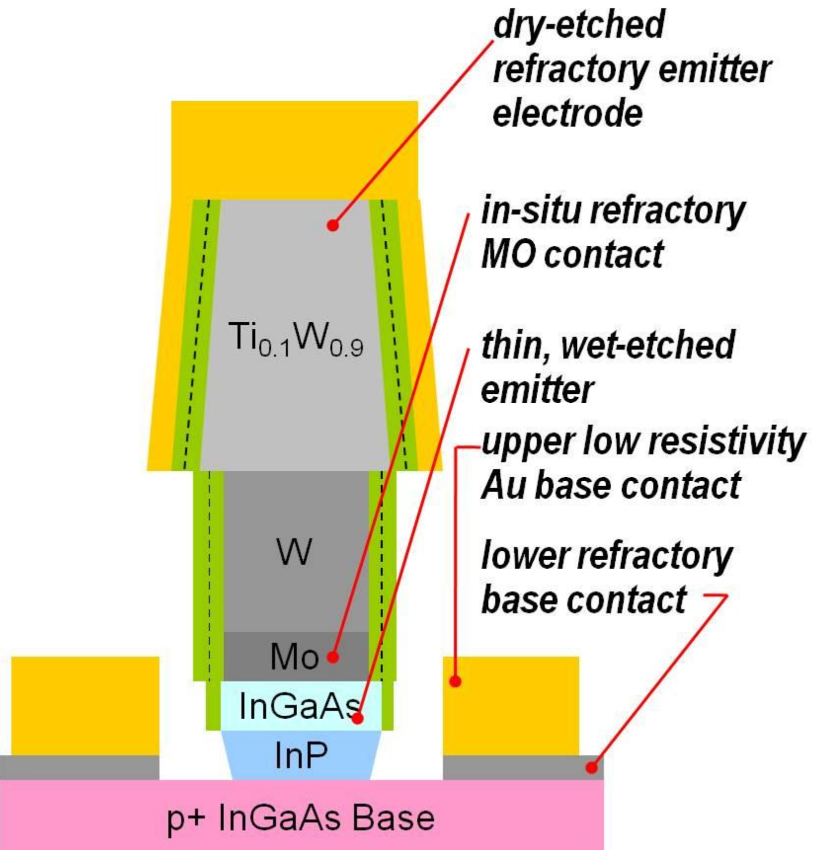
much better results in press ...

InP Bipolar Transistor Scaling Roadmap

emitter	512	256	128	64	32 nm width
	16	8	4	2	1 $\Omega\cdot\mu m^2$ access ρ
base	300	175	120	60	30 nm contact width,
	20	10	5	2.5	1.25 $\Omega\cdot\mu m^2$ contact ρ
collector	150	106	75	53	37.5 nm thick,
	4.5	9	18	36	72 $mA/\mu m^2$ current density
	4.9	4	3.3	2.75	2-2.5 V, breakdown
f_τ	370	520	730	1000	1400 GHz
f_{max}	490	850	1300	2000	2800 GHz
power amplifiers	245	430	660	1000	1400 GHz
digital 2:1 divider	150	240	330	480	660 GHz

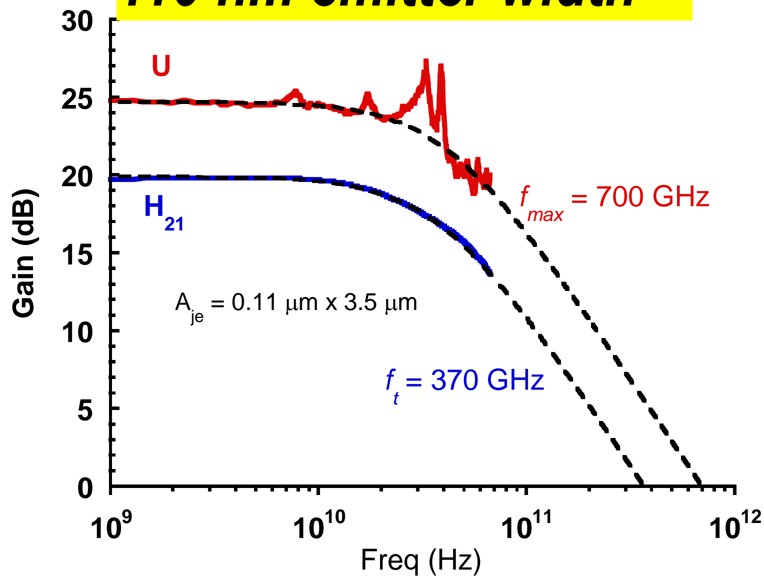


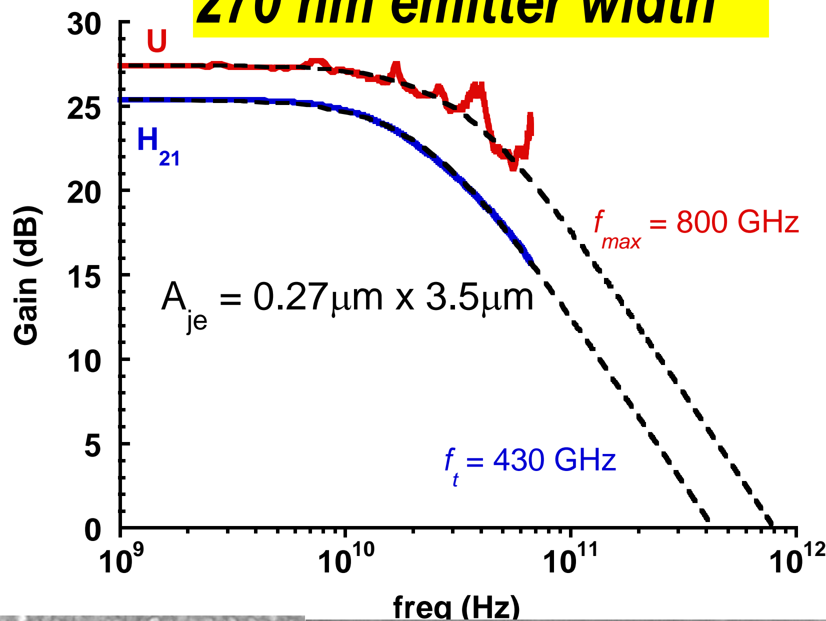
Fabrication Process for 128 nm & 64 nm InP HBTs

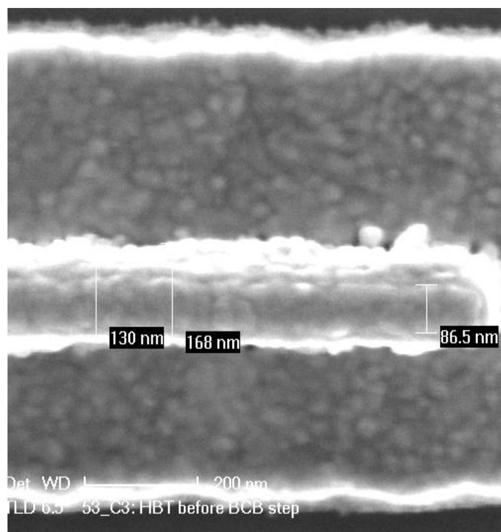


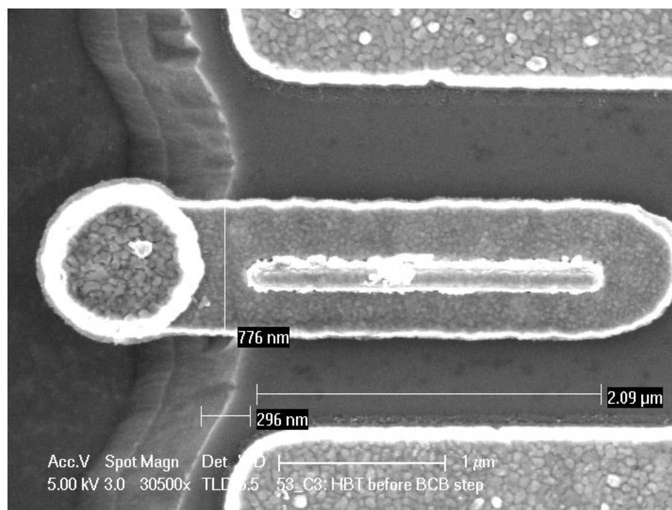
70 nm

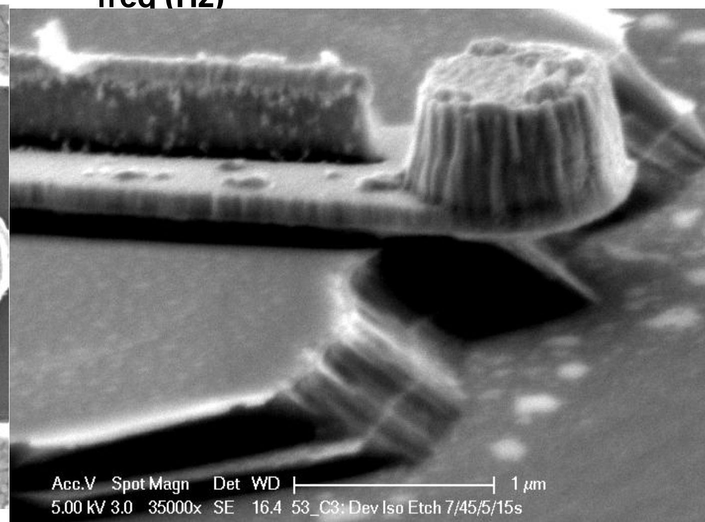
Initial Results: Refractory-Contact HBT Process





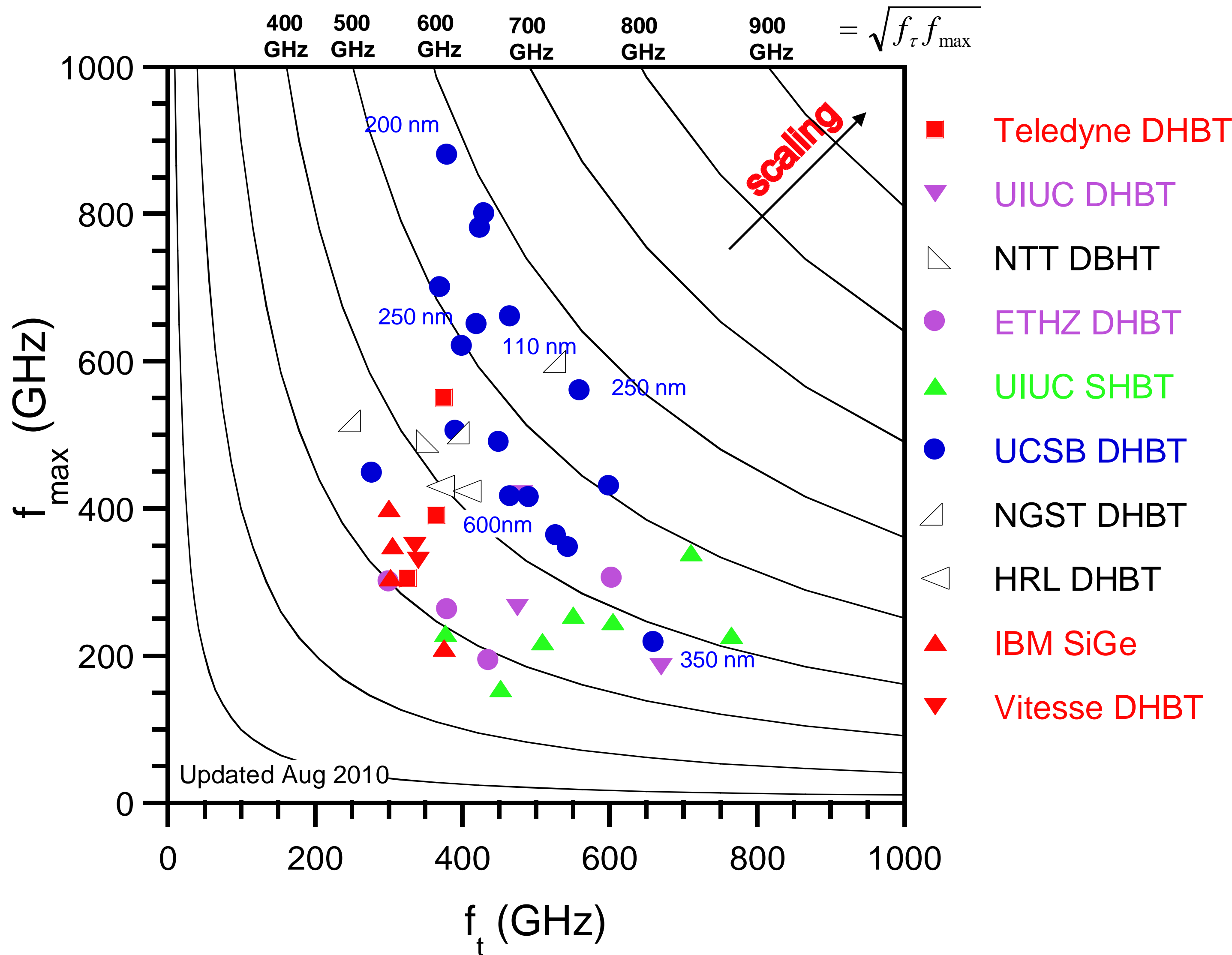






Need to add E-beam defined base, best base contact technology

InP DHBTs: August 2010



popular metrics:

f_τ or f_{max} alone

$(f_\tau + f_{max})/2$

$\sqrt{f_\tau f_{max}}$

$(1/f_\tau + 1/f_{max})^{-1}$

much better metrics:

<u>power amplifiers:</u>

PAE, associated gain,

mW/μm

<u>low noise amplifiers:</u>

F_{min}, associated gain,

<u>digital:</u>

f_{clock}, hence

$(C_{cb}\Delta V / I_c)$,

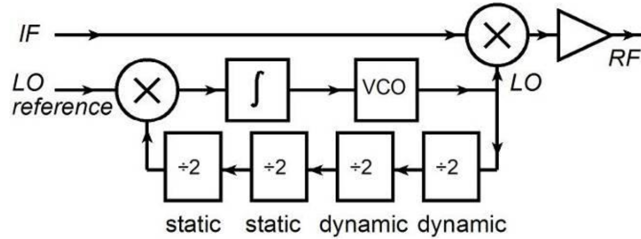
$(R_{ex} I_c / \Delta V)$,

$(R_{bb} I_c / \Delta V)$,

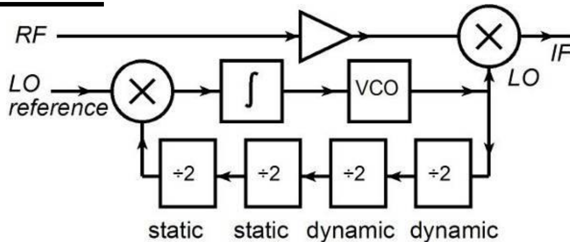
$(\tau_b + \tau_c)$

670 GHz Transceiver Simulations in 128 nm InP HBT

transmitter exciter



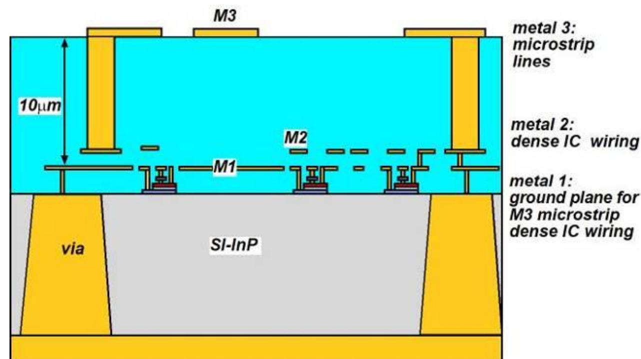
receiver



3-layer thin-film THz interconnects

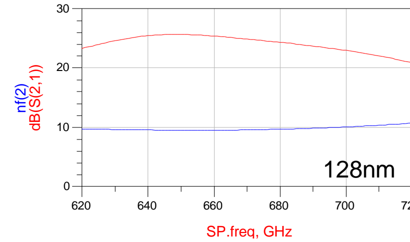
thick-substrate--> high-Q TMIC

thin -> high-density digital

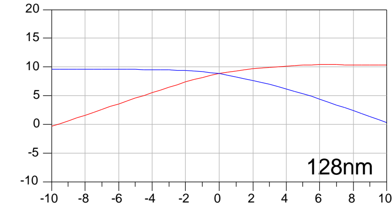


Simulations @ 670 GHz (128 nm HBT)

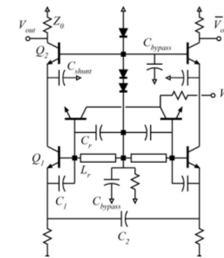
LNA: 9.5 dB Fmin at 670 GHz

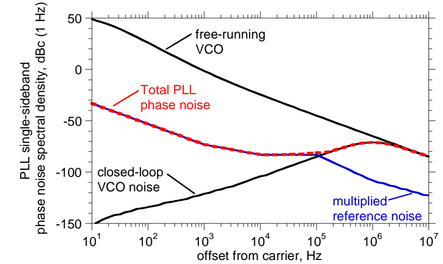


PA: 9.1 dBm Pout at 670 GHz

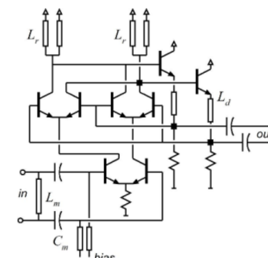


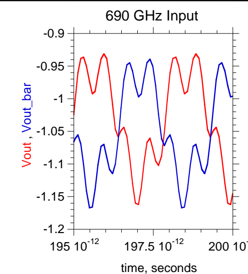
VCO:
-50 dBc (1 Hz)
@ 100 Hz offset
at 620 GHz (phase 1)

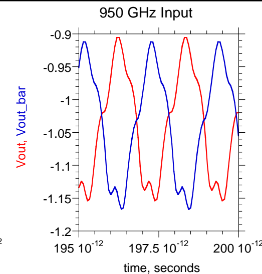




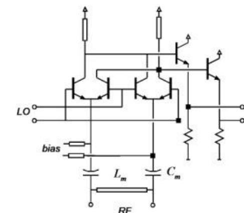
Dynamic divider:
novel design,
simulates to 950 GHz

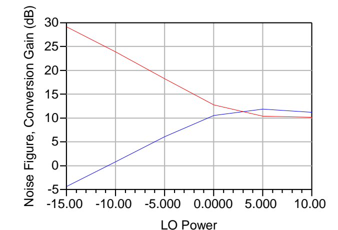






Mixer:
10.4 dB noise figure
11.9 dB gain

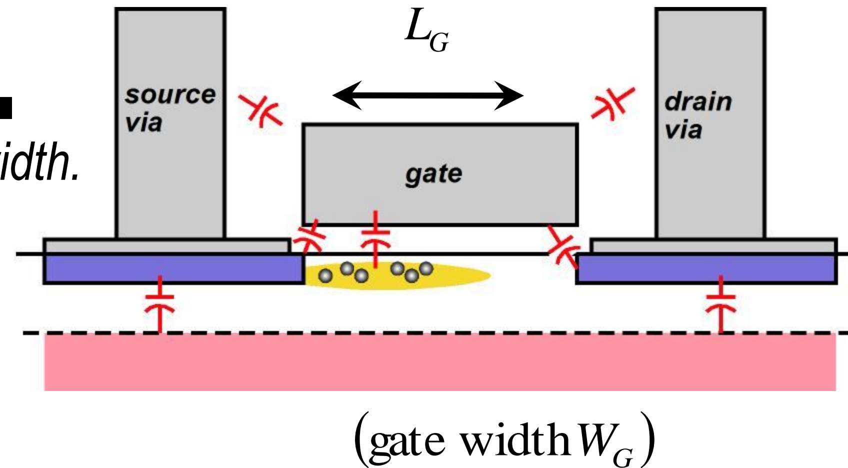




THz
Field-Effect Transistors

(THz HEMTs)

FET Scaling Laws

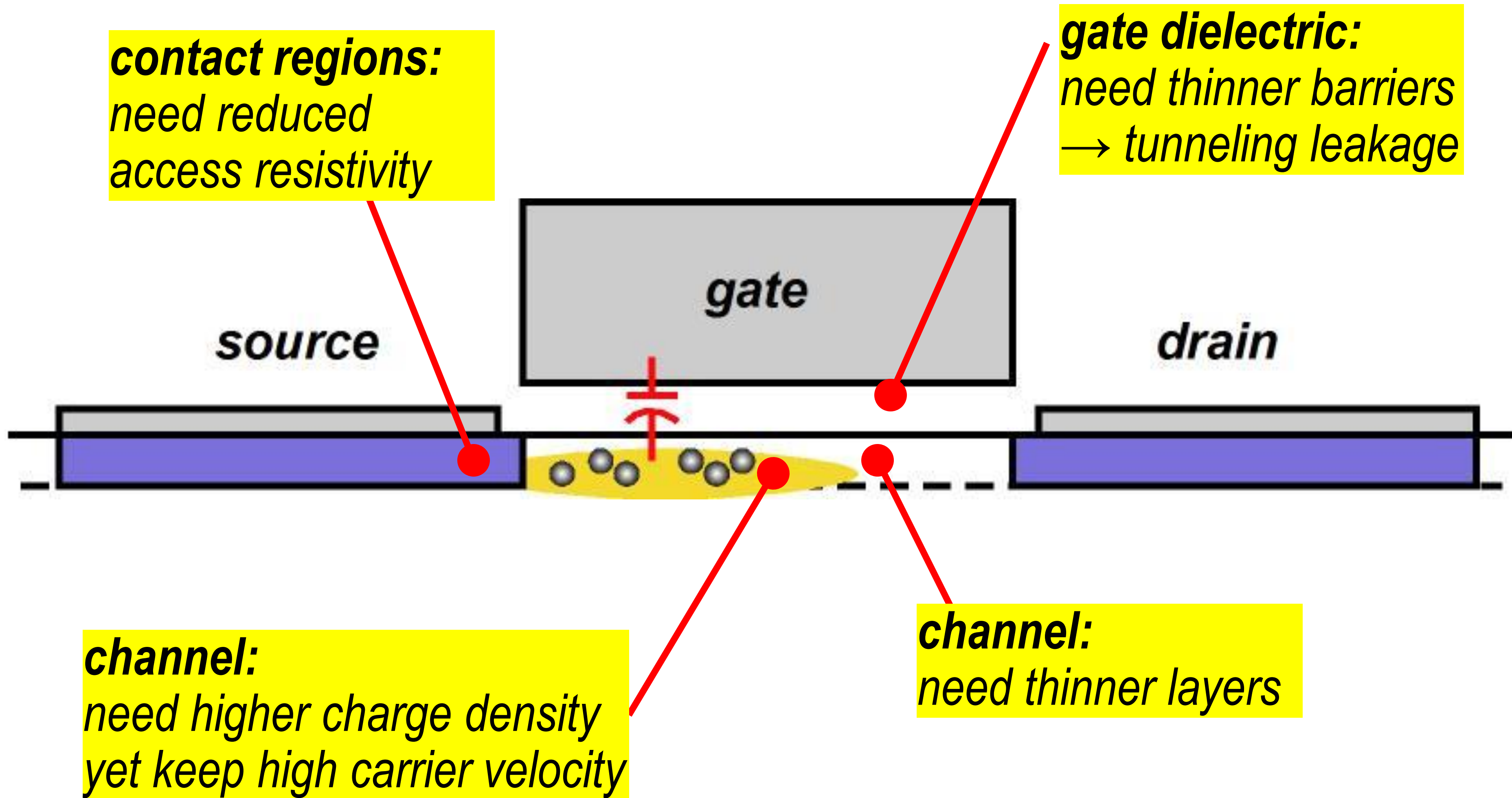


Changes required to double device / circuit bandwidth.

laws in constant-voltage limit:

FET parameter	change
gate length	decrease 2:1
current density (mA/μm), g_m (mS/μm)	increase 2:1
channel 2DEG electron density	increase 2:1
electron mass in transport direction	constant
gate-channel capacitance density	increase 2:1
dielectric equivalent thickness	decrease 2:1
channel thickness	decrease 2:1
channel density of states	increase 2:1
source & drain contact resistivities	decrease 4:1

HEMT/MOSFET Scaling: Four Major Challenges



THz FET Scaling Roadmap

← ? →

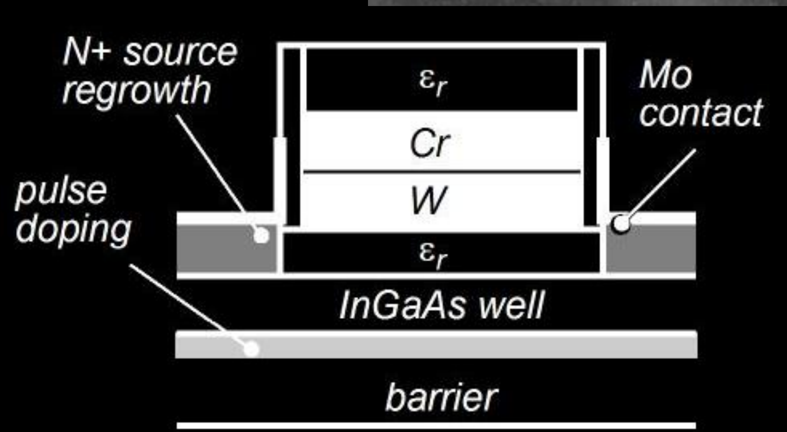
Gate length	nm	35	25	18	13	9
Gate barrier EOT	nm	0.83	0.58	0.41	0.29	0.21
well thickness	nm	5.7	4.0	2.8	2.0	1.4
S/D resistance	Ω–μm	150	100	74	53	37
effective mass	$*m_0$	0.05	0.05	0.08	0.08	0.08
# band minima		1	1	2	3	3
f_τ	GHz	700	**770**	**1100**	**1600**	**2300**
f_{max}	GHz	810	**930**	**1400**	**2000**	**2900**
$f_{divider}$ source-coupled logic	GHz	150	**220**	**300**	**430**	**580**
I_d/W_g @ 200 mV overdrive	mA/μm	0.54	0.69	0.95	1.4	1.8

high-K gate dielectrics (0.29, 0.21 EOT) — **source / drain regrowth** (74, 53, 37 S/D resistance) — **Γ-L transport** (2, 3, 3 band minima)

III-V MOSFETs with Source/Drain Regrowth

27 nm InGaAs MOSFET

100 nm



Regarding
Mixed-Signal ICs
&
Waveform Generation

Clock Timing Jitter in ADCs and DACs

Timing jitter is quantitatively specified by the single-sideband phase noise spectral density L(f).

IC oscillator phase noise varies as ~$1/f^2$ or ~$1/f^3$ near carrier

Impact on ADCs and DACs:
imposition of $1/f^n$ sidebands on signal of relative amplitude L(f)
...not creation of a broadband noise floor.

Dynamic range of electronic DACs & ADCs is limited by factors other than the phase noise of the sampling clock

Why ADC Resolution Decreases With Sample Rate

Dynamic Range Determined by Circuit Settling Time vs. Clock Period

dynamic hysteresis

metastability

ΔV_{logic}

$T_{regen} = \tau * \ln(\Delta V_{logic} / A_v V_{in})$

$T_{load} = \tau * \ln(\Delta V_{logic} / A_v V_{in})$

$A_v V_{in}$

load input

latch / regenerate

load input

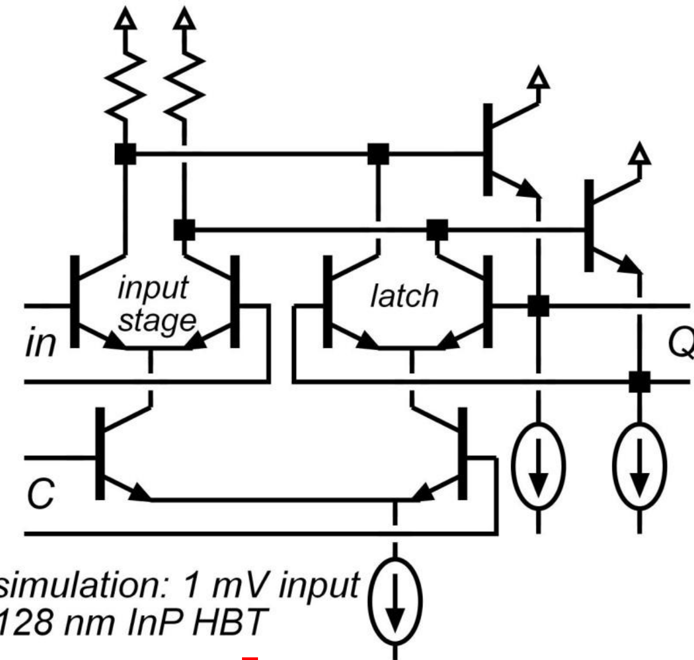
latch / regenerate

latch output voltage

0.3
0.2
0.1
0.0
-0.1
-0.2
-0.3

0 5 10 15 20 25 30 35 40 45 50

time, ps

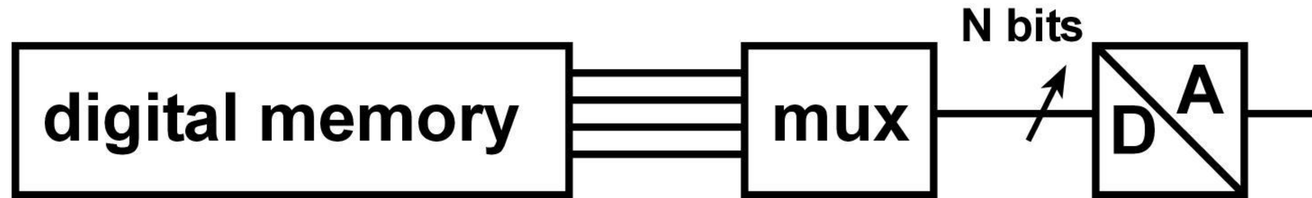


simulation: 1 mV input
128 nm InP HBT

$$\# \text{bits} \propto \frac{1}{f_{\text{sample}} \tau_{\text{latch}}}$$

IC time constants→ Resolution decreases at high sample rates

Fast IC Waveform Generation: General Prospects



Waveform generator → fast digital memory & DAC

Parallel digital memory and 200 Gb/s MUX is feasible
cost limits: power & system complexity vs. # bits, GS/s

Performance limit: speed vs. resolution of DAC
faster technologies → increased sample rates

Feasible ADC resolution:
12 SNR bits @ 4 GS/s feasible using 500 nm (400GHz) InP HBT.
Feasible sample rate will scale with technology speed..

THz Transistors
&
Mixed-Signal ICs

Few-THz Transistors

Few-THz InP Bipolar Transistors: can it be done ?

Scaling limits: contact resistivities, device and IC thermal resistances.

62 nm (1 THz f_{τ}, 1.5 THz f_{max}) scaling generation is feasible.

700 GHz amplifiers, 450 GHz digital logic

Is the 32 nm (1 THz amplifiers) generation feasible ?

Few-THz InP Field-Effect Transistors: can it be done?

challenges are gate barrier, vertical scaling,
source/drain access resistance, channel density of states.

2DEG carrier concentrations must increase.

S/D regrowth offers a path to lower access resistance.

Solutions needed for gate barrier: possibly high-k (MOSFET)

Implications: 1 THz radio ICs, ~200-400 GHz digital ICs, 20 GHz ADCs/DACs