Demonstration of a Linear Ultra-Compact Integrated Coherent Receiver

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***Abstract*—We demonstrate the operation of an ultra-compact coherent receiver for linear optical phase demodulation. The receiver, based on a broadband optical phase-locked loop (OPLL) has a bandwidth of 1.5 GHz. Physical delay in the feedback path is dramatically reduced by incorporating novel photonic and electronic components. Using the receiver in an analog link experiment, a spurious free dynamic range of 122dBHz$^{2/3}$ is measured at 300 MHz. Additionally, the link loss is -2dB at low frequencies.**

I. INTRODUCTION

Demanding military applications require linear links with very high dynamic range. Most of the work on analog optical links has focused on intensity modulated direct detection (IMDD) links [1]. The highest reported Spurious Free Dynamic Range (SFDR) for a broadband (DC-3GHz) IMDD link is 119.5 dB·Hz$^{2/3}$ [2]. IMDD links have their limitations, not the least of which is that their modulation depth is constrained (between 0 and 100%). Phase modulated links on the other hand, have the advantage of having no inherent limitation to their modulation depth and can be swung over many π. However, the challenge with such links is the phase demodulation process. Recently, two techniques to linearly demodulate optical phase have shown a lot of promise. One involves digitization of the I/Q components of the input optical phase and use of DSP techniques to linearly demodulate phase in the digital domain [3]. The second is based on a high gain OPLL that linearly tracks the input signal phase by applying feedback to a linear optical phase modulator [4, 5].

Our work has focused on the implementation of the later technique at microwave frequencies [6]. The primary challenge in realizing a broadband OPLL is the tradeoff between gain and bandwidth of the feedback loop. In order to ensure high gain while maintaining stability we have developed different integrated versions of our receiver [6,7]. What is novel in this current work is that we flip chip bond the photonic integrated circuit (PIC) to the electronic integrated circuit (EIC) to reduce the physical delay in the feedback path from 35ps to 10ps. The EIC is based on a high-speed, multilevel interconnect 0.6μm emitter InP HBT technology [8]. Also, the PIC incorporates an ultra-compact trench splitter that further reduces the feedback delay. The link performance of the receiver is characterized with a series of experiments.

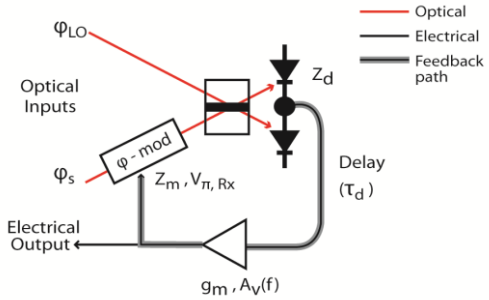

Figure 1. Schematic of receiver architecture

II. SYSTEM ARCHITECTURE

Figure 1 shows a schematic of the receiver architecture. The received optical phase (φ_S) is mixed with an optical reference (φ_{LO}), producing a sinusoidal response to optical phase. The detected differential photocurrent (i_o) is amplified, filtered and fed back to a reference phase modulator whose half wave voltage is denoted as $V_{\pi RX}$. When the loop is closed, the signal and reference optical phase are related as follows:

$$\varphi_S - \varphi_{LO} = \frac{\varphi_S}{1+G} \tag{1}$$

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Where G is the open loop transmission gain. The reduction in the net detected phase results in the demodulator operating within its linear regime. It should be noted that the detector shot noise and the signal phase are reduced by the same feedback gain factor ($1/(1+G)$) and as such the shot noise limited SNR remains unchanged despite the reduction in net phase. More details on the system architecture can be found in [6]. An expression for G can be obtained in terms of the parameters indicated in Figure 1.

$$G = \kappa \left[2 i_0 Z_{\mathrm{d}} Z_{\mathrm{m}} A_v(f) g_m \frac{\pi}{V_{\pi,RX}} e^{2\pi j f \tau_d} \right] \qquad (2)$$

Here Z_D, Z_M are the detector and modulator impedances and g_m is the amplifier transconductance. κ is the coherence penalty. Ideally it should be unity but unequal splitting at the optical beam splitter or polarization mismatches between the reference signal and the input signal could result in a lower κ (and hence, G). One of the key things to note in Equation 2 is the appearance of feedback delay (τ_d) in the exponential term. The delay will add a phase lag at higher frequencies which will result in the feedback loop oscillating if the gain is above unity where the phases crosses over −180°. Thus, delay limits the amount of stable open loop gain that can be realized. Figure 2 plots maximum stable G versus frequency for varying loop delays. Here, an ideal second order feedback loop is assumed [9]. It can be seen that reducing τ_{d} from 35ps to 10ps can result in a 20dB increase in loop gain at 1GHz. Hence, our goal with successive device architectures has been to progressively reduce the latency in the feedback path without compromising the performance of the other elements. Namely, the modulators are sufficiently long (500μm) to ensure low $V_{\pi RX}$ and the detectors are large enough to maintain high linearity at high optical power levels.

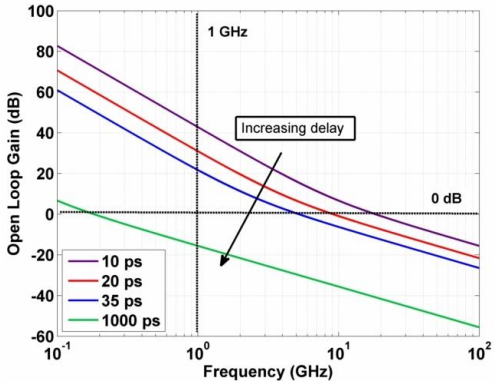

Figure 2. Stable open loop gain (G) versus frequency for an ideal second order feedback loop with varying feedback delay values (τ_{d})

III. INTEGRATED RECEIVER

Previously, we demonstrated an integrated receiver that consisted of two integrated circuits-one photonic (PIC) and the other electronic (EIC) placed adjacent to each other on a common microwave carrier [10]. The PIC consisted of a pair of UTC photodetectors in a balanced configuration [11], tracking phase modulators and a 2x2 Multi-Mode Interference (MMI) beam splitter. The beam splitter was 340μm in length and contributed (along with the PIC-EIC-PIC feedback path) to a total delay of ~35ps. A subsequent version of the PIC incorporated a deeply etched grating and was able to split the incoming optical beams in a region 30 times smaller than a conventional surface ridge MMI based beam splitter [12]. Although this reduced delay through the PIC, the overall loop delay was still limited by the delay from having the EIC placed next to the PIC. In our current version of the receiver we use a flip chip bonding process [13] to integrate the PIC with the EIC. Additionally, the beam splitter is a deeply etched single slot [13]. Together, they bring down the overall loop delay from ~35ps to ~10ps. Figure 3 shows the flip chip bonded integrated receiver mounted on an AlN carrier. The overall dimensions of the receiver are 1.6mm X 0.8mm. Note that in Figure 3 only the rear-side of the PIC is visible as it is flipped and bonded to the EIC.

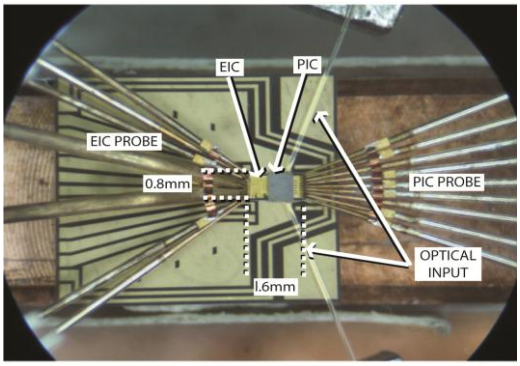

Figure 3. Integrated optoelectronic receiver.

IV. RECEIVER OPERATION

The EIC consists of a differential amplifier pair that is driven on one input with the optical phase detector (common node of balanced detector pair). The other input is grounded. The differential pair current-mode output directly drives balanced phase modulators operated in a push-pull configuration [6]. This doubles the drive voltage to the modulators while reducing the maximum voltage required per modulator to obtain a certain phase swing. We know from Section II that delay in the feedback path reduces the overall phase margin. To compensate for this, a zero is introduced in the transfer function of G via $A_v(f)$. In order for the integrated receiver to function correctly the following need to happen concurrently: 1) The EIC differential pair needs to be balanced, 2) the optical phase demodulator needs to be locked at quadrature and 3) the feedback signal to the PIC modulators has to result in phase tracking of the input signal phase at microwave frequencies. Figure 4 shows the stabilization scheme that is utilized to ensure that all the above three conditions are satisfied. Condition (1) requires that the bias across the modulators be symmetric while (2) requires that the detector common node voltage be forced to 0V by changing the

optical phase of a reference phase modulator (PM2 in Figure 5). Since one side of the differential pair of the EIC is connected to ground it forces the other side (corresponding to the detectors' common node) to 0V to keep the EIC balanced. Any voltage imbalance across the modulators results in the detector common node voltage being non-zero. By sensing the voltage imbalance across the modulators (through two 10kΩ resistors) and generating a correction signal to a phase modulator (PM), the optical phase is adjusted to a condition required to keep the EIC balanced as well as ensure that the interferometer is locked at quadrature.

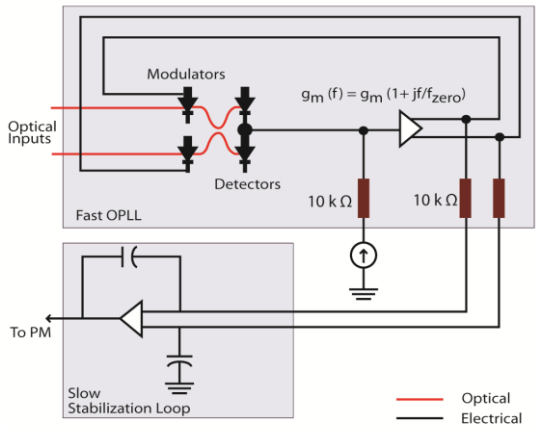

Figure 4. Stablization scheme required for receiver operation

V. LINK DEMONSTRATION

The experimental link is shown in Figure 5. The output of the optical source block is a high-power, amplified laser signal at 1550 nm. A polarizing beam splitter is used to split the input light into the two branches of the interferometer. Two probe tones are applied separately to two $LiNBO_3$ phase modulators, in order to ensure that no mixing products are generated from the two-tone drive signal. PM fiber and components are used for polarization management and stability. Additional details of the experimental setup can be found in [6]. It is important to point out that both the beam splitter and the on-chip tracking modulators, i.e. the semiconductor phase modulators, are sensitive to the polarization of the input light. Hence, we use polarization controllers at the input of the integrated receiver to optimize the splitting ratio in the trench splitter while simultaneously ensuring that the modulators absorb maximally. For the devices used in this experiment, the quantum wells of the semiconductor phase modulators are more efficient (lower V_π) with TE polarized light, which is also absorbed more efficiently than TM polarized light. Further, the trench splitters also have optimal splitting ratio when the input light is TE polarized.

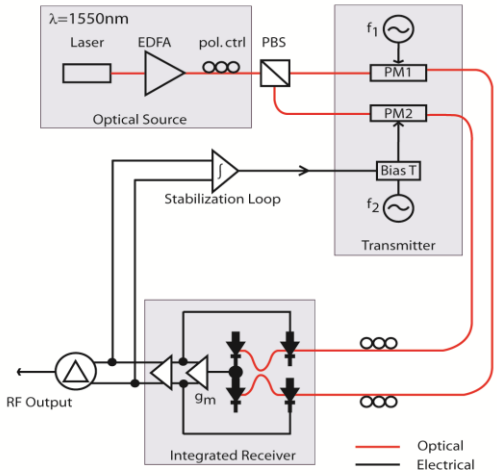

Figure 5. Schematic of experimental setup

A. Link Response

The frequency response of the device for varying values of photocurrent (per detector) is shown in Figure 6. At lower frequencies the combined gain from the photocurrent and electronic g_m block results in a sufficiently high loop transmission gain (G) such that the reference modulator is able to closely track the received signal phase. The optical link gain is now dependent on the ratio of drive voltage between source and reference modulator and in this link is −2dB. At high frequencies, the loop transmission gain is low and hence, the link gain is proportional to the photocurrent and loop filter transfer function as expected. The loop bandwidth, defined here by the 3dB point is 1.5GHz at 3.5mA.

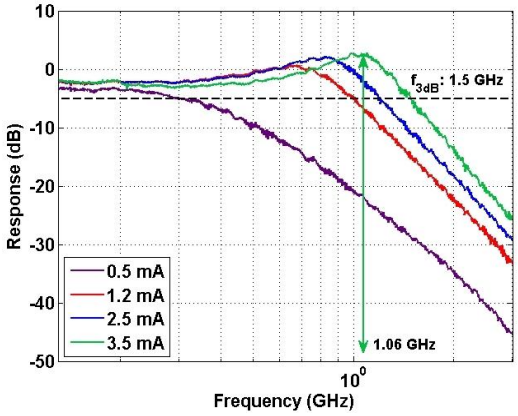

Figure 6. Link gain at different detected photocurrent values

Another interesting feature of the closed loop response is the gain peaking at 1.06GHz. This can be explained by the denominator in the closed-loop gain, $1+G$. Since G is complex, its argument (or phase) can be −180° when $|G| \sim 1$, resulting in unstable operation. From Equation 2 we know that the detector and modulator capacitances provide the necessary integrations in the feedback path resulting in a

second order feedback loop with a −180° feedback phase. To ensure stable operation at unity gain, the transimpedance amplifier contains a lag-compensating network to provide additional phase margin. However, the zero introduced by this element in the open loop transfer function (Equation 2) has been designed for delay-limited feedback gain and therefore does not provide optimum lag-compensation around 1 GHz. Also, any stray capacitances in the feedback path could degrade the phase margin, resulting in unstable operation at higher gain values. Several variants of the EIC with different g_m and f_o values have been designed and currently we are investigating pairing the appropriate EIC variant with the appropriate PIC in order to obtain the highest loop gain while still maintaining stability.

B. *Spurious Free Dynamic Range (SFDR)*

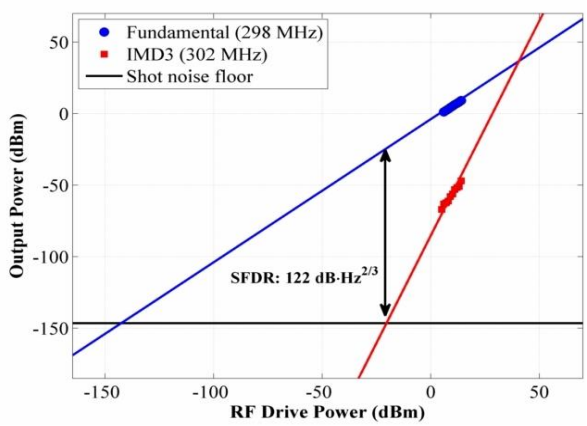

Figure 7. SFDR at 300MHz with 2.8mA of photocurrent per detector

Figure 7 shows SFDR data taken at 300 MHz. The photocurrent per detector was roughly 2.8mA. This is ~4x lower than what was reported in [10] for a similar SFDR value. However, from Section II, we know that the open loop gain (G) is proportional to both the photocurrent (i_0) as well as the gain of the electronic amplification block (g_m). Here, we use a high gain g_m block to compensate for the lower photocurrent. The high gain in the feedback loop results in linear phase tracking especially at lower frequencies and consequently, an SFDR of 122dB·Hz$^{2/3}$ was measured. The noise floor shown in the plot in Figure 7 is not the measured noise floor but rather it is the shot noise of the receiver referred back to the input (i.e. the transmitter). Based on V_π=4.4V for the transmitter modulator the shot noise floor is calculated to be −146.5dBm/Hz. The principal benefit of this type of receiver, which uses feedback to suppress nonlinearities in the phase demodulation process, is realized when the optical modulation index of the transmitted signal is very large. From Figure 7 it can be seen that the maximum input RF drive power to the $LiNbO_3$ modulators is 15dBm per tone. This corresponds to φ_{rms} =0.3π which in turn means that $\varphi_{peak\text{-}peak}$ is ~0.81 π rad. This is for a single tone and hence, for two tones the peak to peak phase swing ($\varphi_{peak\text{-}peak}$) is ~1.62 π . Having such a large modulation index without feedback would cause the output of a traditional interferometer-based phase demodulator to be severely distorted. However, in the case of our feedback receiver the third order intermodulation (IMD3) terms remain suppressed at −56dBc.

VI. CONCLUSION

In this paper we have experimentally demonstrated the baseband operation of an ultra-compact coherent integrated receiver that tightly integrates a photonic IC and an electronic IC via a flip chip bonding process that dramatically reduces delay in the feedback path. A loop bandwidth of 1.5 GHz and SFDR of 122dB.Hz$^{2/3}$ at 300MHz is reported. Additionally, we report an extremely low link loss: −2dB at low frequencies, when the loop is closed and the reference phase modulator is closely tracking the input signal phase. Current efforts are focused on improving the linearity performance of the receiver by trying to increase the photocurrent in the detectors so as to get higher open loop gain (G).

ACKNOWLEDGMENT

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