100+ GHz Transistor Electronics; Present and Projected Capabililties

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***Abstract*—Design principle and the present status of high-frequency transistors and integrated circuits are reviewed. Given presently-demonstrated process and material parameters, bipolar transistors having ~3 THz power-gain cutoff frequencies are feasible. Demonstration of field-effect transistors having similar bandwidth requires development of high-capacitance-density gate dielectrics of adequately low leakage current, and high-K oxide gate barriers may therefore be necessary. Transistors of such bandwidths would enable e.g. ~1.5 THz radio transmitters and receivers; classical electron device and circuit techniques are feasible over most of the sub-millimeter-wave (0.3-3 THz) spectrum.**

I will review both recent results and underlying design principles in the development of high frequency transistors and integrated circuits.

In the design of high-frequency bipolar transistors [1], a 2:1 increase in bandwidth is obtained by thinning the collector depletion region 2:1, reducing the base thickness ~1.41:1, reducing the widths (the lithographic feature sizes) of the emitter-base and base-collector junctions 4:1, reducing the resistivities (resistances per unit area) of the metal-semiconductor interfaces 4:1, and increasing by 4:1 the device operating current density. At the 256 nm scaling generation, InP-based HBTs exhibit ~400 GHz current-gain and >800 GHz power-gain cutoff frequencies [2]. *Published* circuit results at this scaling generation include 340 GHz amplifiers [3] and oscillators [4] and 205 GHz master-slave latches (static frequency dividers) [5]. Results at higher frequencies will soon be reported at this and smaller HBT scaling generations.

The 128 nm and 64 nm HBT scaling generations are in development. With the 64 nm scaling generation, 1 THz current-gain and 2 THz power-gain cutoff frequencies are targeted; the primary challenges faced in developing such transistors are the requirements for very low metal-semiconductor contact resistivities (1-2 $\Omega-\mu m^2$), contact and metal conductor stability very high (~40 $mA/\mu m^2$) current densities, and the general challenges of high-yield fabrication at 64 nm feature size. HBT bandwidth at the 64 nm feature size should be sufficient to enable 1.0 THz radio transmitters and receivers and medium scale digital ICs (i.e. optical transceivers) operating at 500 GHz digital clock rate.

In the design of high-frequency III-V field effect transistors [7], a 2:1 increase in bandwidth is obtained by reducing the gate length 2:1, reducing the access resistance per unit gate width of the source and drain regions by 2:1, increasing the drain current and transconductance per unit gate width by 2:1, and increasing the capacitance per unit area between the gate electrode and the 2-dimensional electron gas by 2:1. Increasing the gate-channel capacitance density requires decreased thickness or increased permittivity of the gate dielectric, decreased thickness of the quantum well or inversion layer carrying the current, and increased two-dimensional density of carrier states within the channel. III-V HEMTs are FETs using a wide-gap semiconductor as the gate barrier; HEMTs at 35 nm gate length have shown [7] somewhat greater than 1 THz power-gain cutoff frequencies. Using these FETs, amplifiers have been demonstrated at 480 GHz [7]. As with HBTs, increased III-V FET bandwidth can be expected with further scaling. From simple geometric scaling theory [6], 1.6 THz current-gain and 2.0 THz power-gain cutoff frequencies should be obtainable at 13 nm gate length in FETs using III-V semiconductor channels, but the source and drain access resistivities must be reduced 2:1 below the ~100 $\Omega-\mu m$ presently achieved, and the SiO_2-equivalent gate dielectric thickness reduced to approximately 0.3 nm. Achieving these underlying device performance parameters may require significant changes to the basic FET design, with the possible introduction of semiconductor regrowth of the source-drain regions for reduction of access resistivities and high-K oxide gate dielectrics for the gate barrier.

Comparing these results to Silicon VLSI, 150 GHz amplifiers at 2 dB/stage gain have been demonstrated in 65nm bulk CMOS processes [8]. Difficulties in scaling the gate oxide equivalent thickness have made MOSFET power-gain cutoff frequencies increase much more slowly than simple geometric scaling theory would predict, and it is at present unclear whether useful amplifiers much above 200 GHz can be realized in the 45 nm or 32 nm scaling generations.

Bandwidths of transistors, whether III-V or Silicon, are increased by reducing epitaxial layer thicknesses, reducing lithographic dimensions, and increasing current densities. Critical are improved surface properties, with dielectric-semiconductor interfaces of low interfacial trap density and high capacitance density of central importance to FET scaling, and with metal-semiconductor interfaces of low resistivity and reliability under high operating current density being of central importance to both bipolar and field-effect transistors. Scaling of III-V HBTs through at least the 32 nm (2.8 THz)

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generation appears feasible. Attaining similar power-gain cutoff frequencies with III-V FETs at the 9 nm scaling generation depends critically upon the success in development of high-K gate dielectrics for these materials. As with VLSI, power per unit IC die area scales as the square of circuit bandwidth, and greatly improved techniques must be developed for removing heat.

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