Submitted

on October 29, 09:18 AM

for mrsspring2010

Proof

CONTROL ID: 756345

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Abstract Details

PRESENTATION TYPE: Invited Speaker

SYMPOSIUM: I: Materials for End-of-Roadmap Scaling of CMOS Devices

KEYWORDS: Composition & Microstructure / Material Type / III-V, Performance / Functionality / devices, Properties / Transport / electrical properties.

Abstract

TITLE: Scaling FETs to 10 nm: Coulomb Effects, Source Starvation, and Virtual Source.

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ABSTRACT BODY: Summary. In our attempts to scale FETs to the 10 nm length, alternatives to conventional Si CMOS are sought on the grounds that: **1.** Si seems to have reached its technological and performance limits and **2.** the use of alternative high-mobility channel materials will provide the missing performance. With the help of numerical simulations here we establish the reasons why indeed Si seems to have hit a performance barrier and whether high-mobility semiconductors can indeed grant us our wishes. The role of long- and short-range electron-electron interactions will be revisited together with a recent analysis of the historical performance trends. The density-of-states (DOS) bottleneck and source starvation issues will also be reviewed to see what advantage alternative substrates may bring us. Finally, the well-known `virtual source model' will be analyzed to assess whether it can be used as a quantitative tool to guide us to the 10 nm gate length.

Coulomb Interactions and Historical Trends of Si nMOS Performance. Khakifirooz and Antoniadis have analyzed the historical performance trends of Si MOSFETs and found that their performance (measured by the `injection velocity' at the virtual source) saturates and even decreases for gate lengths smaller than about 30-to-40 nm. We will argue that this trend finds its origin in an intrinsic process: Monte Carlo calculations -- performed accounting for long-range and short-range Coulomb interactions among electrons -- have provided a remarkably similar trend and hint strongly at the intrinsic nature of the problem. The use of metal gates can mitigate the effect to some extent, but the channel-S/D interaction is intrinsic and unavoidable, barring the use of Schottky S/D contacts.

High-mobility Channel Materials. The use of high-mobility semiconductors also presents intrinsic difficulties: The DOS bottleneck -- *i.e.*, the reduced inversion capacitance due to their small effective mass -- overcomes the advantage of the higher velocity. Source starvation -- *i.e.*, the inability of the source region to provide the amount of carriers required to maintain a high current across the channel -- makes it necessary to modify significantly our device design. We shall discuss how our simulated InGaAs-channel devices had to be optimized by using thicker channels, higher-doping and raised S/D regions to counter these effects.

**Revisiting the `Virtual Source Model'.** Coulomb effects, DOS bottleneck, and source starvation (with the associated off-equilibrium effects near the source) force us to revisit the virtual-source model. It will be argued that while providing a useful qualitative guideline to understand the `essential physics' of MOSFETs, its quantitative predictions cannot be trusted when considering gate length at the sub-50 nm scale.

(No Table Selected)

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