A Self-Aligned Epitaxial Regrowth Process for Sub-100-nm III-V FETs

M. J.W. Rodwell[a], A. D. Carter, G. J. Burek[a], M. A. Wistey[a,b], B. J. Thibeault[a], A. Baraskar[a], U. Singisetti[a], Byungha Shin[c], E. Kim[c], J. Cagnon[b], Y.-J. Lee[d], S. Stemmer[a], P. C. McIntyre[c], A. C. Gossard[a], C. Palmstrøm[a], D. Wang[e], B. Yu[e], P. Asbeck[e], Y. Taur[e]

[a]U.C. Santa Barbara, [b]Univ. of Notre Dame, [c]Stanford University, [d]Intel, [e]U.C. San Diego.

Because of the low electron effective mass and the high resulting carrier velocities, MOSFETs with InGaAs channels are being investigated for potential application in VLSI circuits at scaling generations beyond 22 nm. In addition to formidable challenges faced in developing gate dielectrics with the necessary low interface state density, transistors must be built with ~ 20 nm gate lengths, ~5 nm channel thicknesses, and source and drain contacts of ~20 nm width separated by no more than 10-20 nm from the gate edges. In the ballistic transport limit, a FET with ~0.6 nm EOT gate dielectric would show ~5 mS/micrometer transconductance and 1.5 mA/micrometer drain current at 300 mV gate overdrive; hence even 20 Ohm-micron source and drain access resistivities would reduce the drive current by 10%. Given contacts 20 nm wide, source and drain contact resistivities should thus be below 0.4 Ohm-micron^2. At 300 mV gate overdrive, the inversion charge density is ~2.5E12/cm^2, hence the source electron density should exceed 5E12/cm^2 to avoid source starvation; this corresponds to 1E19/cm^3 in a 5 nm thick channel. The source and drain regions must be very heavily doped, yet the extrinsic source and drain junctions must be at most a few nm deep in order to obtain steep subthreshold slope and low drain-induced barrier lowering. To meet these electrical and structural requirements, the transistor design and process flow must differ markedly from that of III-V transistors now used in microwave amplification. Nor can silicon MOS processes be used, given that III-V materials have characteristics different from silicon and can tolerate only much lower process temperatures.

Addressing these requirements, we have developed a process for fabrication of self-aligned III-V MOSFETs. The process has self-aligned in-situ source/drain Ohmic contacts and self-aligned N+ source/drain n+ regions formed by epitaxial regrowth. The epitaxial dimensions are small, as is required for 22 nm gate length MOSFETs; with a 5 nm thick channel confined below by a heterojunction, and the n++ source/drain junctions do not extend below the 5 nm channel.

In this gate-first process, thin 5 nm InGaAs channels are grown by MBE and alumina gate dielectric deposited by ALD. The gate electrode is a sputter-deposited refractory metal patterned by reactive-ion etching, and device electrodes are separated by dielectric sidewalls. Self-aligned InAs source/drain N+ regions are defined by epitaxial (migration enhanced epitaxy, MEE) regrowth. These are doped at 4E19/cm^3, are 60 nm thick, and show 18 Ohm sheet resistivity. Source/drain contacts self-aligned to the gate are formed by in-situ blanket molybdenum deposition and a patterned by height-selective etching. Mesa isolation and pad contact complete the process. A device with 200 nm gate length showed 0.95 mA/micrometer current density at Vgs=4.0 V, and 0.45 mS/micrometer peak transconductance.