2010 Materials Research Society Spring Meeting, April 7, San Francisco

A Self-Aligned Epitaxial Regrowth Process for Sub-100-nm III-V FETs

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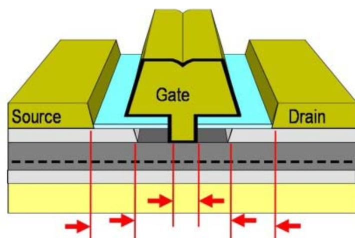
III-V MOS: What is needed ?

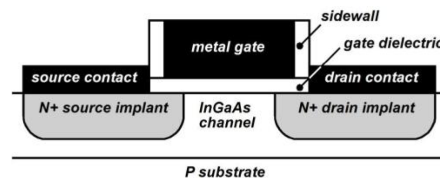
True MOS device structures at ~10 nm gate lengths

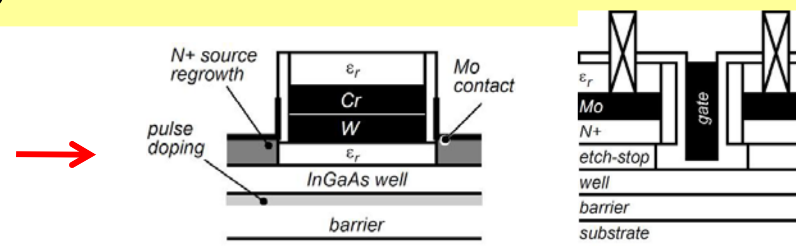
10nm gate length, < 10nm electrode spacings, < 10nm contact widths

< 3 nm channel, < 1 nm gate-channel separation, < 3nm deep junctions

Fully self-aligned processes: N+ S/D, S/D contacts







Drive currents >> 1 mA/micron @ 1/2-Volt V_{dd}.

Low access resistances.

Density-of-states limits.

Dielectrics: < 0.6 nm EOT , D_{it} < 10^{12} /cm^2-eV

impacts I_{on}, I_{off} , ...

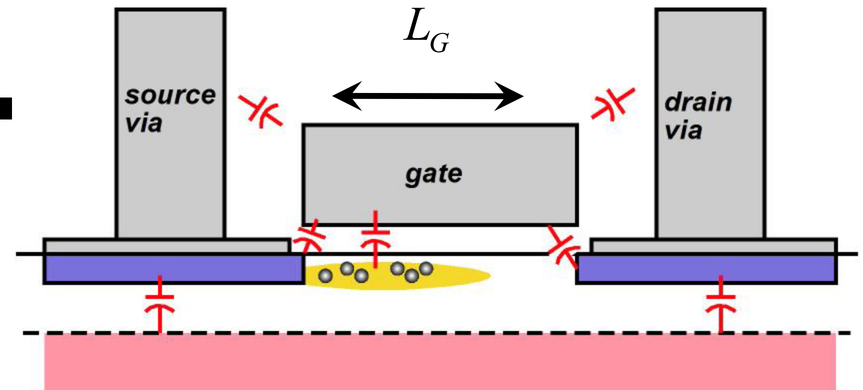
Low dielectric D_{it} must survive FET process.

...and the channel must be grown on Silicon

FETs

FET Scaling Laws

Changes required to double device / circuit bandwidth.



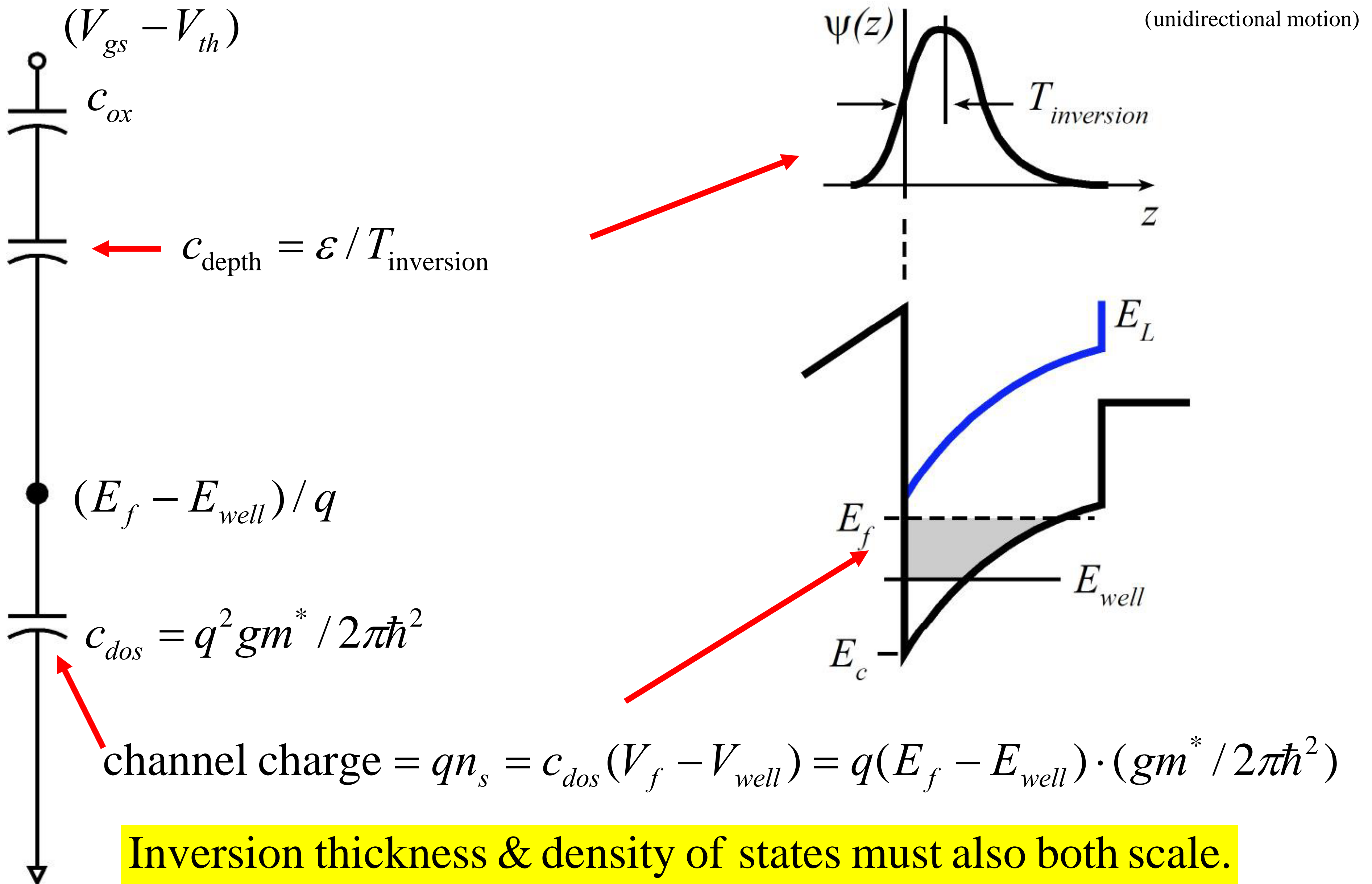
(gate width W_G)

laws in constant-voltage limit:

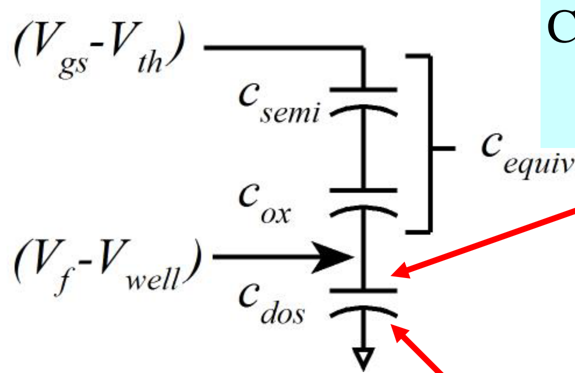
FET parameter	change
gate length	decrease 2:1
current density (mA/μm), g_m (mS/μm)	increase 2:1
channel 2DEG electron density	increase 2:1
electron mass in transport direction	constant
gate-channel capacitance density	increase 2:1
dielectric equivalent thickness	decrease 2:1
channel thickness	decrease 2:1
channel density of states	increase 2:1
source & drain contact resistivities	decrease 4:1

Current densities should double
Charge densities must double

Semiconductor Capacitances Must Also Scale

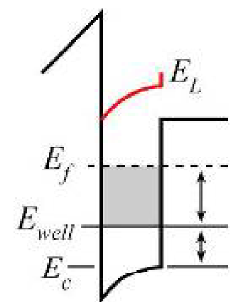


Calculating Current: Ballistic Limit



Channel Fermi voltage = voltage applied to c_{dos}

determines Fermi velocity v_f through $E_f = qV_f = m^* v_f^2 / 2$



mean electron velocity = $\bar{v} = (4/3\pi)v_f$

Channel charge : $\rho_s = c_{dos}\left(V_f - V_c\right) = \frac{c_{dos}c_{equiv}}{c_{equiv} + c_{dos}}\left(V_{gs} - V_{th}\right)$

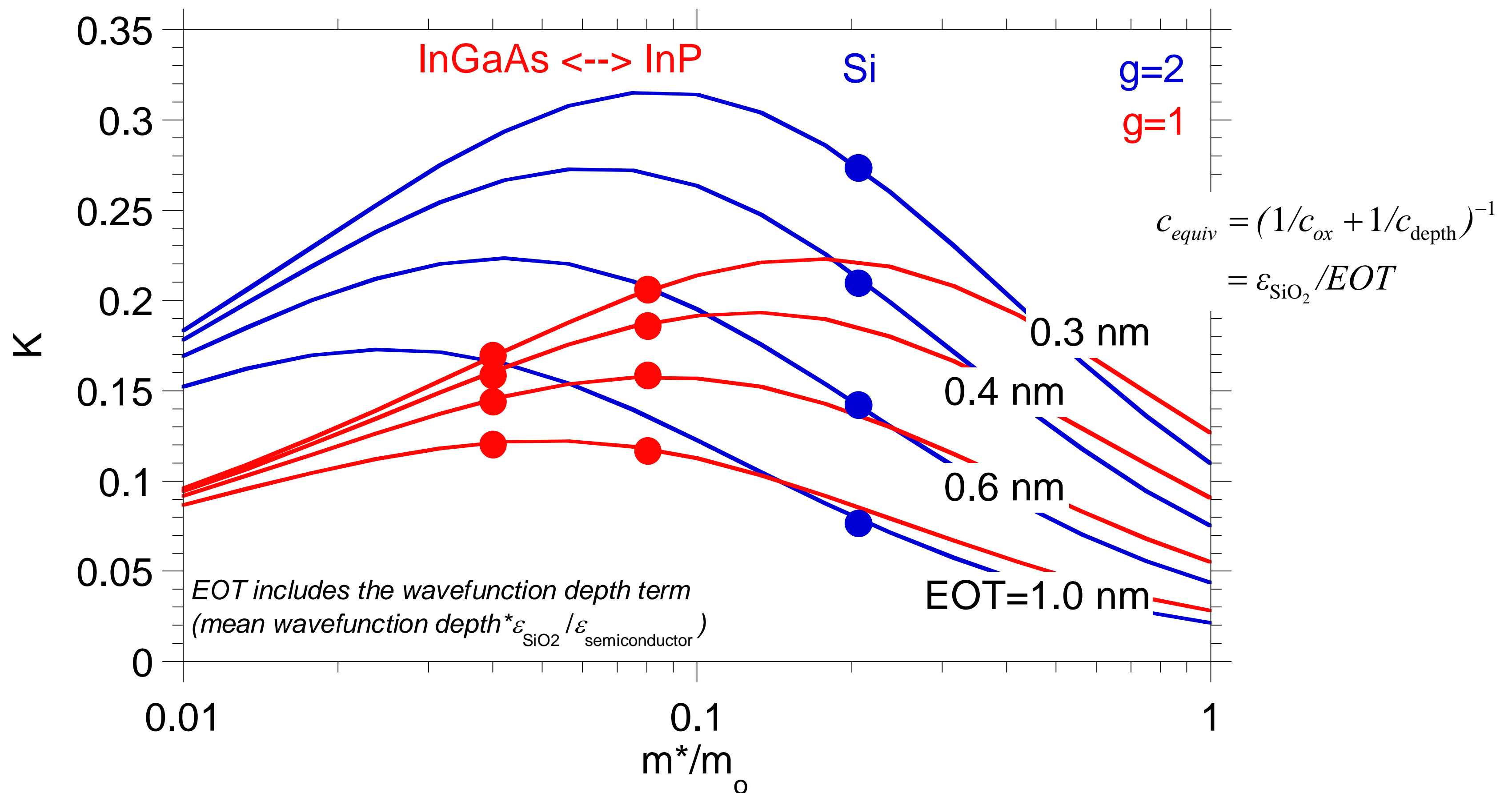
$c_{dos} = q^2 g m^* / 2\pi\hbar^2 = c_{dos,o} \cdot g \cdot (m^*/m_o)$, where g is the # of band minima

$$\Rightarrow \quad J = \left(84\,\frac{\text{mA}}{\mu\text{m}}\right)\frac{g \cdot (m^*/m_o)^{1/2}}{\left(1 + (c_{dos,o}/c_{ox}) \cdot g \cdot (m^*/m_o)\right)^{3/2}}\left(\frac{V_{gs} - V_{th}}{1\,\text{V}}\right)^{3/2}$$

Do we get highest current with high or low mass ?

Drive Current Versus Mass, # Valleys, and EOT

$$J = \underline{K} \cdot \left(84\frac{\text{mA}}{\mu\text{m}}\right) \cdot \left(\frac{V_{gs} - V_{th}}{1\text{ V}}\right)^{3/2}, \quad \text{where } \underline{K} = \frac{g \cdot (m^*/m_o)^{1/2}}{\left(1 + (c_{dos,o}/c_{equiv}) \cdot g \cdot (m^*/m_o)\right)^{3/2}}$$

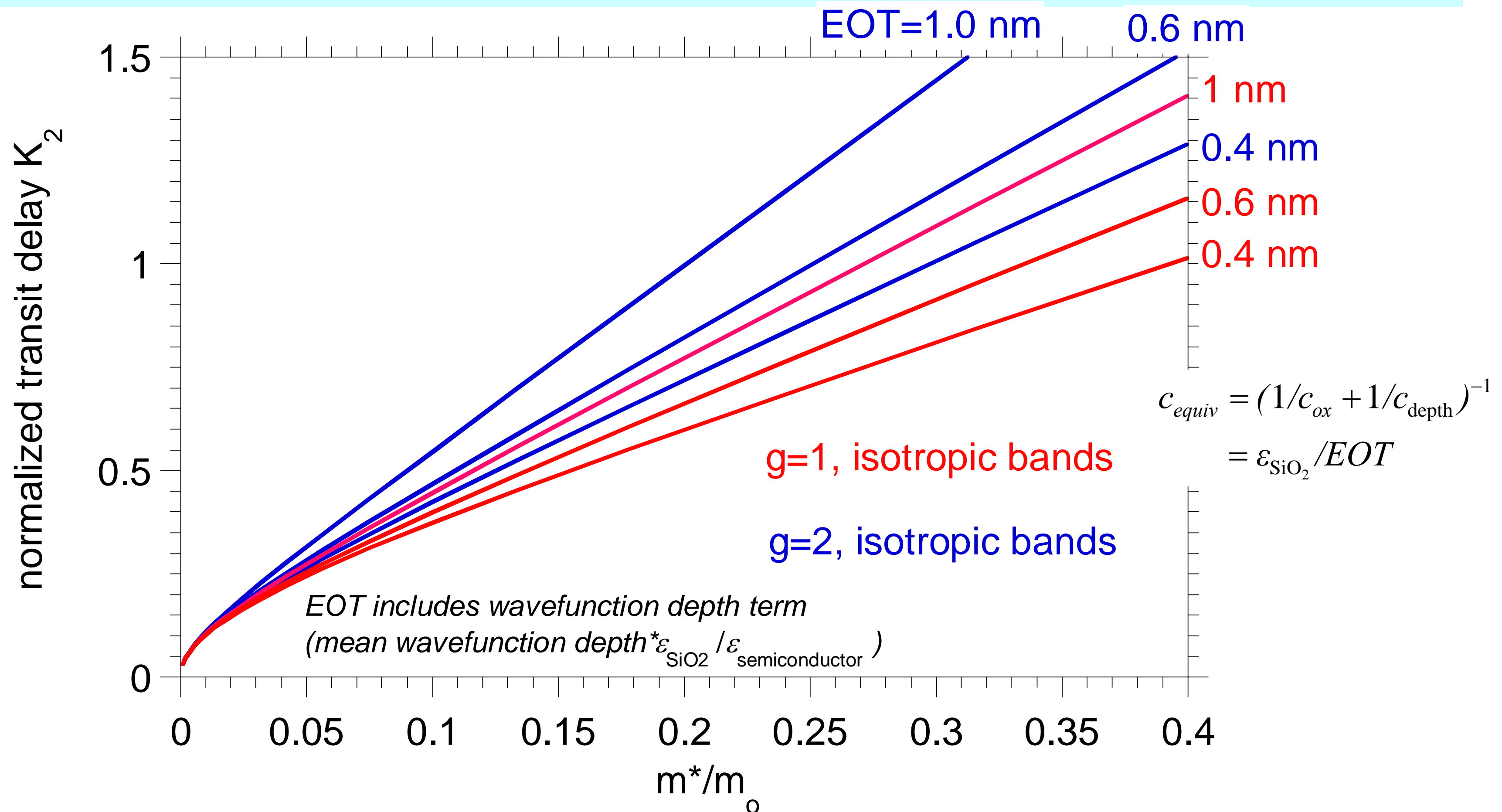


Standard InGaAs MOSFETs have superior I_d to Si at large EOT.

Standard InGaAs MOSFETs have inferior I_d to Si at small EOT.

Transit Delay versus Effective Mass

$$\tau_{ch} = K_2 \cdot \left(\frac{L_g}{2.52 \cdot 10^7 \text{ cm/s}} \right) \cdot \left(\frac{1 \text{ Volt}}{V_{gs} - V_{th}} \right)^{1/2} \quad \text{where } K_2 = \left(\frac{m^*}{m_0} \right)^{1/2} \cdot \left(1 + \frac{c_{dos,o}}{c_{eq}} \cdot g \cdot \frac{m^*}{m_o} \right)^{1/2}$$



Low m* gives lowest transit time, lowest C_{gs} at <u>any</u> EOT.

III-V MOSFETs for VLSI: Why and Why Not.

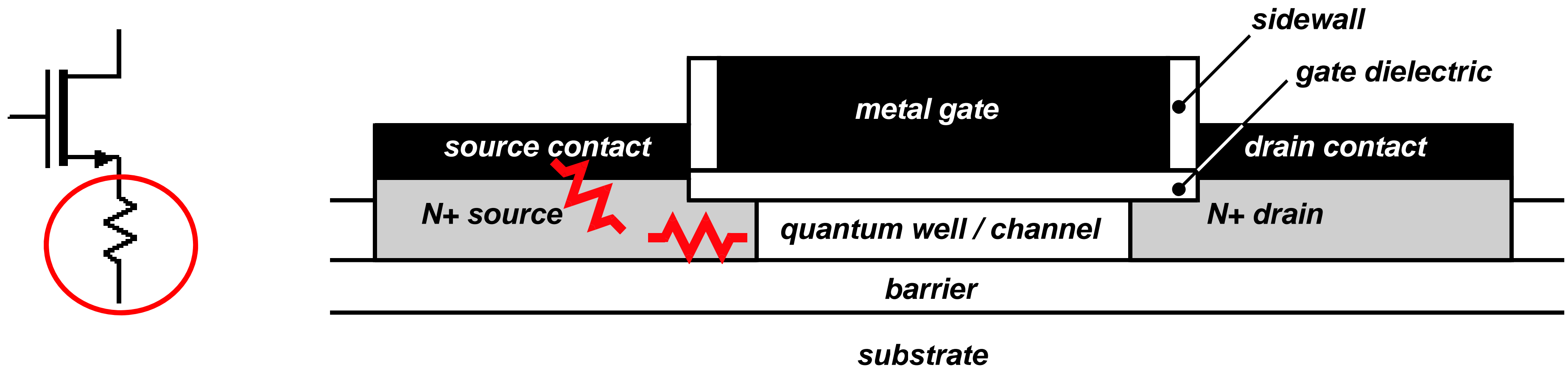
Lower mass → Higher Carrier Velocity→ lower input capacitance
improved gate delay in transistor-capacitance-limited gates
not relevant in wiring-capacitance-limited gates (i.e. most of VLSI)

More importantly: potential for higher drive current
improved gate delay in wiring-capacitance-limited gates (VLSI)

But this advantage is widely misunderstood in community
InGaAs channels→ higher I_d / W_g than Si only for thick dielectrics
....LOWER I_d / W_g than Si for thin dielectrics
break-even point is at ~0.5 nm EOT

We will introduce (DRC2010) candidate III-V channel designs
providing higher I_d / W_g than Si even for small EOT

Contacts: Low Resistivity, High Current Density



For < 10% impact on drive current,

$$I_D R_S /(V_{DD} - V_{th}) < 0.1$$

Target $I_D / W_g \sim 1.5 \text{ mA}/\mu\text{m} \ @ \ (V_{DD} - V_{th}) = 0.3 \text{ V}$

$$\rightarrow R_s W_g < 20\,\Omega - \mu\text{m}$$

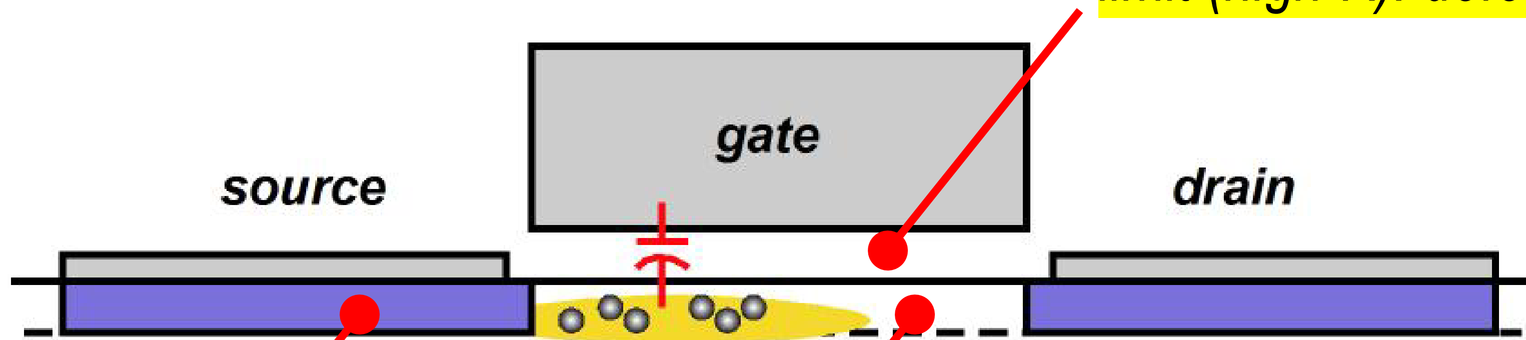
10 nm wide contact $\rightarrow \rho_c < 0.2\,\Omega - \mu\text{m}^2$ (!)

current density in contact $= 150 \text{ mA}/\mu\text{m}^2$ → refractory contacts

FET: Key Regions, Key Challenges

For each 2:1 reduction in gate length:

***gate dielectric**:*
2:1 reduction in thickness
limit: tunneling→high-K
limit (high-K): defects



***contacts**:*
4:1 reduction in contact resistivity
2:1 shallower
4:1 higher J

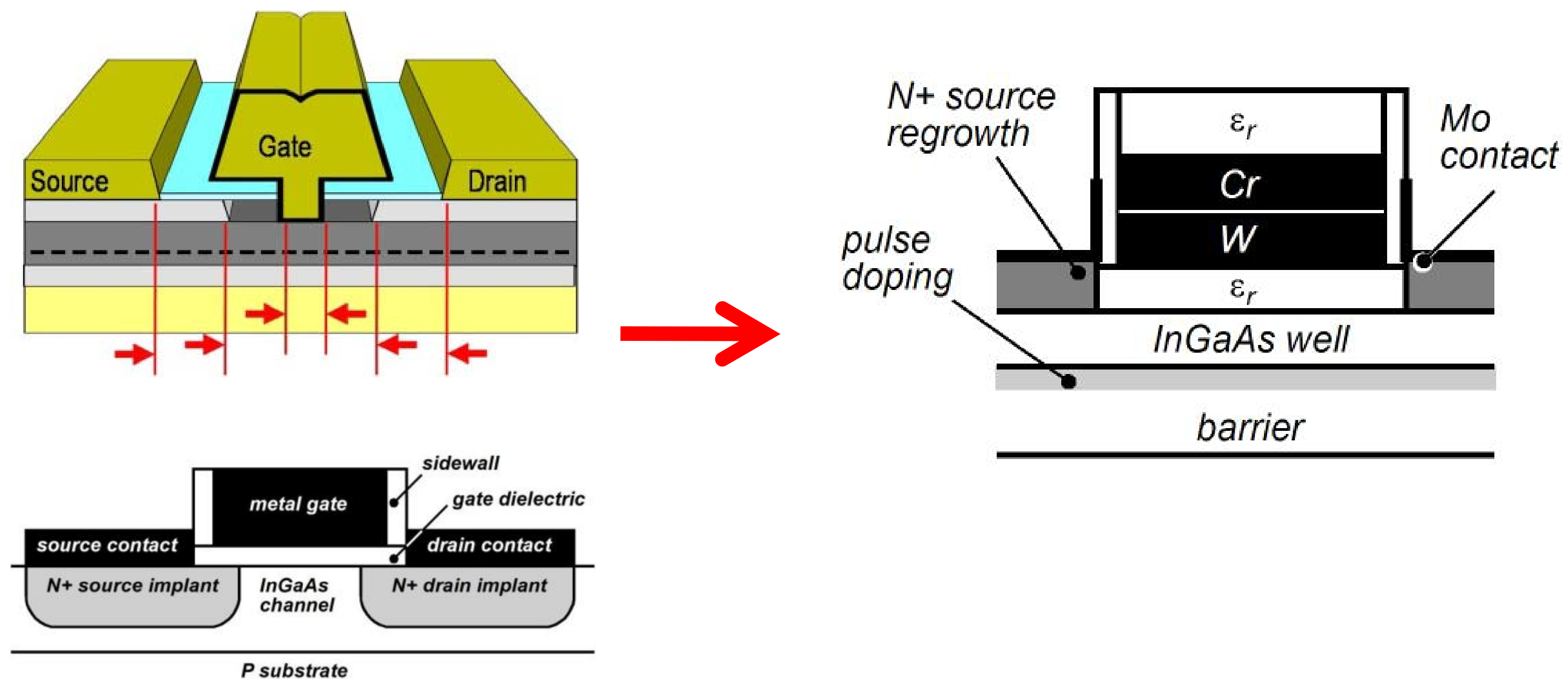
***channel** :*
2:1 increase in electron density @ same voltage
limit: # available electron states / area / energy
"density of states bottleneck"; perceived to be fundamental

Highly Scaled FET Process Flows

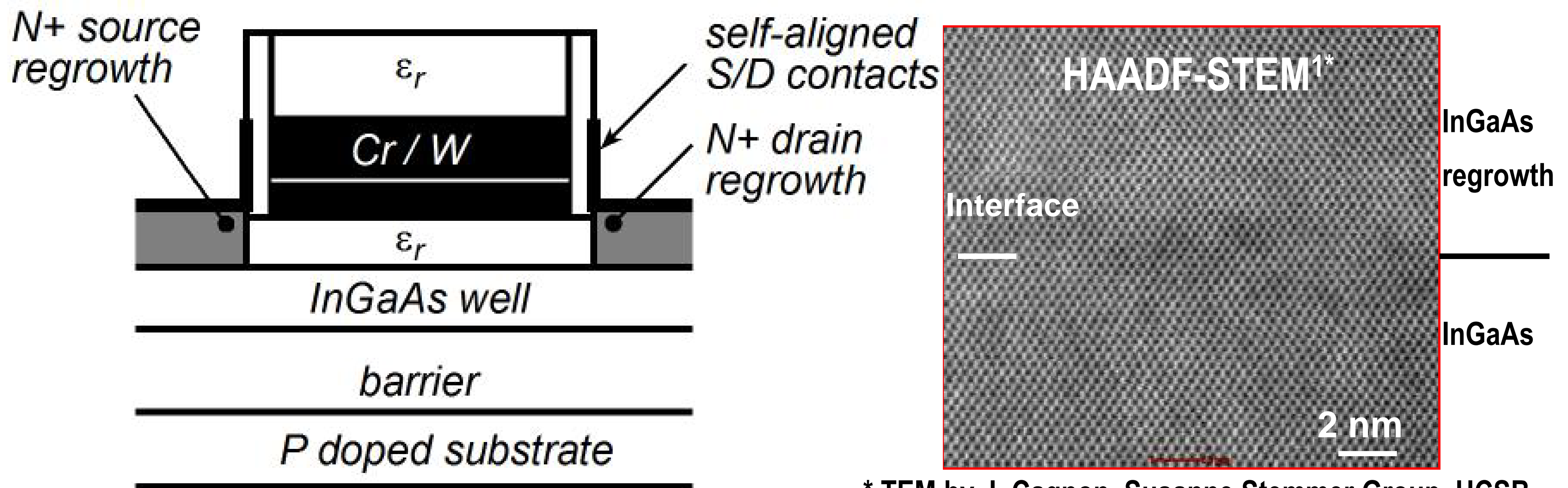
Scalable nm III-V MOSFET: what is needed

True <u>MOS</u> device structures at ~10 nm gate lengths

10 nm gate length, < 10nm electrode spacings, < 10nm contact widths
< 3 nm channel, < 1 nm gate-channel separation, < w nm deep junctions
Fully self-aligned processes: N+ S/D, S/D contacts



InGaAs MOSFET with N+ Source/Drain by MEE Regrowth[1]



Self-aligned source/drain defined by MBE regrowth[2]

Self-aligned in-situ Mo contacts[3]

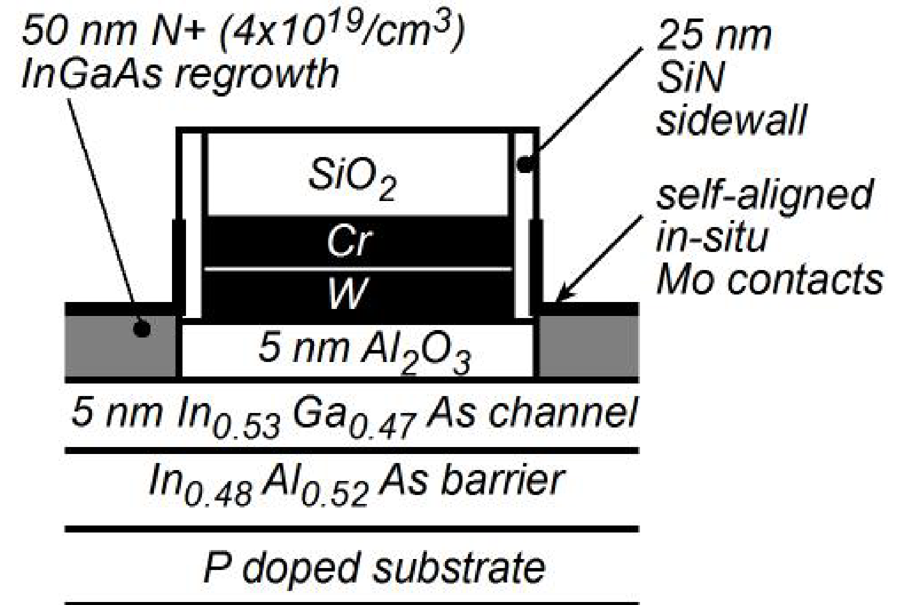
Process flow & dimensions selected for 10-30 nm L_g design;

[1]Singisetti, ISCS 2008

[2]Wistey, EMC 2008

[3]Baraskar, EMC 2009

Regrown S/D process: key features



Self-aligned <u>& low resistivity</u>

...source / drain N+ regions

...source / drain metal contacts

Vertical S/D doping profile set by MBE

no n+ junction extension below channel

abrupt on few-nm scale

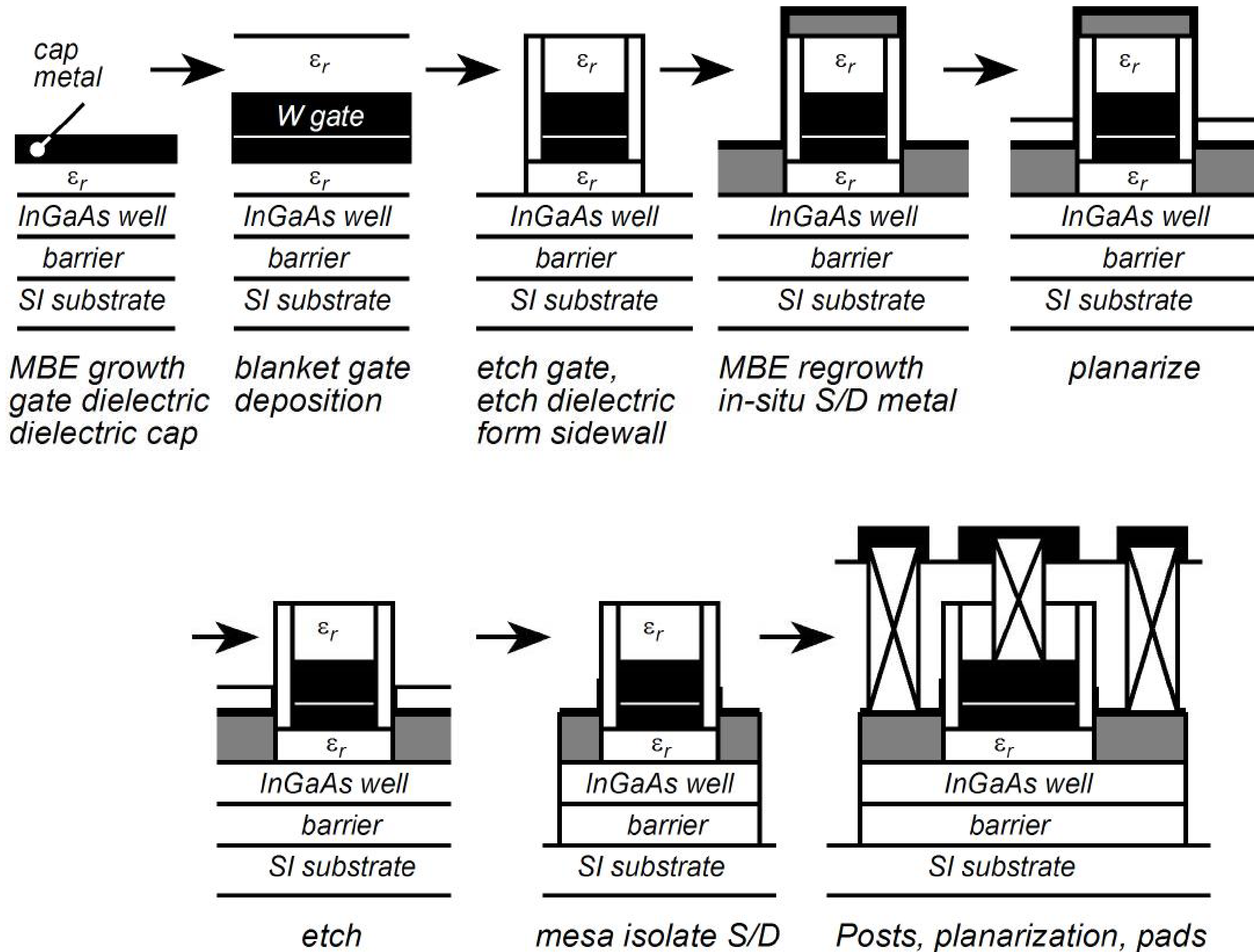
Gate-first

gate dielectric formed after MBE growth

uncontaminated / undamaged surface

Process flow*

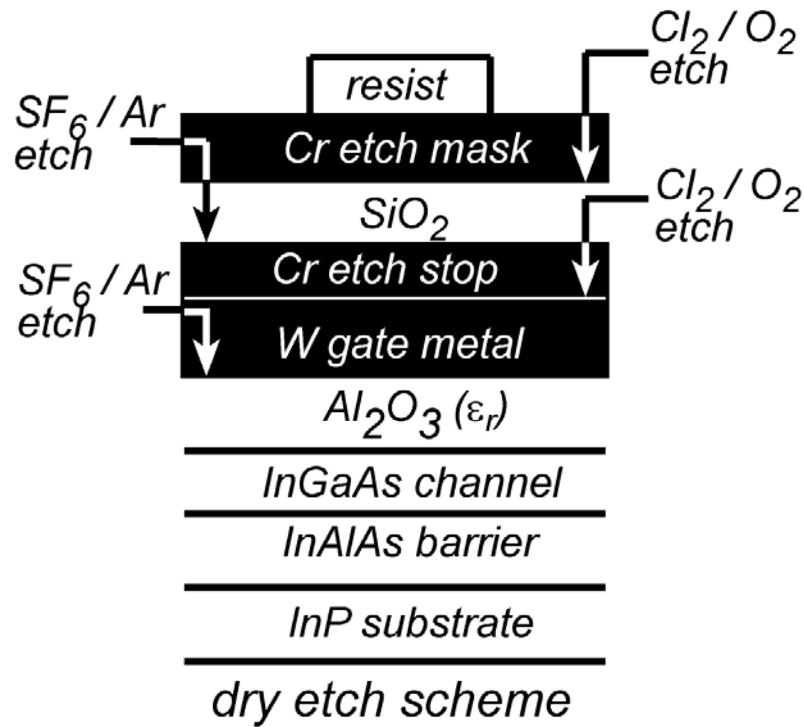
* Singisetti et al, 2008 ISCS, September, Frieburg
Singisetti *et al*; Physica Status Solidi C, vol. 6, pp. 1394,2009

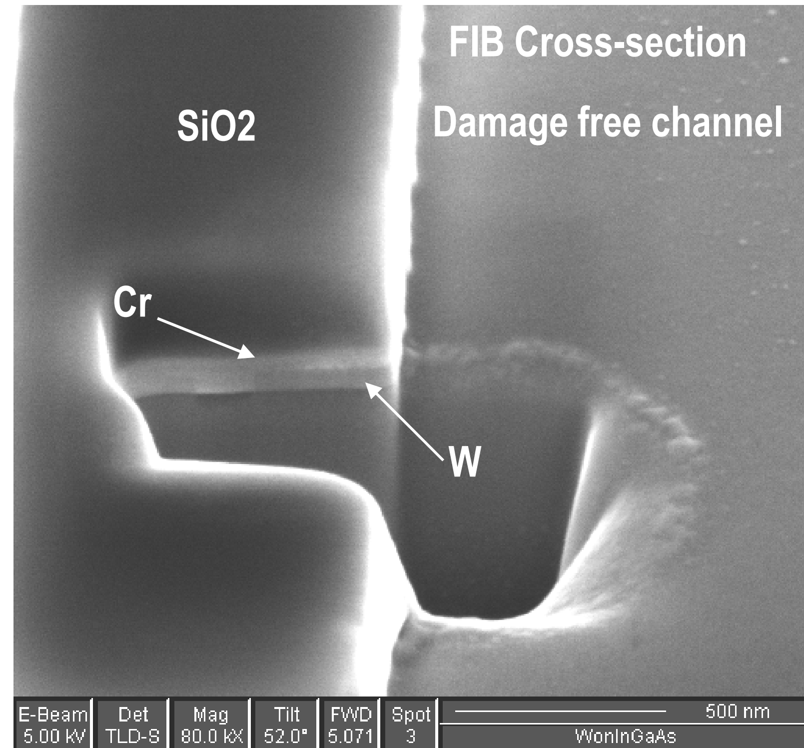


Key challenge in S/D process: gate stack etch

Requirement: avoid damaging semiconductor surface:

*Approach: Gate stack with multiple selective etches**

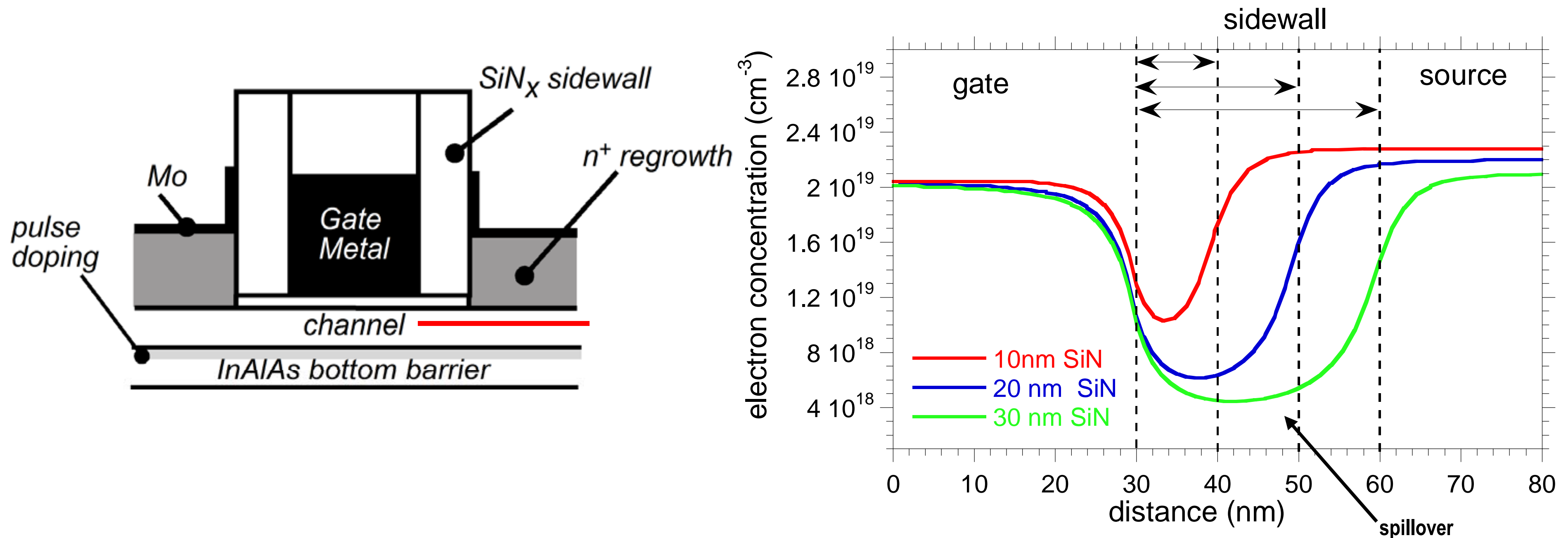




Process scalable to ~10 nm gate lengths

*** Singisetti *et al*; Physica Status Solidi C, vol. 6, pp. 1394,2009**

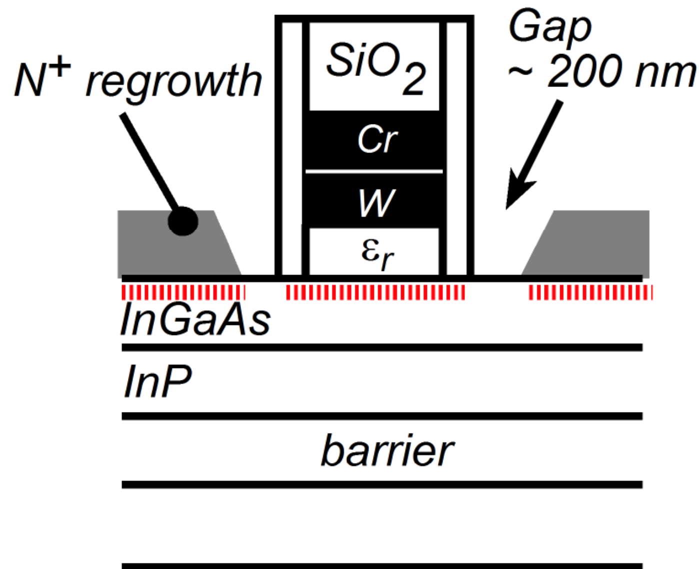
Challenge in S/D process: dielectric sidewall

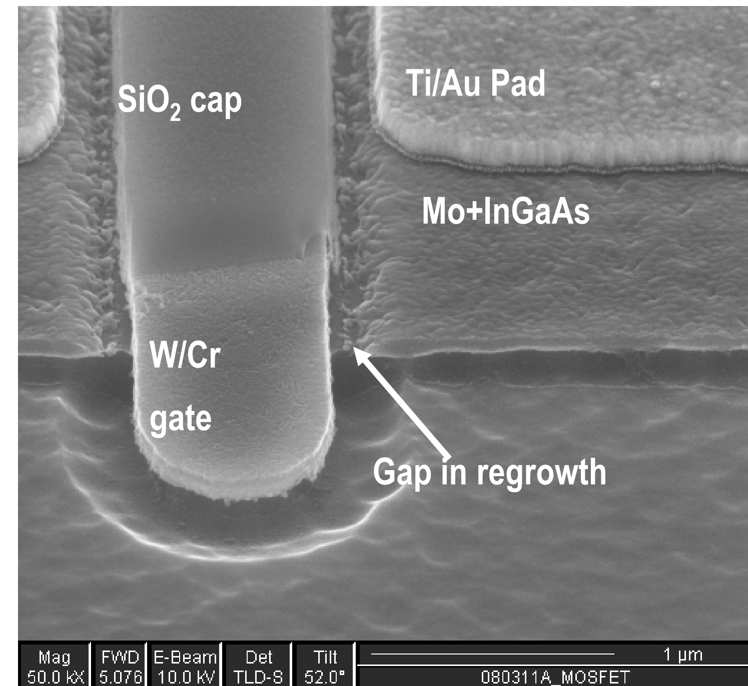


n_s under sidewall:
electrostatic spillover from source, gate

Sidewall must be kept thin:
avoid carrier depletion,
avoid source starvation

MBE Regrowth→ Gap Near Gate→ Source Resistance





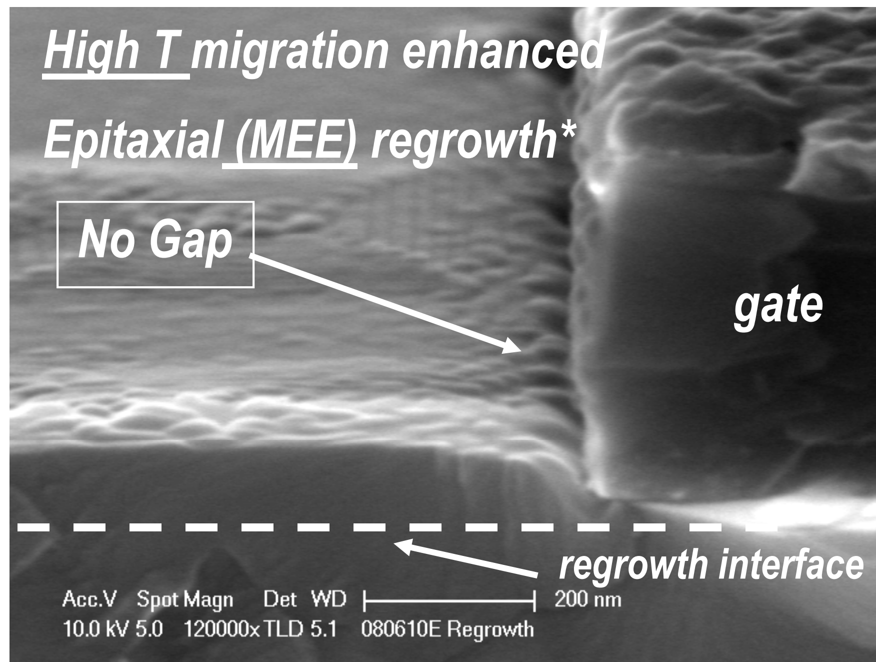
- ***Shadowing by gate: No regrowth next to gate***

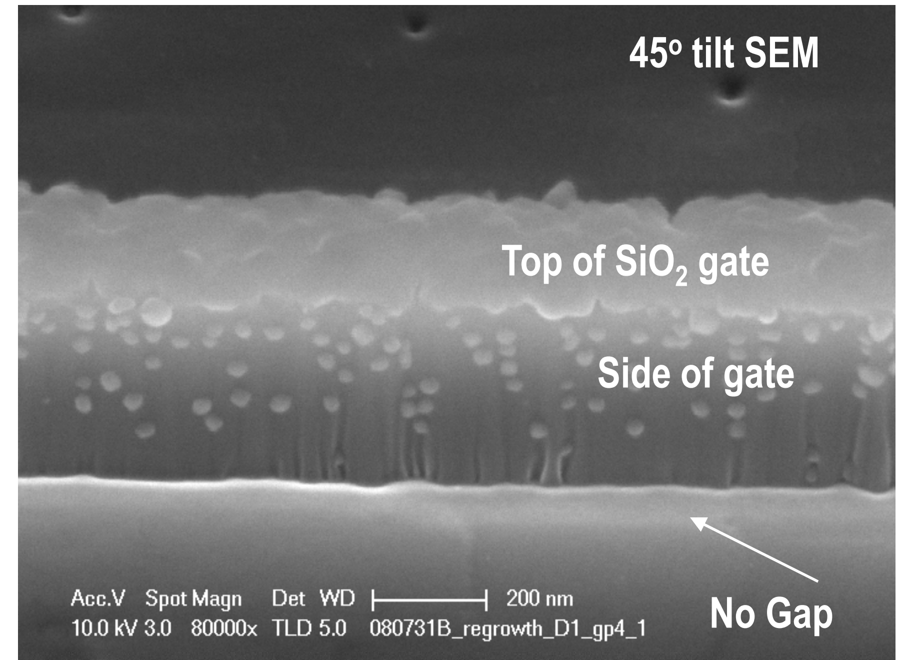
- ***Gap region is depleted of electrons***

High source resistance because of electron depletion in the gap

MBE growth by Dr. Mark Wistey, device fabrication and characterization by U. Singisetti

Migration Enhanced Epitaxial (MEE) S/D Regrowth*





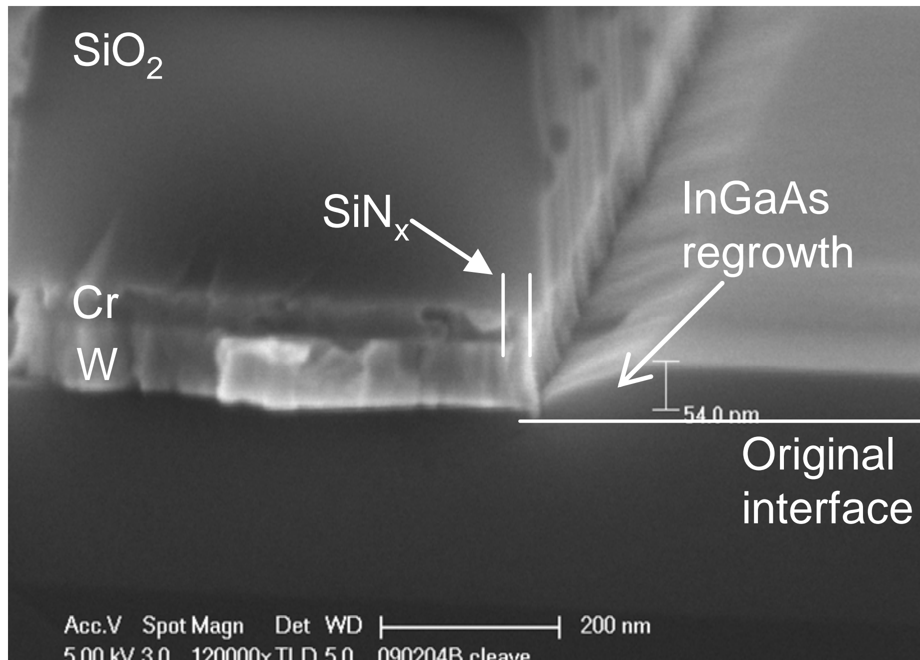
High temperature migration enhanced epitaxial regrowth

***Wistey, EMC 2008**

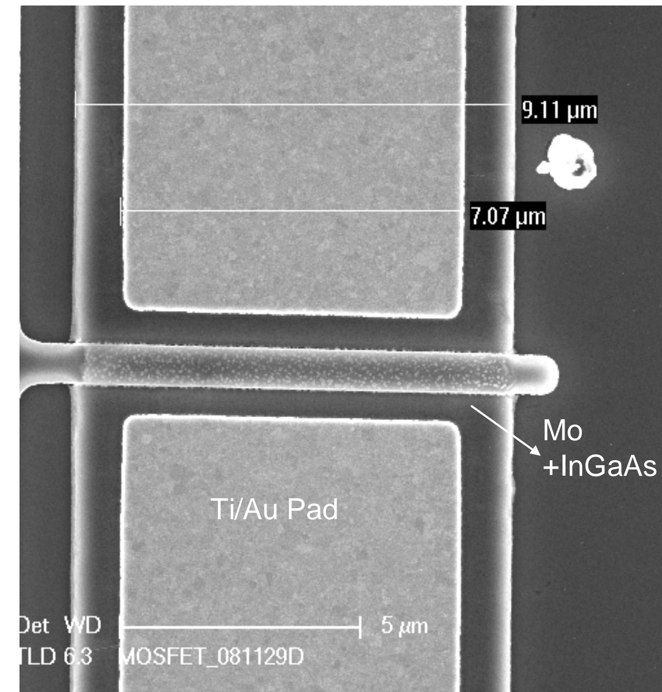
Wistey, ICMBE 2008

MBE growth by Dr. Mark Wistey, device fabrication and characterization by U. Singisetti

Regrown S/D III-V MOSFET: Images

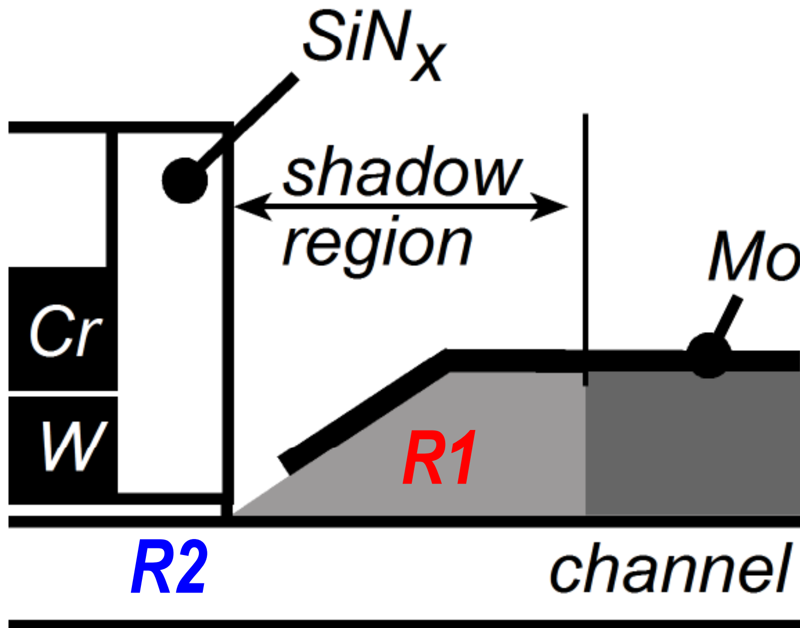


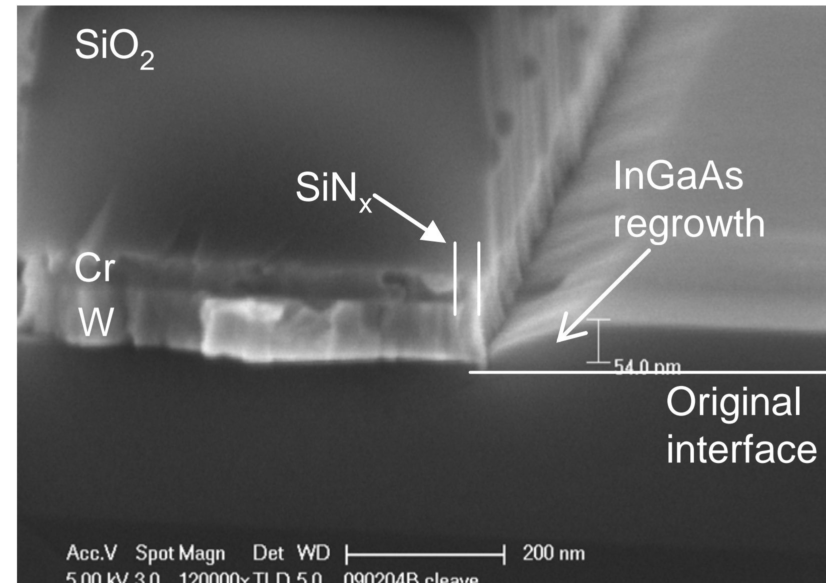
Cross-section after regrowth, but before Mo deposition



Top view of completed device

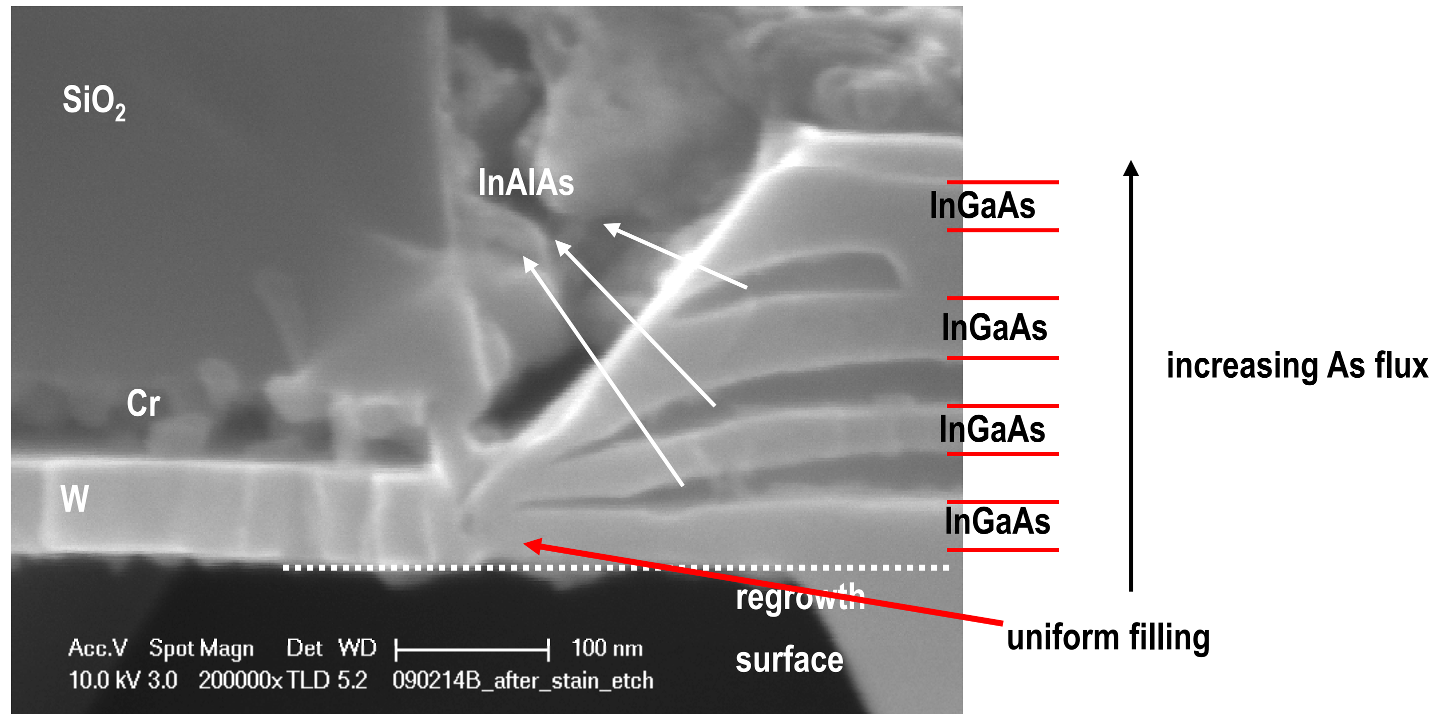
Source Resistance: electron depletion near gate





- *Electron depletion in regrowth shadow region (R_1)*
- *Electron depletion in the channel under SiN_x sidewalls (R_2)*

Regrowth profile dependence on As flux*



multiple InGaAs regrowths with InAlAs marker layers

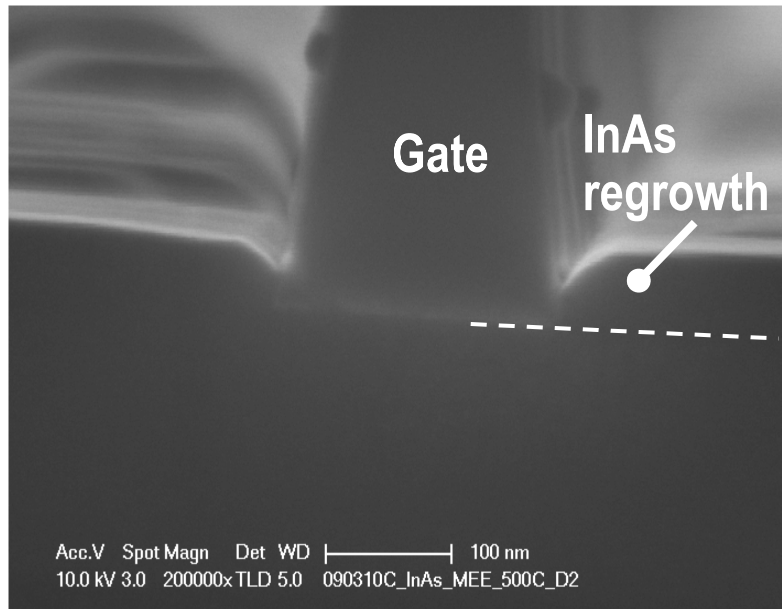
Uniform filling with lower As flux

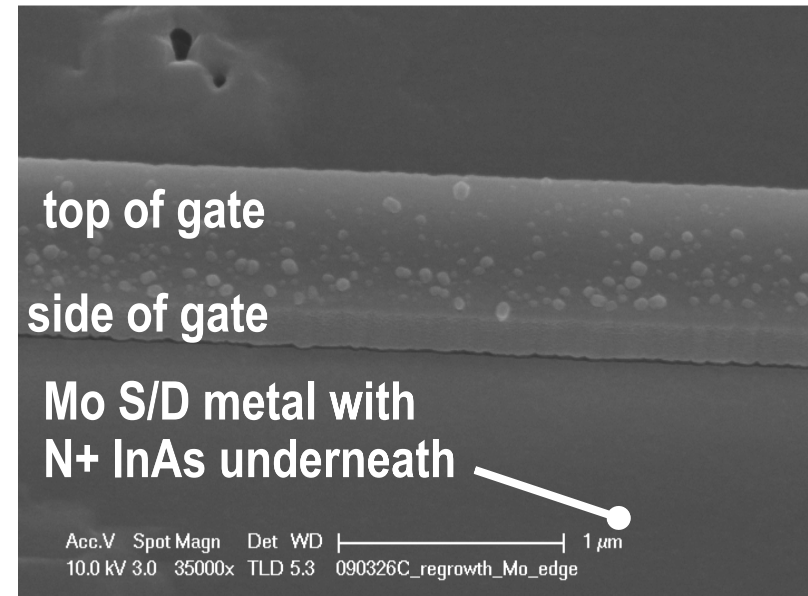
* Wistey *et al*, EMC 2009

Wistey *et al* NAMBE 2009

MBE growth by Dr. Mark Wistey, device fabrication and characterization by U. Singisetti

InAs source/drain regrowth





***Improved InAs regrowth with low As flux for uniform filling*[1]**

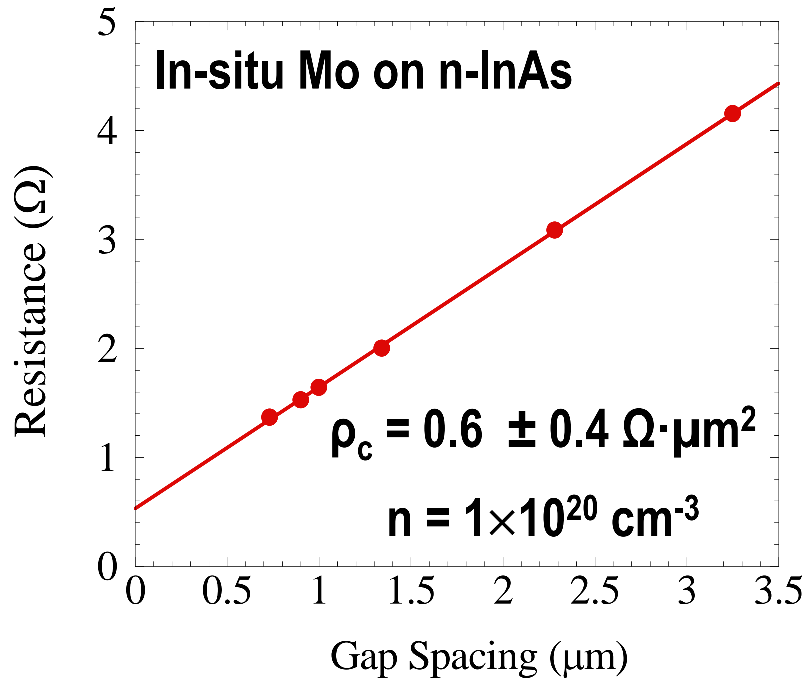
***InAs less susceptible to electron depletion: Fermi pinning above E_c*[2]**

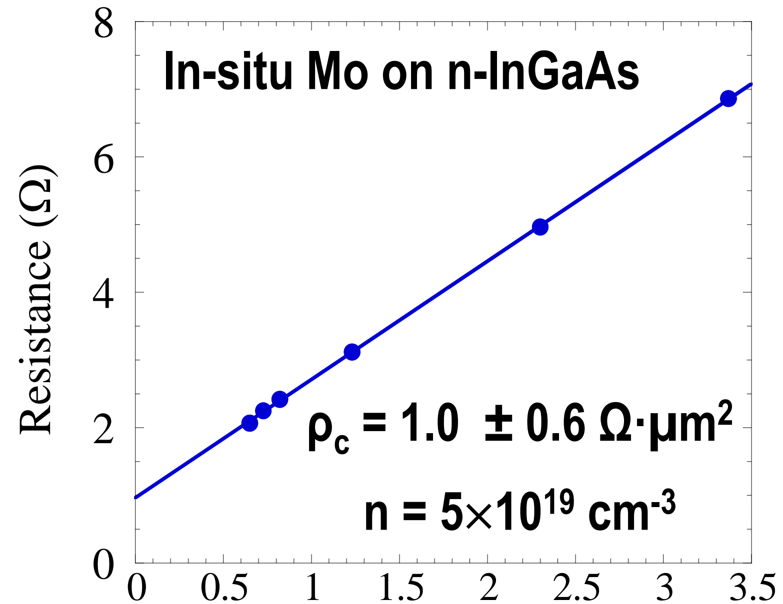
[1] Wistey *et al*, EMC 2009

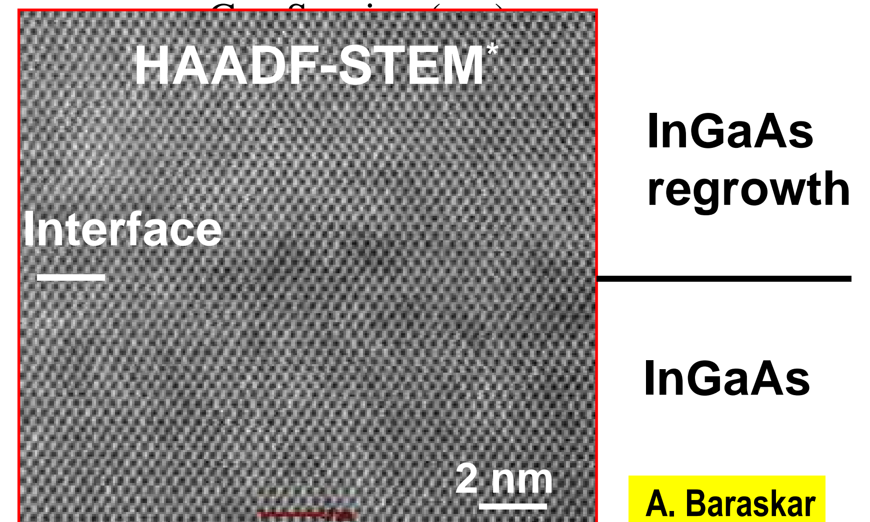
Wistey *et al* NAMBE 2009.

[2]Bhargava *et al* , APL 1997

In-Situ Refractory Ohmics on MBE Regrown N-InGaAs





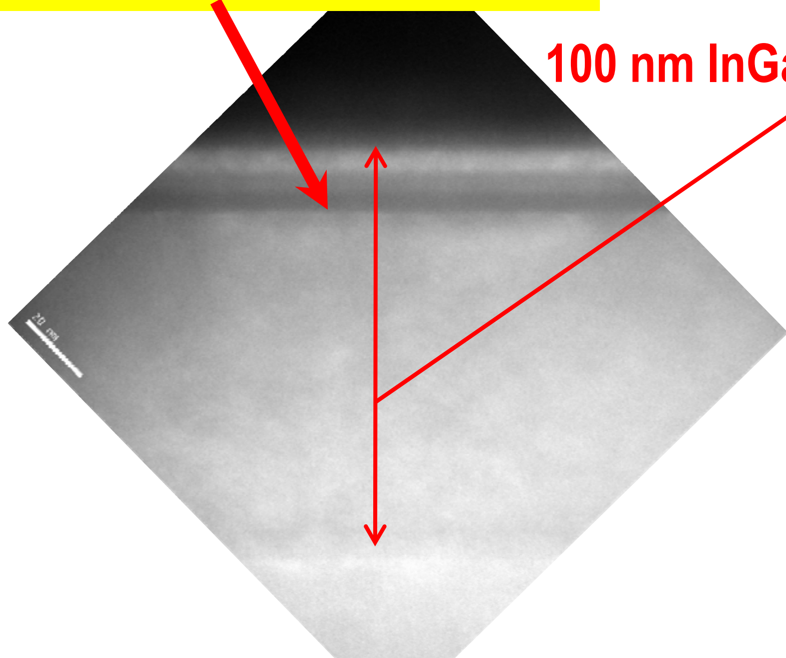


A. Baraskar

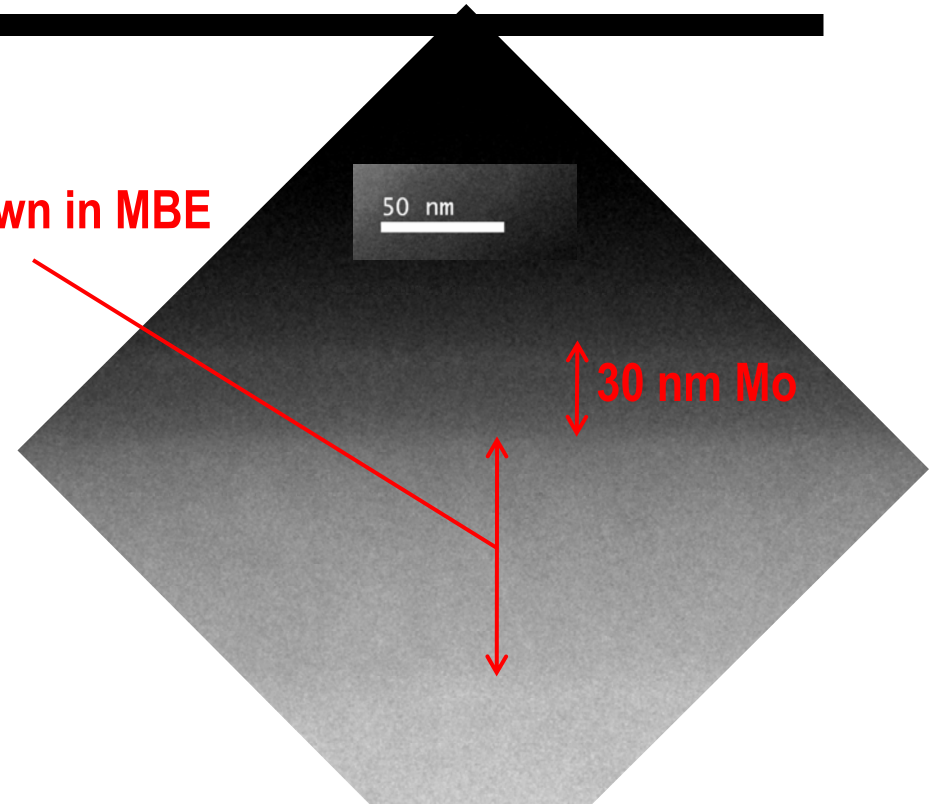
TEM by Dr. J. Cagnon, Stemmer Group, UCSB

Benefits of refractory contacts

15 nm Pd/Ti diffusion



100 nm InGaAs grown in MBE



After 250°C anneal, Pd/Ti/Pd/Au *diffuses* 15nm into semiconductor
deposited Pd thickness: 2.5nm

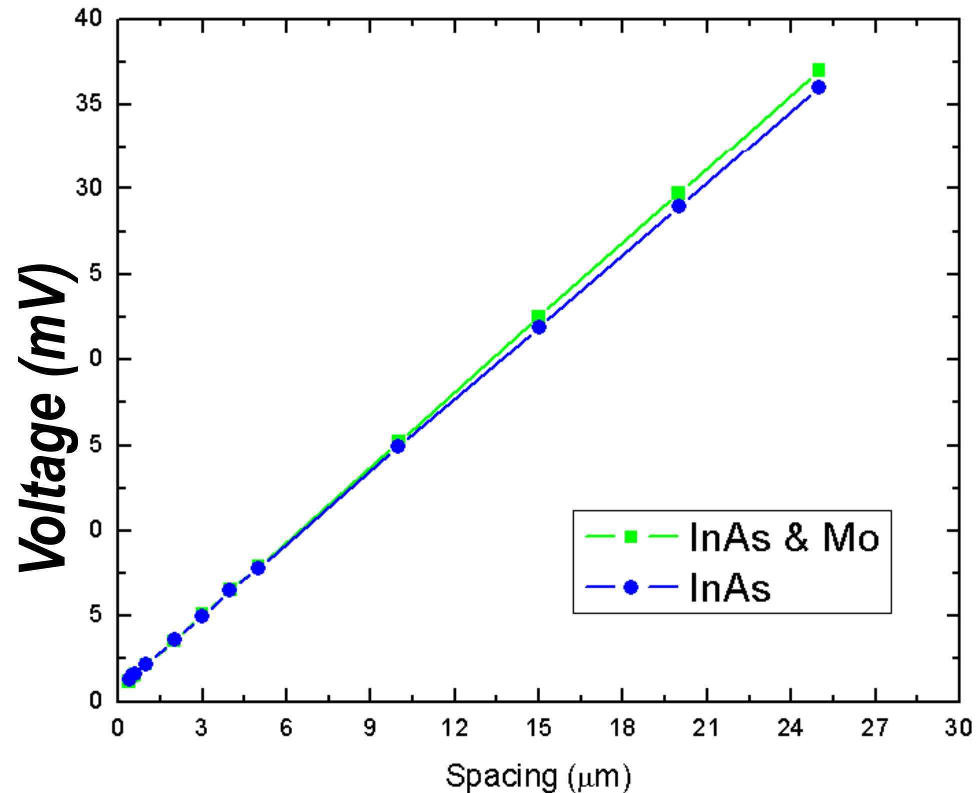
Refractory Mo contacts *do not diffuse measurably*

Refractory, non-diffusive metal contacts for thin semiconductor layers

A.. Baraskar

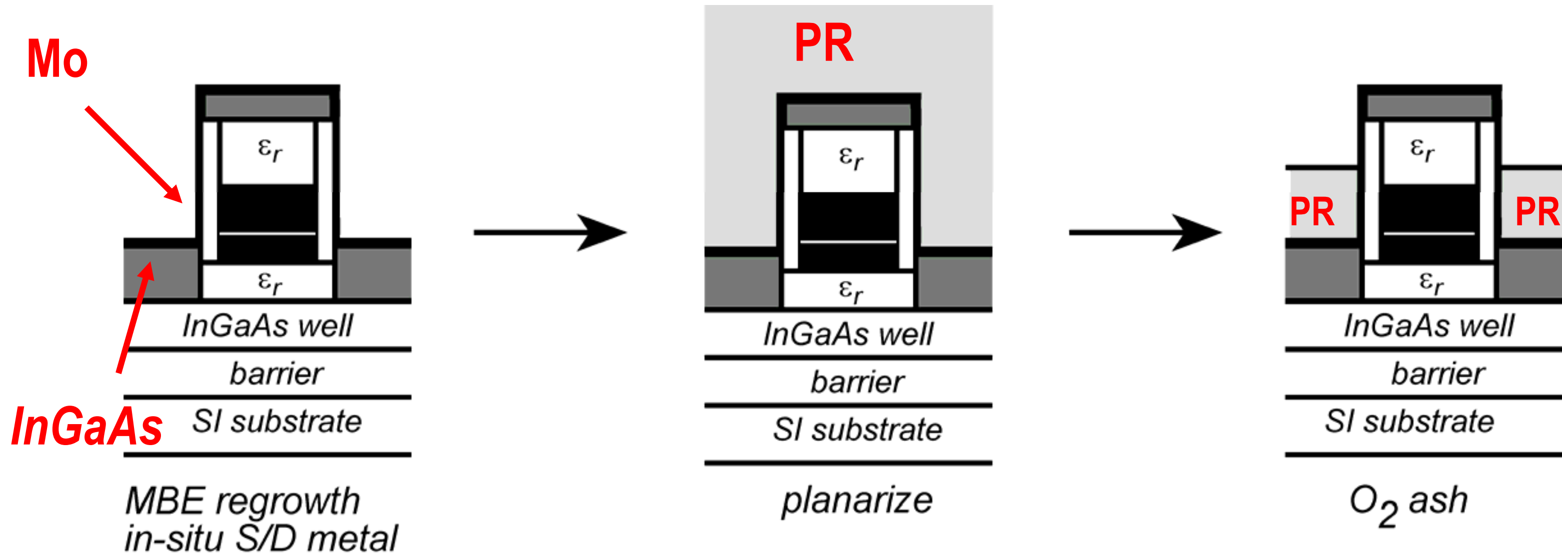
Resistivity of MEE Regrowth

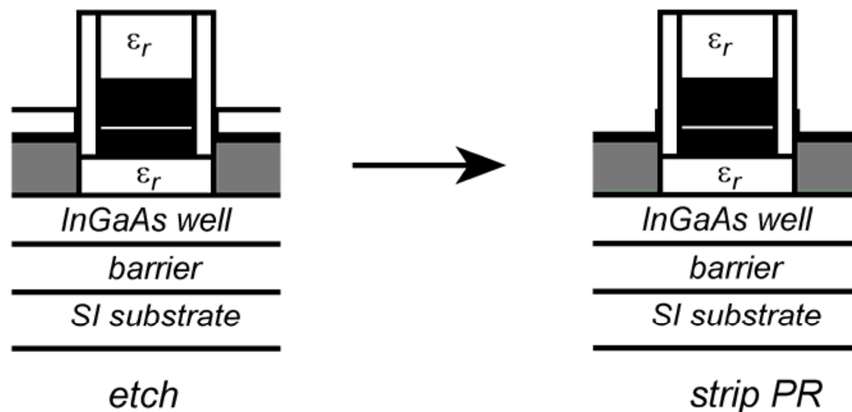
15 μm TLM width

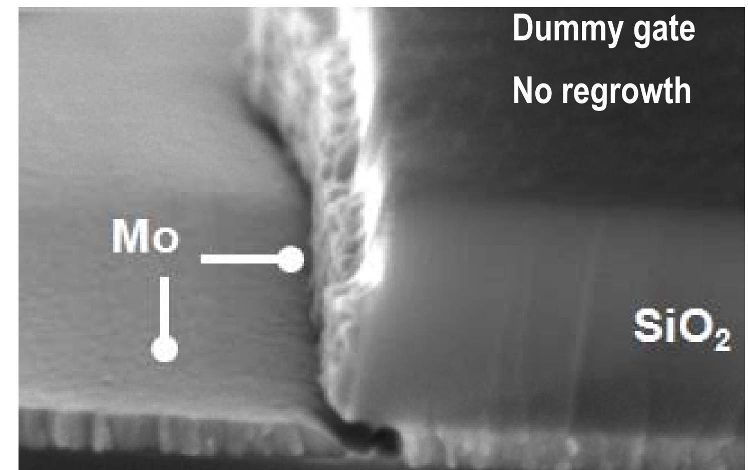


~50 nm InAs regrowth has ~22 Ω sheet resistivity
Contact resistivity is ~1.2 Ω-μm^2.

Self-Aligned Contacts: Height Selective Etching*

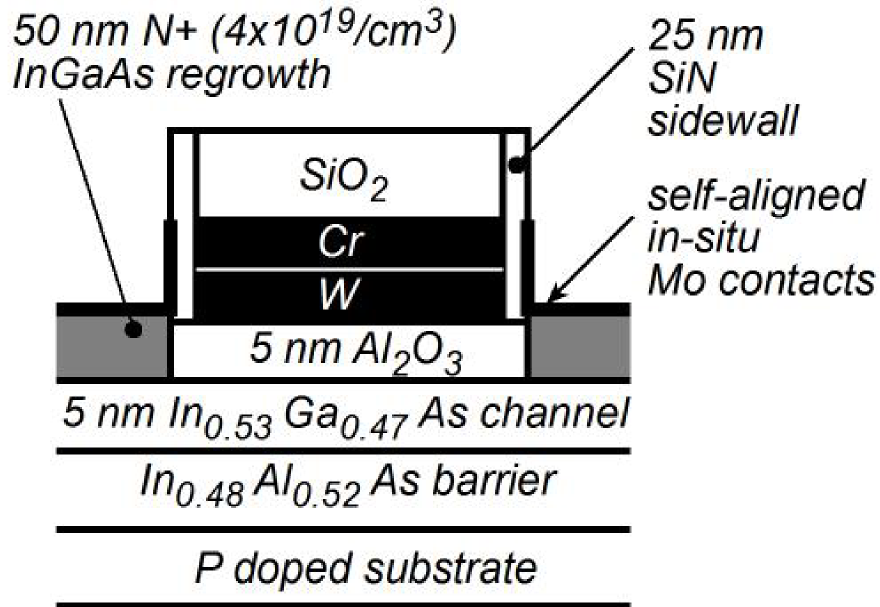


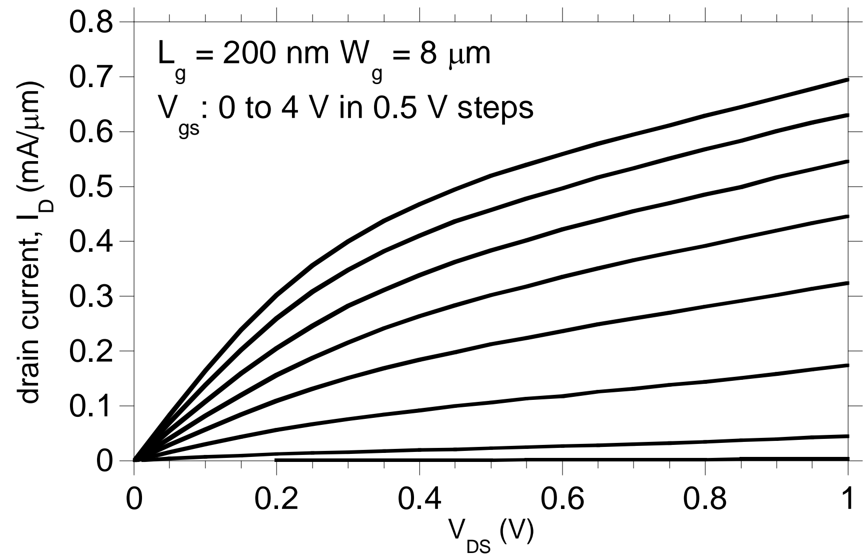


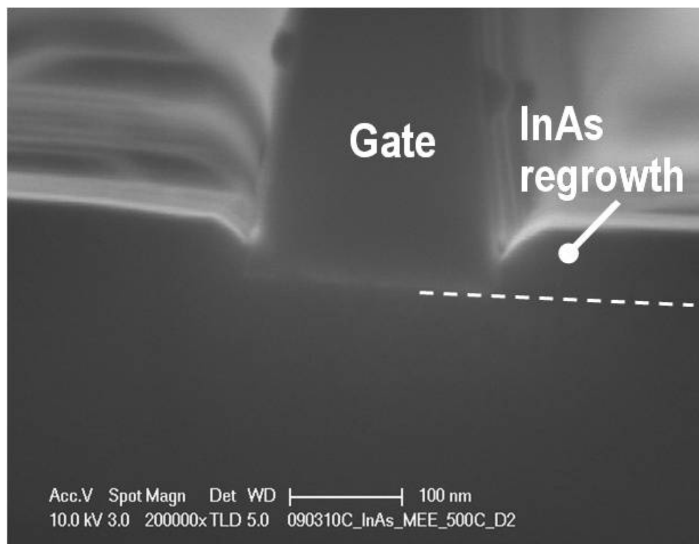


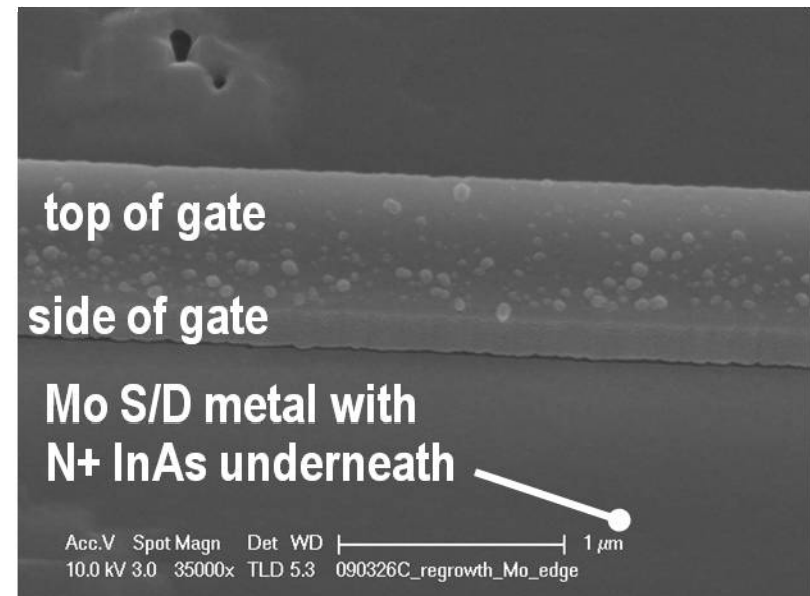
* Burek *et al*, J. Cryst. Growth 2009

Fully Self-Aligned III-V MOSFET Process

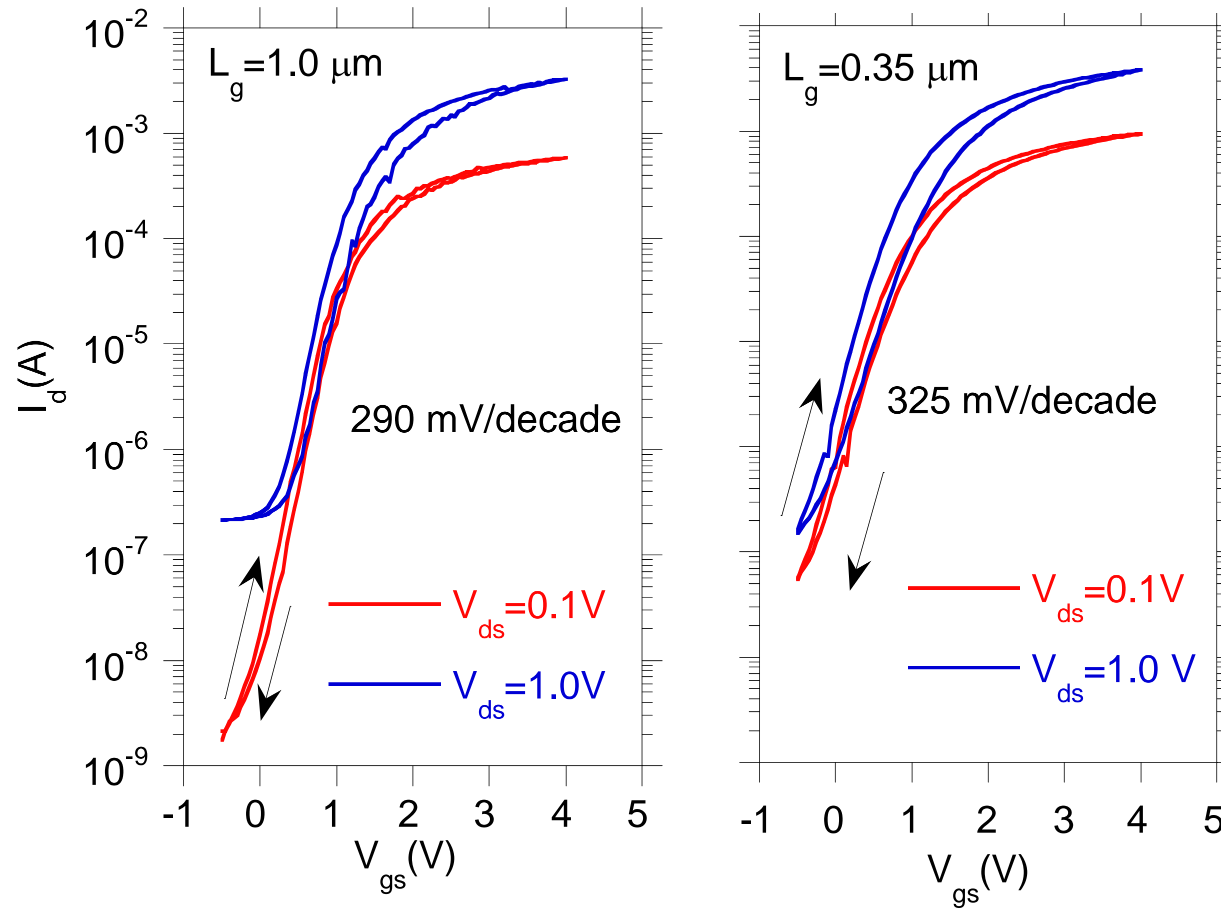




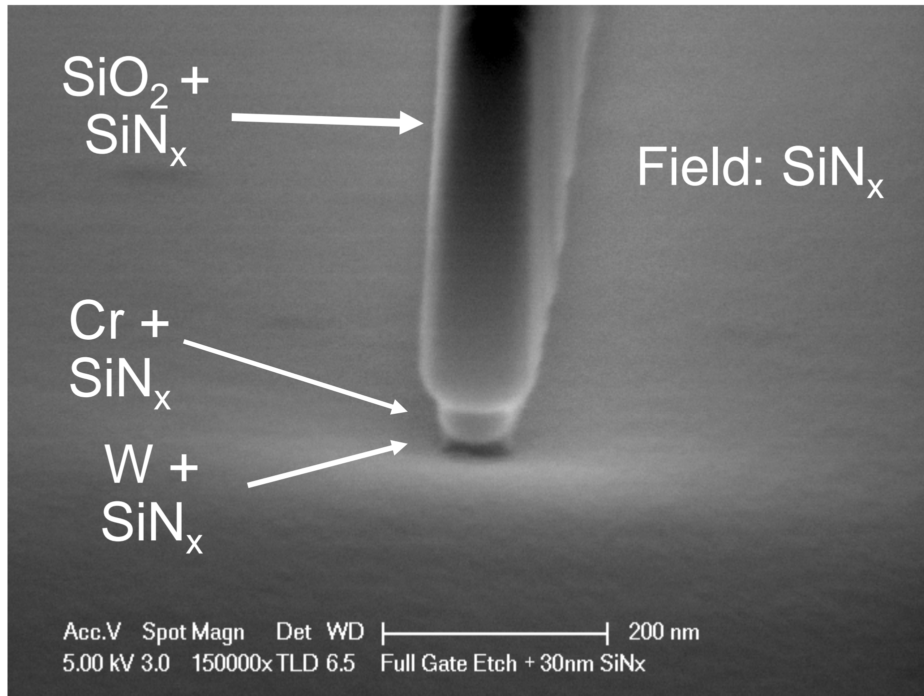


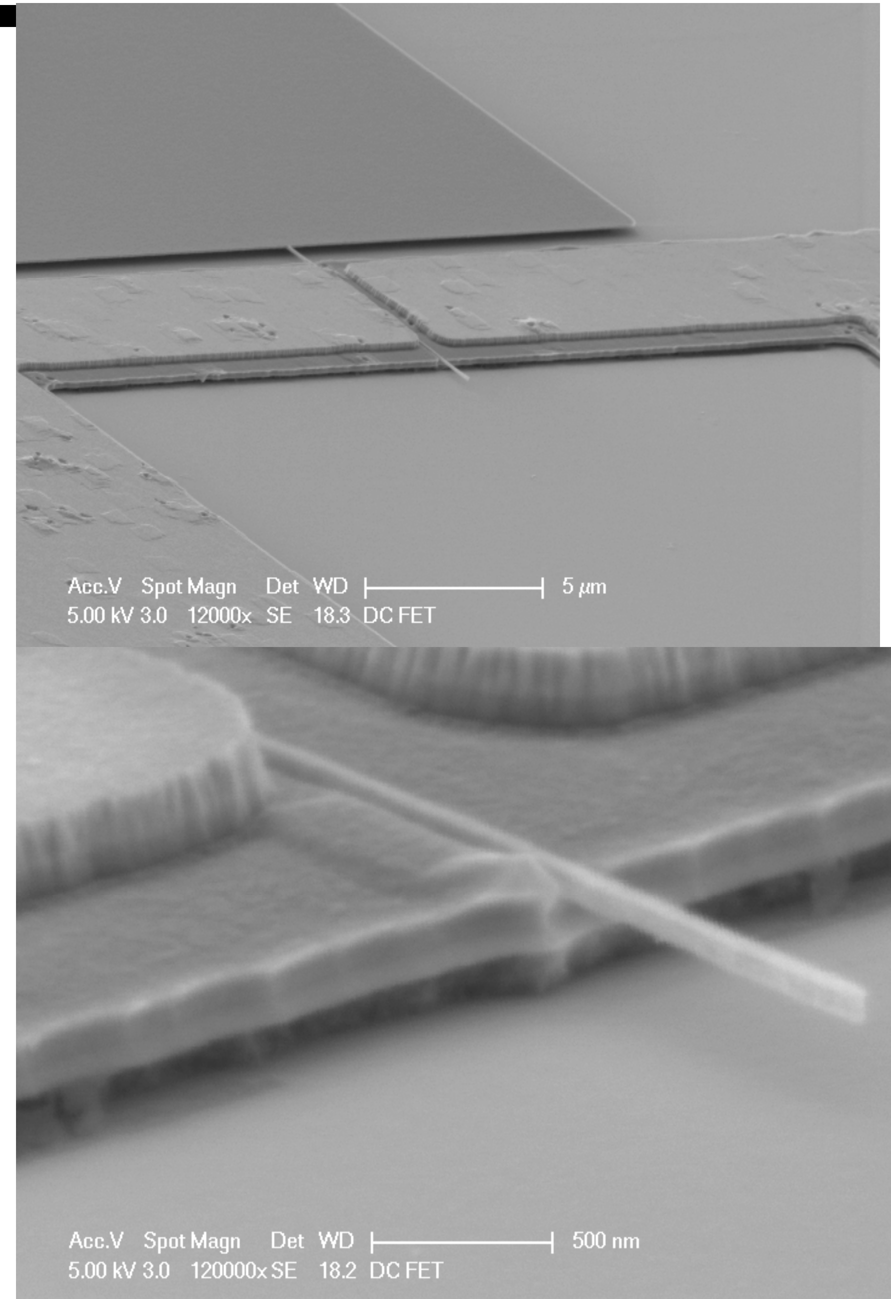


Subthreshold characteristics



10-30 nm Process Development



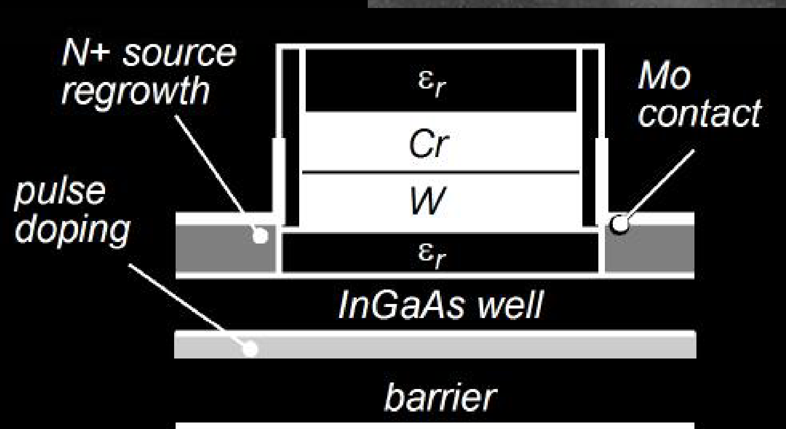


Excellent structural yield in sub-100nm process flow

27 nm Self-Aligned InGaAs MOSFET

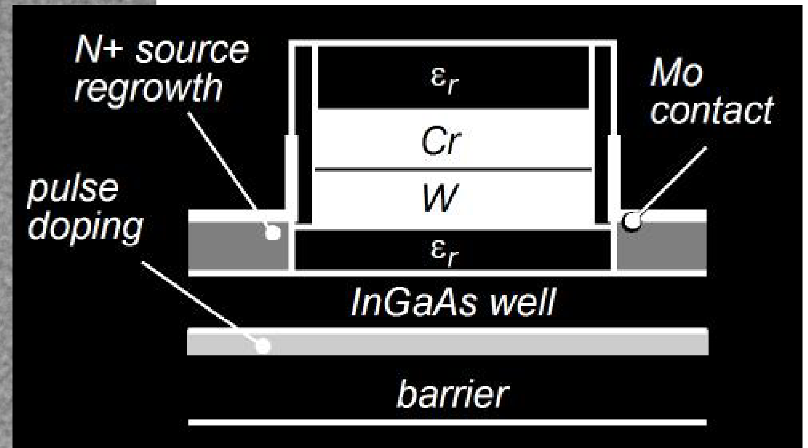
Self-aligned N+ S/D regrowth
shallow , high doping , low sheet ρ

Self-aligned Mo in-situ S/D contacts:
low ρ , refractory → shallow

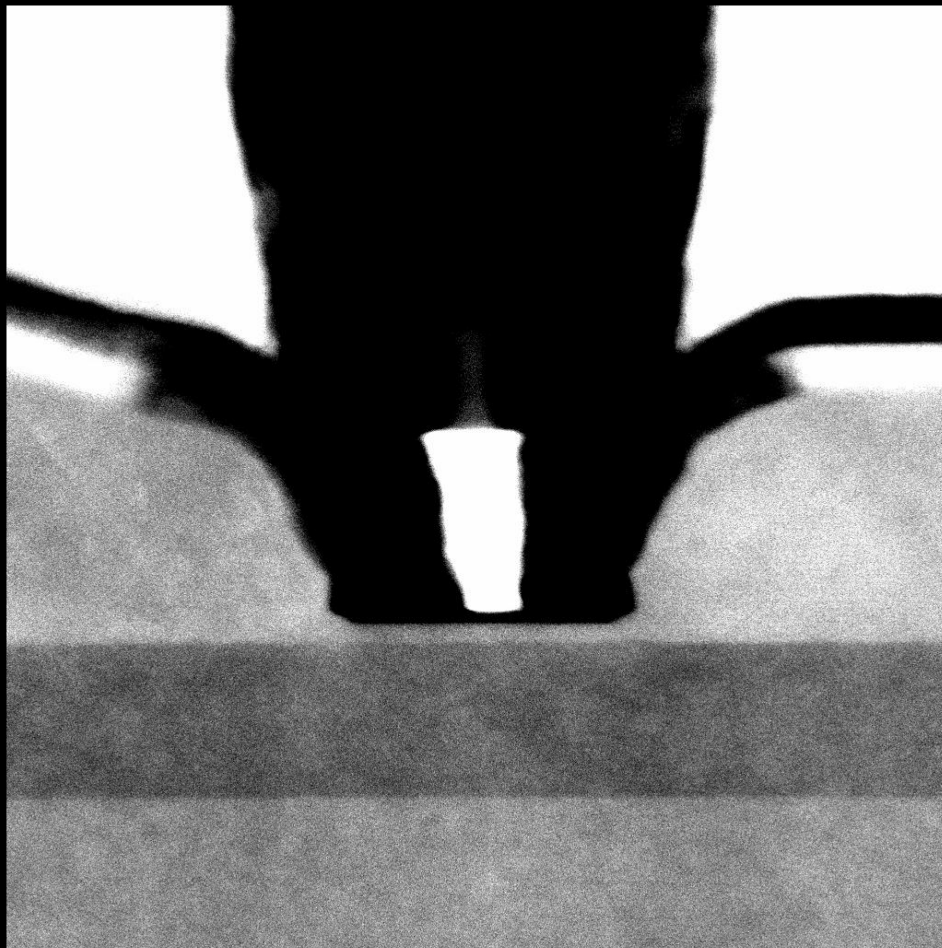


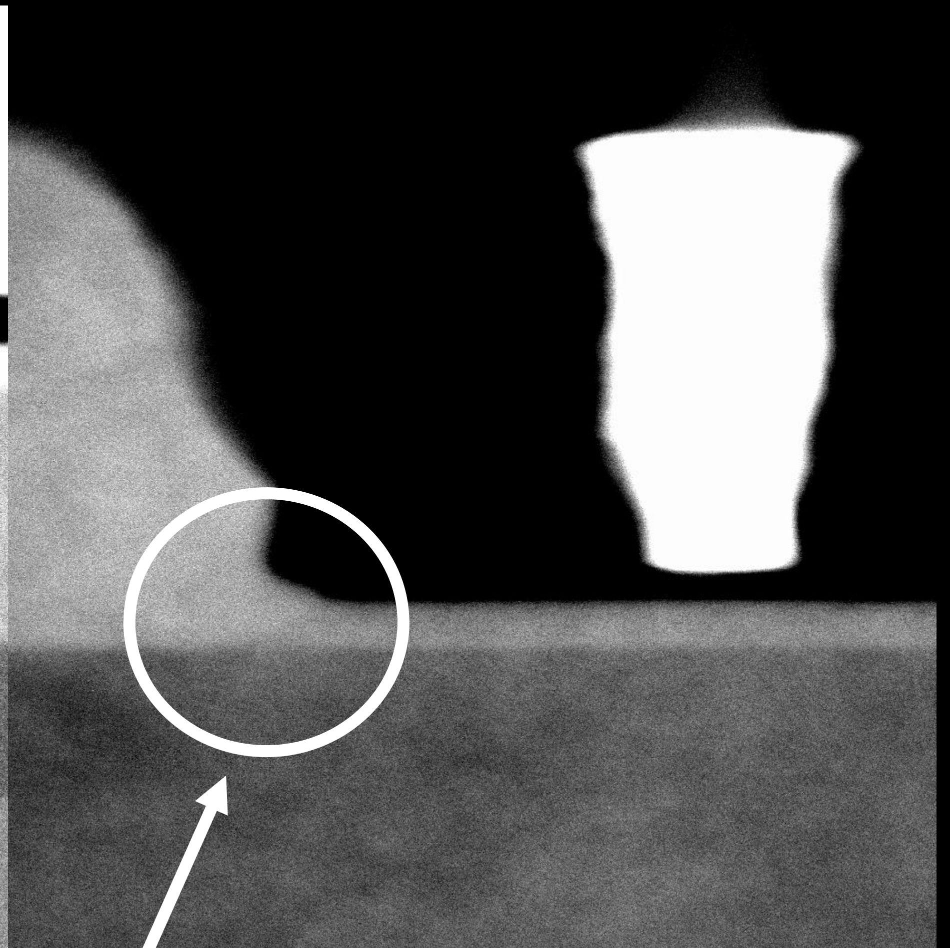
100 nm

HAADF TEM



HAADF TEM





STEM is chemical contrast imaging -> Is the regrowth sinking?

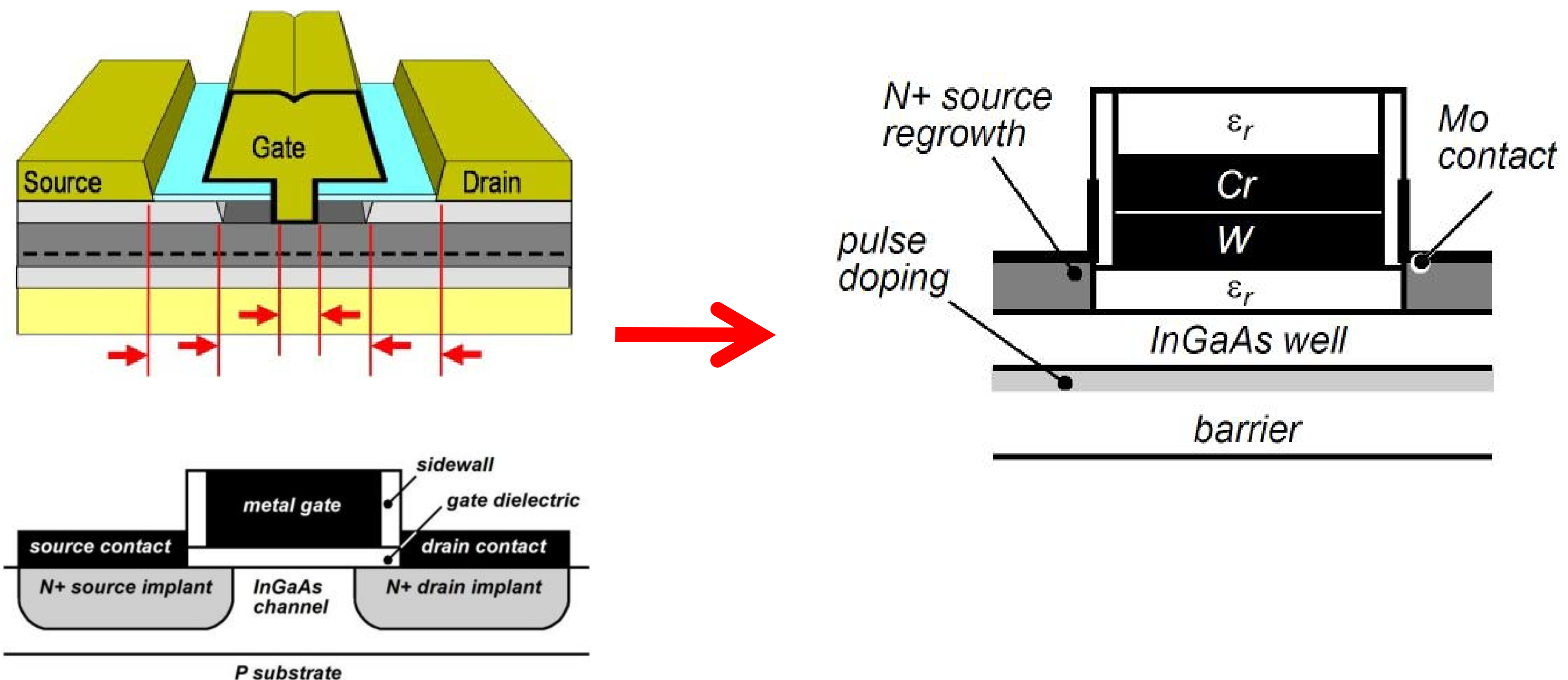
Conclusion

III-V MOS

With appropriate design, III-V channels can provide > current than Si
...even for highly scaled devices

But present III-V device structures are also unsuitable for 10 nm MOS
large access regions, low current densities, deep junctions

Raised S/D regrowth process is a path towards a nm VLSI III-V device



(end)