III-V MOSFETs: Scaling Laws, Scaling Limits, Fabrication Processes

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Abstract—III-V FETs are in development for both THz and VLSI applications. In VLSI, high drive currents are sought at low gate drive voltages, while in THz circuits, high cutoff frequencies are required. In both cases, source and drain access resistivities must be decreased, and transconductance and drain current per unit gate width must be increased by reducing the gate dielectric thickness, reducing the inversion layer depth, and increasing the channel 2-DEG density of states. We here describe both nm self-aligned fabrication processes and channel designs to address these scaling limits.

I. Introduction

III-V transistors of ~10 to 100 nm lithographic dimensions are being developed both for sub-mm-wave (0.3--3 THz) applications and for use in large-scale digital integrated circuits. Both applications demand improved transistor characteristics; both applications demand significant changes in the design and fabrication of the channel, of the source/drain access regions, and of the gate dielectric.

For application in VLSI, FET leakage currents must be low and drain drive current densities must be high despite low supply voltages. High intrinsic transconductance and low source / drain access resistivities are therefore required.

For application in THz ICs, high current-gain (f_τ) and power-gain ($f_{\max}$) cutoff frequencies are required. With present InGaAs HEMTs, f_τ is limited by parasitic capacitance charging times which are only reduced by increasing the FET transconductance per unit gate width. As with the VLSI application, the drive current and transconductance must be increased and the source access resistance reduced.

THz InGaAs HEMTs and InGaAs MOSFETs thus face several similar design challenges. To increase the transconductance of both HEMTs and MOSFETs, the gate barrier must be thinned, which increases gate leakage. In VLSI application, gate leakage must be very small, and an MOS structure with a wide-gap (insulating) gate dielectric is required. Even for HEMTs used in THz ICs, the wide-gap gate barrier semiconductor layer has been thinned to the point where gate leakage reduces microwave power gain; better barriers are needed. In both devices high transconductance implies both high carrier velocities and high carrier densities in the 2-dimensional electron gas. Semiconductors with low carrier effective mass provide high carrier velocities yet low 2-D densities of states hence low carrier densities, high effective mass provides low velocities yet high carrier densities. [1] This limitation must somehow be addressed. Both devices need low access resistances. Both devices need thin channels both for high transconductance and for low output conductance.

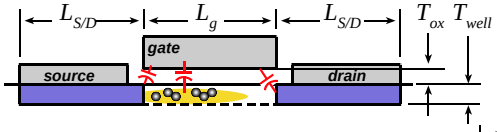
Design challenges with THz InGaAs HEMTs and InGaAs MOSFETs also differ in key aspects. Unlike THz HEMTs, where overall device dimensions can be much larger than the gate length, in VLSI the device packing density must be high hence all device dimensions must be small. In particular, in VLSI the source/drain contacts must have dimensions comparable to the gate length, placing greater demands on low-resistivity source/drain contacts. Similarly, while in THz HEMTs the N+ drain can have a large offset from the gate to reduce drain electrostatic coupling and consequently output conductance, in MOSFETs for VLSI both density and logic design requirements force the N+ drain region to be placed adjacent to or under the gate. Electrostatic design and vertical scaling of the VLSI device is therefore more demanding.

We describe below our efforts to develop III-V MOSFETs for VLSI. Although III-V MOS gate dielectrics [2, 3] remain an area of intense development, we focus here on device design and on development of process flows for fabrication of nm devices. Since their low 2-dimensional density of states makes III-V channel materials uncompetitive for application in nm FETs, we also discuss modified III-V channel designs which address this limitation.

II. FET Scaling Laws

First consider FET scaling laws (Table 1) [4] . To increase bandwidth γ:1, capacitances and transit delays must be reduced γ:1 while maintaining constant voltages, currents, and resistances. In InGaAs FETs with L_g ~35 nm, the gate-source $C_{gs,f} \propto \varepsilon W_g$ and gate-drain $C_{gd} \propto \varepsilon W_g$ fringing capacitances are a *substantial* fraction of the total capacitance, and consequently limit f_τ . $C_{gs,f}$ and C_{gd} are only weakly dependent on lateral

Table 1: Constant-voltage / constant-velocity FET scaling laws: changes required for γ:1 increased bandwidth in an arbitrary circuit



parameter	law	parameter	law
gate length L_g, source-drain contact lengths $L_{S/D}$ (nm)	γ^{-1}	electron density $n_s = (C_{g-ch}/L_g W_g)(V_{gs}-V_{th})/q$ (cm^{-2})	γ^{1}
gate width W_g (nm)	γ^{-1}	injection velocity (m/s) $v_{injection} = (4/3\pi)(2qC_{g-ch}(V_{gs}-V_{th})/m_{\|}C_{dos})^{1/2}$	γ^{0}
equivalent oxide thickness $T_{eq} = T_{ox}\varepsilon_{SiO_2}/\varepsilon_{oxide}$ (nm)	γ^{-1}	drain current $I_d = qn_s v_{injection}$ (mA)	γ^{0}
dielectric capacitance $C_{ox} = \varepsilon_{SiO_2} L_g W_g / T_{eq}$ (fF)	γ^{-1}	drain current density I_d/W_g ($\mathrm{mA}/\mu\mathrm{m}$)	γ^{1}
		transconductance $\partial I_d/\partial V_{gs}$ (mS)	γ^{0}
wavefunction mean depth T_{inv} (nm)	γ^{-1}	gate-source, gate-drain fringing capacitances $C_{gs,f} \propto \varepsilon W_g$, $C_{gd} \propto \varepsilon W_g$ (fF)	γ^{-1}
wavefunction depth capacitance $C_{depth} = \varepsilon_{semi} L_g W_g / T_{inv}$ (fF)	γ^{-1}	S/D access resistances R_s, R_d (Ω)	γ^{0}
DOS capacitance (ballistic case) $C_{dos} = q^2 g (m_{\|}^* m_{\perp}^*)^{1/2} L_g W_g / 2\pi\hbar^2$ (fF)	γ^{-1}	S/D access resistivities $R_s W_g$, $R_d W_g$ ($\Omega-\mu$m)	γ^{-1}
		S/D contact resistivities ρ_c ($\Omega-\mu\mathrm{m}^2$)	γ^{-2}
gate-channel capacitance $C_{g-ch} = [1/C_{ox} + 1/C_{depth} + 1/C_{DOS}]^{-1}$ (fF)	γ^{-1}	temperature rise (one device, K)	$\sim W_g^{-1}$

geometry, hence the $(C_{gs,f}+C_{gd})\Delta V/I_d$ delay is reduced γ:1 only if I_d/W_g is increased γ:1.

Consider drive current scaling in the ballistic limit. $I_d = qn_s v_{inj}$ is determined by the carrier injection velocity v_{inj} and the sheet carrier concentration $n_s = (C_{g-ch}/L_g W_g)(V_{gs}-V_{th})/q$, where the gate-channel capacitance $C_{g-ch} = [1/C_{ox} + 1/C_{depth} + 1/C_{DOS}]^{-1}$ is the series combination of dielectric $C_{ox} = \varepsilon_{SiO_2} L_g W_g / T_{eq}$, wavefunction depth $C_{depth} = \varepsilon_{semi} L_g W_g / T_{inv}$ and density of states $C_{dos} = q^2 \cdot dn_s/dE_f$ capacitances. T_{inv} is here the wavefunction mean depth. In the ballistic case, $C_{dos} = q^2 g (m_{\|} m_{\perp})^{1/2} L_g W_g / 2\pi\hbar^2$, where g is the # of populated valleys, and $m_{\|}$ and $m_{\perp}$ the effective masses parallel and perpendicular to transport; near equilibrium, C_{dos} is 2:1 larger. Given ballistic transport [5] and assuming degenerate carrier concentrations, $E_f - E_{well} >> kT$, $v_{inj} = (4/3\pi)(2(E_f - E_{well})/m_{\|})^{1/2} = (4/3\pi)(2qC_{g-ch}(V_{gs}-V_{th})/m_{\|}C_{dos})^{1/2}$. We scale by maintaining constant v_{inj} while reducing $C_{ox}/L_g W_g$, $C_{depth}/L_g W_g$, and $C_{dos}/L_g W_g$ by γ:1 so as to increase n_s by γ:1. This requires fixed transport mass $m_{\|}$, T_{eq} and T_{inv} reduced γ:1, and C_{dos} increased γ:1 by increasing the # of valleys or the perpendicular mass.

The FET is scaled such that the on-state current density I_d/W_g ($\mathrm{mA}/\mu\mathrm{m}$) varies as γ^1 while the current per unit source and drain Ohmic contact area ($\mathrm{mA}/\mu\mathrm{m}^2$) varies as γ^2. It is well understood that difficulties in reducing T_{eq} (gate leakage by tunneling) will impede constant-voltage FET scaling; note also that T_{inv} must scale as γ^{-1}, requiring thinner wells or stronger confinement of the wavefunction in the well by strong vertical fields, and $(R_s+R_d)/W_g$ must scale as γ^{-1}, requiring a γ^2:1 reduction in contact resistivity ρ_c and increased carrier concentrations in the access regions. Design goals include low access resistance, high drive current density, thin wells, high sheet carrier density, and gate barriers that are both thin and high in energy.

To out-perform future scaled Si MOSFETs, drive currents must exceed 1-2 $\mathrm{mA}/\mu\mathrm{m}$ at 300 mV gate overdrive $(V_{gs}-V_{th})$. We must develop Ohmic contacts of ~0.5 $\Omega-\mu\mathrm{m}^2$ contact resistivity; this resistivity must not increase when operating ~150 $\mathrm{mA}/\mu\mathrm{m}^2$ current density, nor can the contact metals diffuse under such high current and thermal stress through device junctions only ~3-5 nm below the surface. T_{inv} must be at most 2-3 nm.

We describe our efforts to develop process to fabricate FETs having such parameters. We must also consider changes in the channel design necessary to enable the target high current densities.

III. Density-Of-States Limits And High Current Density Channels

We now examine the density-of-states limit to drive current and modified channel designs which address this limit.

Low transport mass produces high carrier velocities but low charge densities while high transport mass produces low carrier velocities but high charge densities. At a given dielectric thickness T_{equiv}, there is an optimum m^* maximizing I_d. We find

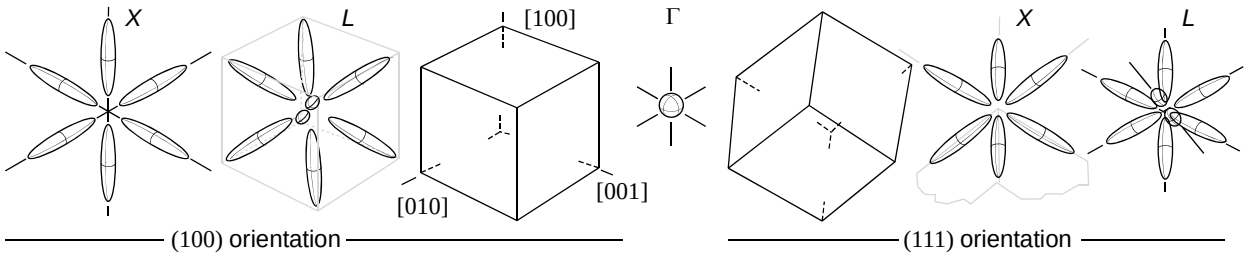


Figure 1: Γ , L, and X-valley orientations for (100)- and (111)-oriented wafers

Table 2 Parameters of Γ , L, and X-valleys for several suitable semiconductors

		Γ valley	X valleys*			L valleys		
material	substrate	m^*/m_0	m_l/m_0	m_t/m_0	$E_X - E_\Gamma$	m_l/m_0	m_t/m_0	$E_L - E_\Gamma$
$In_{0.5}Ga_{0.5}As$	InP	0.045	1.29	0.19	0.83 eV	1.23	0.062	0.47 eV
InAs	InP	0.026	1.13	0.16	0.87 eV	0.65	0.050	0.57 eV
GaAs	GaAs	0.067	1.3	0.22	0.47 eV	1.9	0.075	0.28 eV
GaSb	GaSb	0.039	1.51	0.22	0.30 eV	1.3	0.10	0.07 eV
Si	Si		0.92	0.19	(negative)	*Si minima at $\Delta \sim 0.85 \cdot \langle 100 \rangle$		

$$I_d / W_g = J_0 \cdot K_1 \cdot ((V_{gs} - V_{th})/1\text{V})^{3/2} \quad , \qquad (1)$$

where

$$J_0 = \left(\frac{4}{3\pi}\right)\left(\frac{2q}{m_0}\right)^{1/2}\left(\frac{q^2 m_0}{2\pi\hbar^2}\right)(1\text{ V})^{3/2} = 84\ \text{mA}/\mu\text{m} \qquad (2)$$

and

$$K_1 = \frac{n \cdot (m_\perp / m_o)^{1/2}}{(1 + (C_{dos,o}/C_{eqvuiv}) \cdot g \cdot (m_\perp^{1/2} m_\parallel^{1/2}/m_o))^{-3/2}} \qquad (3)$$

is the normalized current density. $C_{equiv} = [1/C_{ox} + 1/C_{inv}]^{-1}$ is C_{depth} and C_{ox} in series, while $C_{dos,o} = q^2 m_0 L_g W_g / 2\pi\hbar^2$ . . Given one isotropic valley ($m_\perp = m_\parallel = m^*$, g =1) and 1 nm *total* equivalent dielectric thickness EOT (i.e. $C_{equiv} = \varepsilon_{r,SiO_2} L_g W_g /(1\text{ nm})$), highest current is obtained for m^*/m_0 =0.05, while for 0.3 nm EOT, peak I_d is obtained at m^*/m_0 =0.2; given one isotropic valley, low m^* gives low I_d in nm FETs [6], though low m^* reduces transit time for any EOT. Note than for Si {100} FETs [6], m^*/m_0 =0.19 and g =2.

Consider a 3 nm (100) GaAs well with strained AlSb barriers. The L bound states lie 177 meV above that of Γ . Equilibrium (not ballistic transport) analysis uses Schrödinger-Poisson, the effective mass approximation, and parabolic bands. 0.66 nm Al_2O_3 and 0.34 nm AlSb lie between the well and gate, giving T_{eq} =0.37 nm. Under strong inversion $C_{g-ch}/L_g W_g \cong 2.4$ $\mu\text{F}/\text{cm}^2$, far below $C_{ox}/L_g W_g$ =9 $\mu\text{F}/\text{cm}^2$, and the high-mass L-valleys fill for $n_s > 2.4 \cdot 10^{12}\ \text{cm}^{-2}$. Under ballistic transport, C_{dos} and the maximum n_s would both decrease 2:1.

Increased C_{dos} and low $m_\parallel$ can be obtained by using L valley minima alone or combined with the Γ valley. The InGaAs, GaAs, and GaSb L-valleys [7] have low m_t/m_o (0.062-0.1) and high m_l/m_o (1.23-1.9). The L-valleys have $\langle 111 \rangle$ orientations, and transport in a (100) channel includes contributions from the high m_l. Using instead a (111) wafer, the L[111] valley is oriented vertically, and shows low transport masses ($m_\parallel = m_\perp = m_t$) and high confinement mass ($m_q = m_l$). The L$[\bar{1}11]$, $[1\bar{1}1]$, and $[11\bar{1}]$ minima show high transport mass[6] $(m_t + 8m_l)/9$ in one in-plane direction, but low confinement mass [6] $m_q = 9m_t m_l/(m_t + 8m_l)$. The X valleys have $\langle 100 \rangle$ orientations, in bulk InGaAs, GaAs, and GaSb have minima well above Γ and L, and in a (111) well have low $m_q = 3m_t m_l/(m_t + 2m_l)$ quantization mass. In appropriate thin wells, the X and L$[\bar{1}11]$, $[1\bar{1}1]$, and $[11\bar{1}]$ quantized states are driven to high energies and depopulated. T_{well} can be selected to place Γ and L[111] at similar energies, doubling C_{dos}, or Γ driven in energy above L[111], and transport provided in multiple L[111] valleys.

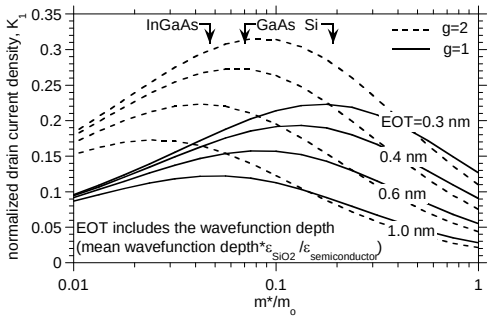


Figure 2: FET normalized drive current K_1 where $I_d / W_g = (84\ \text{mA}/\mu\text{m}) \cdot K_1 \cdot ((V_{gs} - V_{th})/1\text{V})^{3/2}$, and g is the # of valley minima.

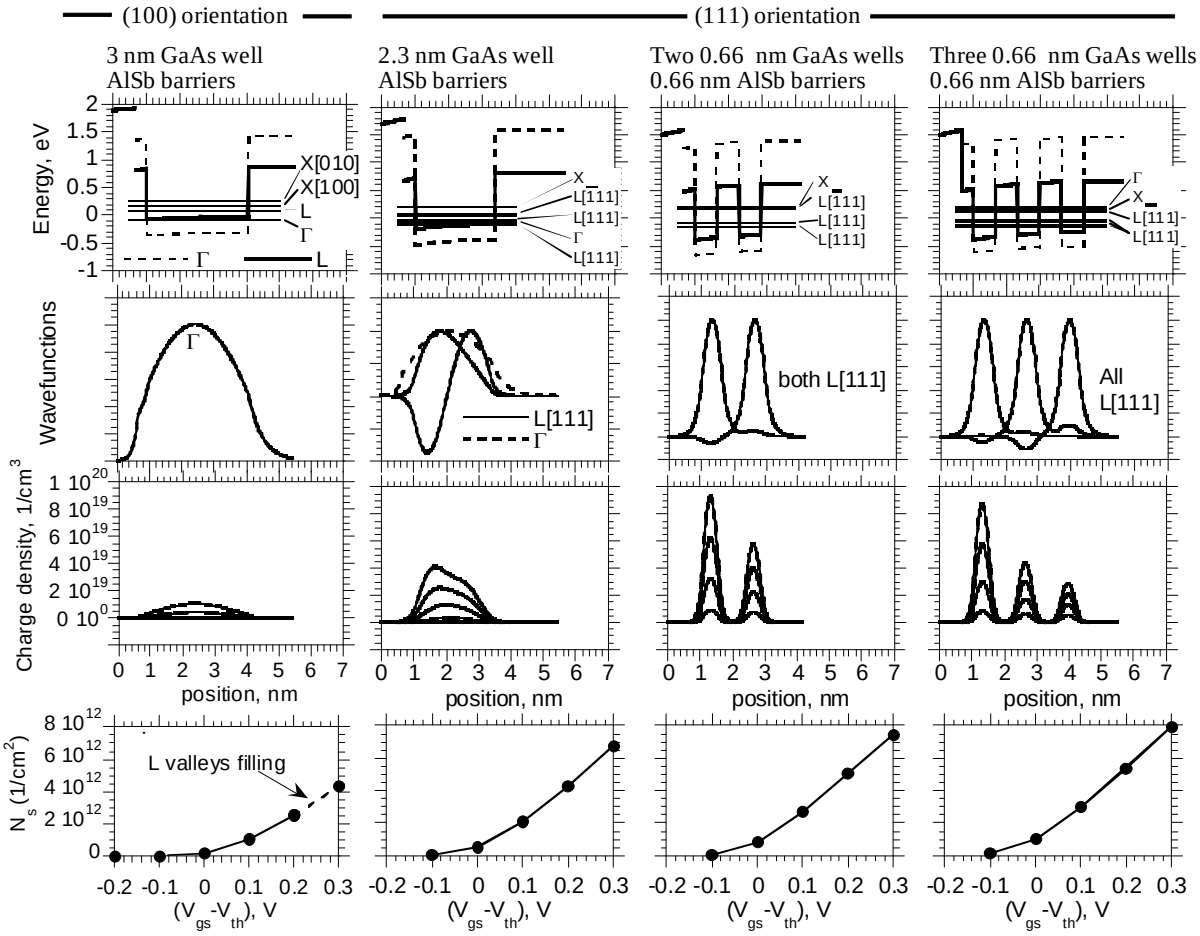


Figure 3: Simulation of Γ, Γ-L, and multiple-L valley FETs: quantized states, wavefunctions, charge density, and sheet carrier concentrations vs. bias. Well energies and charge densities calculated using the effective mass approximation and assuming parabolic bands. The gate dielectric is 0.3 nm Al_2O_3. Well charge densities are computed assuming thermal equilibrium; in the ballistic limit, C_{does} is 2:1 smaller than in equilibrium, and multiple-valley FET channels provide a proportionally larger improvement in N_S. 0.66 nm is 2 monolayers.

Consider a 2.3 nm (111) GaAs well with strained AlSb barriers. m_q is large, thus the first two L[111] states are separated by only 84 meV. The Γ state lies 41 meV above the lower L[111] state; 3 valleys are populated over a 300mV range of V_{gs}. L$[\bar{1}11]$, L$[1\bar{1}1]$, and L$[11\bar{1}]$ and X lie 175 and 288 meV above the lower L[111] state. In equilibrium simulation n_s = $7\cdot10^{12}$ cm^{-2} with $V_{gs}-V_{th}$ =300 mV, and moderately higher n_s does not populate heavy valleys. In inversion, $C_{g-ch}/L_gW_g \cong 4$ μF/cm^2. The benefit over the (100) design is larger in the ballistic case.

In InGaAs, GaAs, and GaSb, the L-valley m_l is >25:1 larger than the Γ-valley mass, hence T_{well} can be made 5:1 smaller for a given quantization energy. m_q is high in the barriers, hence multiple wells can be placed between ~ 1 nm barriers without significant well coupling hence energy redistribution. Multiple L[111] quantum wells can stacked to increase g hence C_{dos}.

Consider a FET with two 0.66 nm (2 ML) (100) GaAs wells separated by strained 0.66 nm AlSb barriers. Given zero field, the two L[111] states split in energy by < 40 meV; for $V_{gs}-V_{th}$ =300 mV the separation is 56 meV. L$[\bar{1}11]$, L$[1\bar{1}1]$, and L$[11\bar{1}]$ and X lie 322 and 346 meV above the lower L[111] state. The Γ state is driven to high energy. In equilibrium, n_s is driven to $7.8\cdot10^{12}$ cm^{-2} with $V_{gs}-V_{th}$ ~300 mV; moderately higher n_s does not populate heavy valleys. $C_{g-ch}/L_gW_g \cong 4$ μF/cm^2. The advantage over Γ{100} is greater for ballistic transport. A triple- well L[111] design gives similar results. In these FETs, the upper wells charge most strongly because of charge division between the wells' C_{dos} and the well-well capacitance $C_{well} = \varepsilon L_gW_g/T_{pitch}$, where T_{pitch} is the well pitch. With thin wells, and low m_t, C_{dos} can be increased 1.5:1 to 2.2:1.

The designs above use very thin wells and barriers. It must be determined whether such layers can be grown and whether mobility is acceptable. The energy calculations must be refined. 2-4 ML GaSb and InAs wells [8,9] have been grown. Preliminary tightbinding calculations using an sp3d5s* basis [10] conducted for triple 1.1nm GaSb wells with 1.1nm AlSb barriers confirm the symmetry of the lowest state manifold and its expected transverse dispersion. Excited states are slightly lower than predicted by effective mass, but the design still appears viable. Experimental demonstration of such channel designs would enable III-V FETs to provide smaller carrier transit times and larger drive currents than Si MOSFETs even for gate dielectrics with equivalent thickness below 0.5 nm.

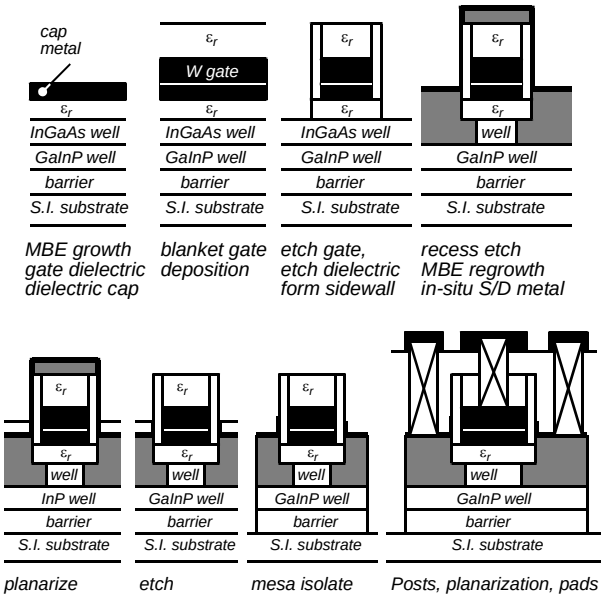


Figure 4: Process flow for III-V FETs with source/drain regrowth by MEE.

IV. Fabrication Processes For nm III-V MOSFETs

Established III-V HEMT structures do not well address scaling requirements of Section II. We have therefore developed a fully self-aligned InGaAs MOSFET process flow [11,12,13,14] (fig. 1). In this flow, 4.7 nm Al_2O_3 gate dielectric is deposited by ALD on a 5 nm $In_{0.53}Ga_{0.47}As$ channel, the gate is formed by blanket W/Cr/ SiO_2 deposition and RIE etching, and thin ~25 nm Si_xN_y gate sidewalls formed. After etching the Al_2O_3, self-aligned S/D InAs N+ regions (50 nm thick, 8×10^{19} cm^{-3}, 23 Ω sheet resistance) are formed by migration enhanced epitaxy, and self-aligned S/D contacts formed by in-situ blanket evaporation of Mo (1-3 $\Omega-\mu m^2$ contact resistance) and a subsequent height-selective etch [15]. Mesa isolation and back-end metal completes the process. Unlike HEMTs, no gate barrier is present in the S/D regions, the source and drain are fully self-aligned to the gate, and carrier densities in the S/D access regions are high ($\sim1.5\times10^{13}cm^{-2}$). Figure 3 shows measured I_D for a 200-nm-L_g device.

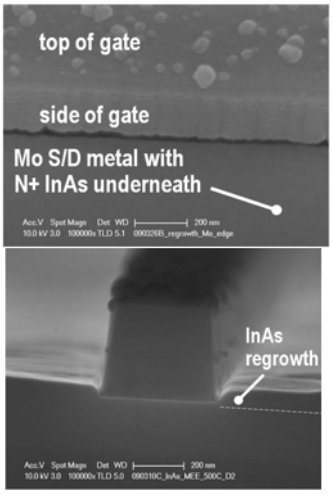


Figure 5: Regrown S/D InGaAs FET, oblique view & cross-section

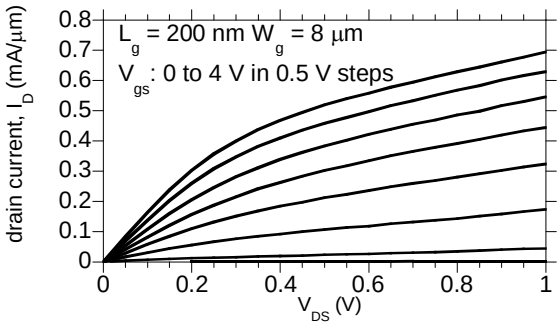


Figure 6: Common-source characteristics, 200 nm FET

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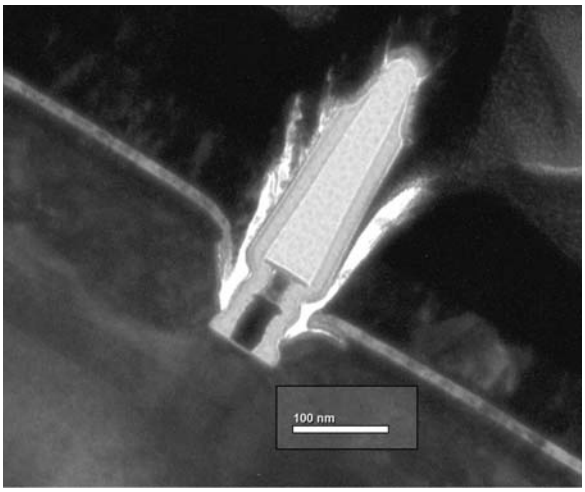

Figure 7: Cross-section of regrown S/D InGaAs FET with a 27 nm gate

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