2010 Conference on Indium Phosphide and Related Materials, June 2-4, Takamatsu, Japan

III-V MOSFETs: Scaling Laws, Scaling Limits,Fabrication Processes

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III-V MOSFETs for VLSI: Why and Why Not.

Lower mass → Higher Carrier Velocity→ lower input capacitance
improved gate delay in transistor-capacitance-limited gates
not relevant in wiring-capacitance-limited gates (i.e. most of VLSI)

More importantly: <u>potential</u> for higher drive current
improved gate delay in wiring-capacitance-limited gates (VLSI)

But this advantage is widely misunderstood in community
InGaAs channels→ higher I_d / W_g than Si only for thick dielectrics
....LOWER I_d / W_g than Si for thin dielectrics
break-even point is at ~0.5 nm EOT

We will introduce later candidate III-V channel designs
providing higher I_d / W_g than Si even for small EOT

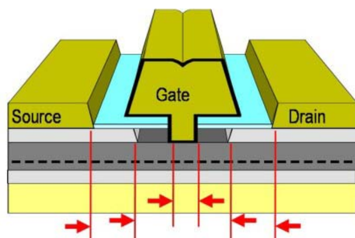
III-V MOS: What is needed ?

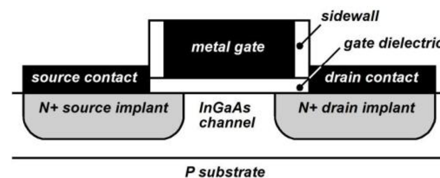
True MOS device structures at ~10 nm gate lengths

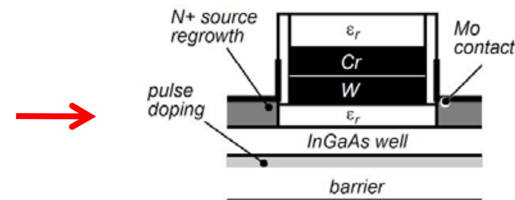
10nm gate length, < 10nm electrode spacings, < 10nm contact widths

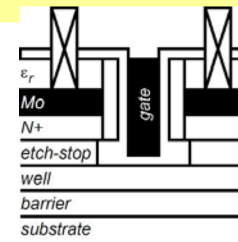
< 3 nm channel, < 1 nm gate-channel separation, < 3nm deep junctions

Fully self-aligned processes: N+ S/D, S/D contacts









Drive currents >> 1 mA/micron @ 1/2-Volt V_{dd}.

Low access resistances.

Density-of-states limits.

Dielectrics: < 0.6 nm EOT , D_{it} < 10^{12} /cm^2-eV

impacts I_{on}, I_{off} , ...

Low dielectric D_{it} must survive FET process.

...and the channel must be grown on Silicon

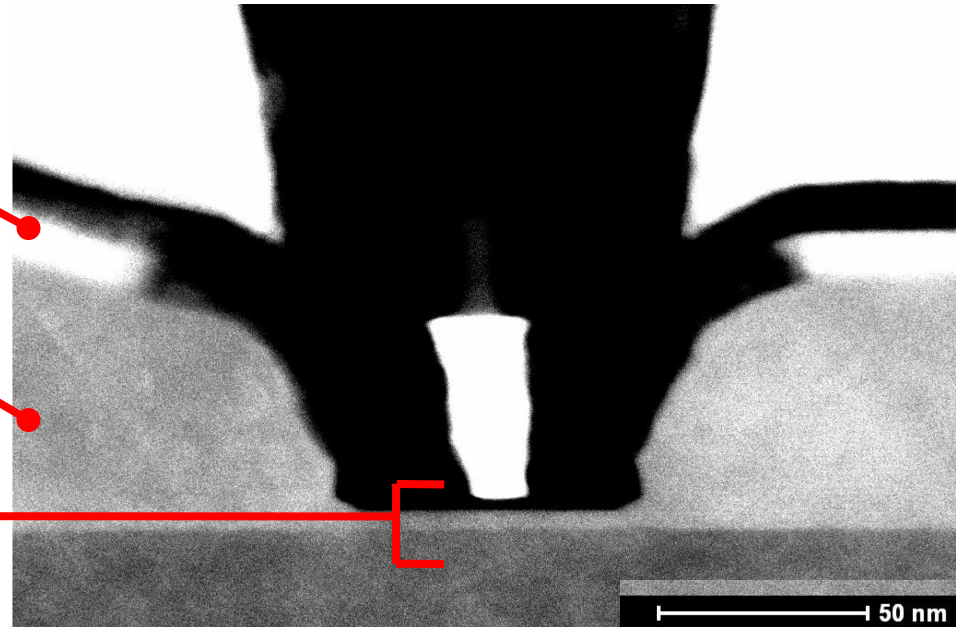
Highly Scaled FET Process Flows

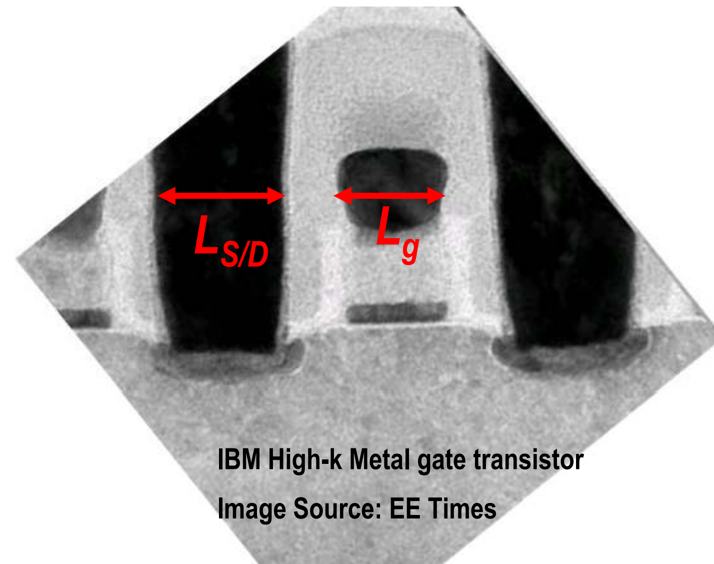
Requirements: 10 nm L_g III-V MOSFET

Self-aligned S/D contacts
low resistance in ~10 nm width,
< 0.5 Ω-μm^2 resistivity needed.

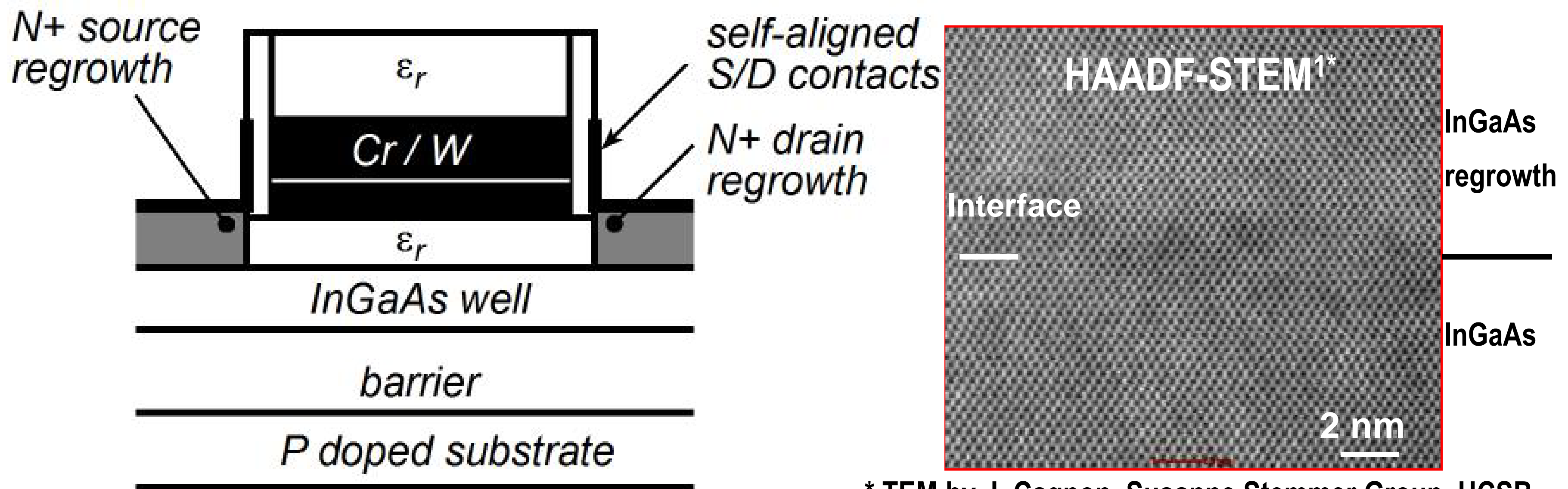
Self-aligned N+ source/drain
shallow, heavily-doped
aligned within nm of gate

Thin oxide < 1 nm EOT
Thin channel < 5nm
Shallow channel: no setbacks





InGaAs MOSFET with N+ Source/Drain by MEE Regrowth[1]



* TEM by J. Cagnon, Susanne Stemmer Group, UCSB

Self-aligned source/drain defined by MBE regrowth[2]

Self-aligned in-situ Mo contacts[3]

Process flow & dimensions selected for 10-30 nm L_g design;

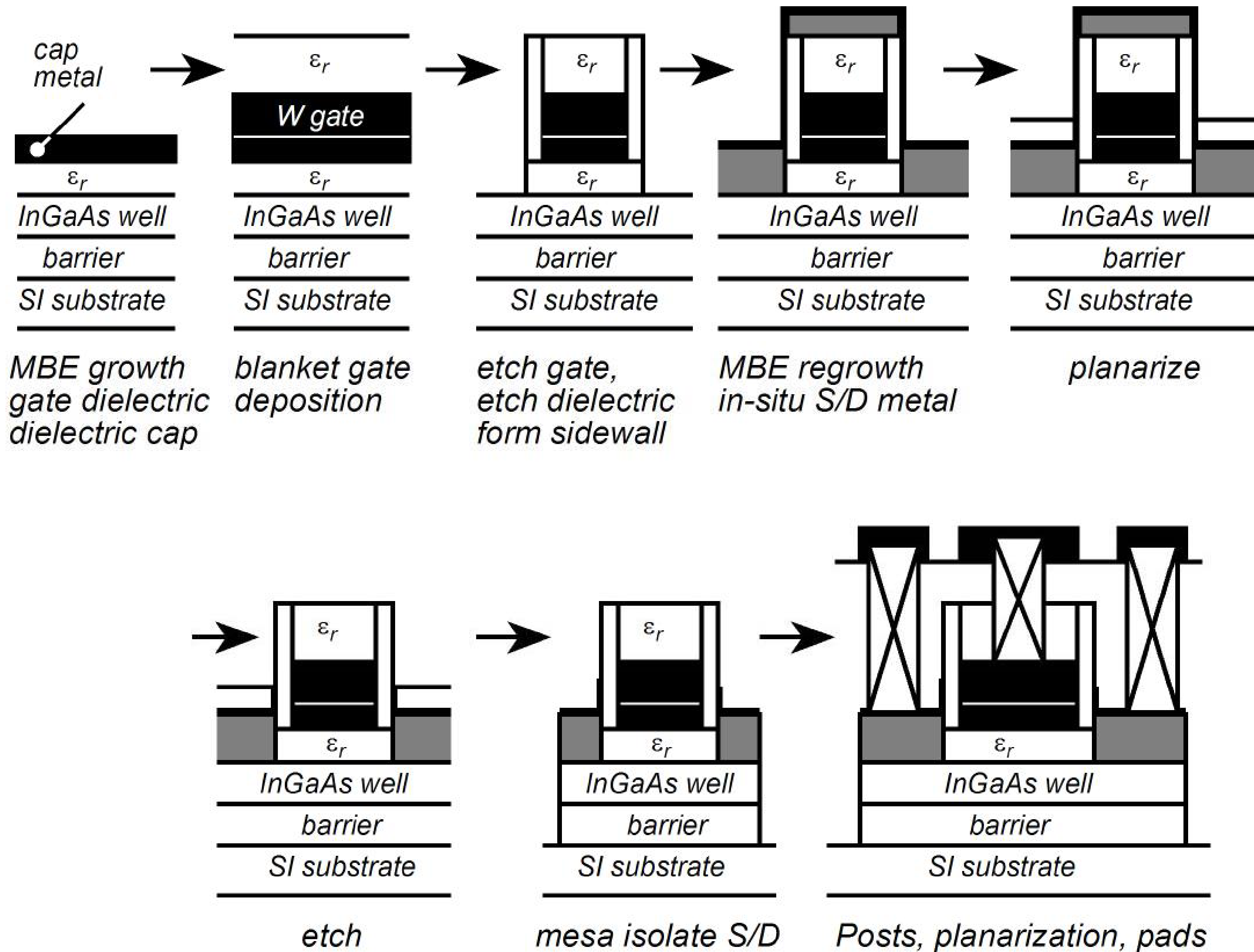
Gate-first

gate dielectric formed after MBE growth
uncontaminated / undamaged surface

[1]Singisetti, ISCS 2008
[2]Wistey, EMC 2008
[3]Baraskar, EMC 2009

Process flow*

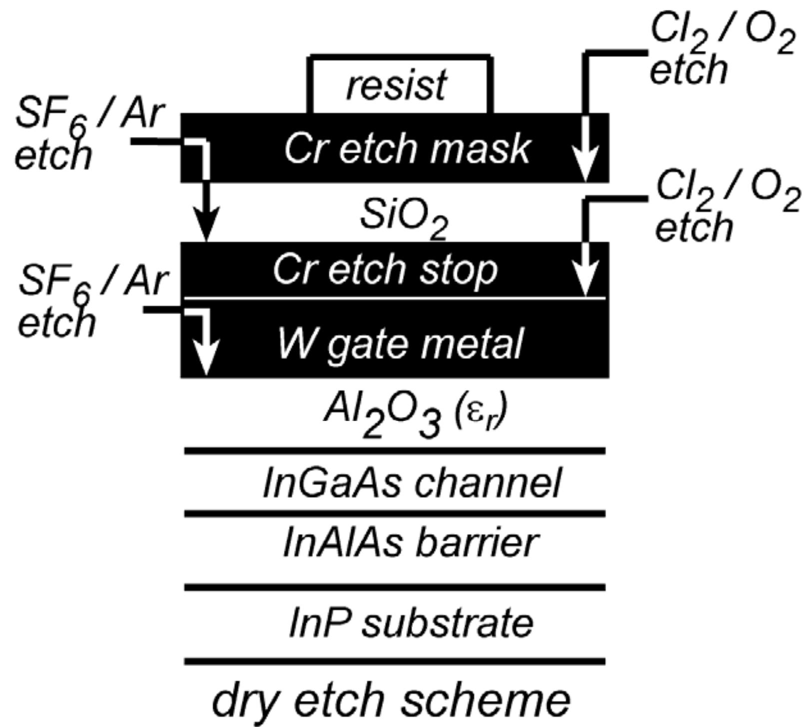
* Singisetti et al, 2008 ISCS, September, Frieburg
Singisetti *et al*, Physica Status Solidi C, vol. 6, pp. 1394,2009

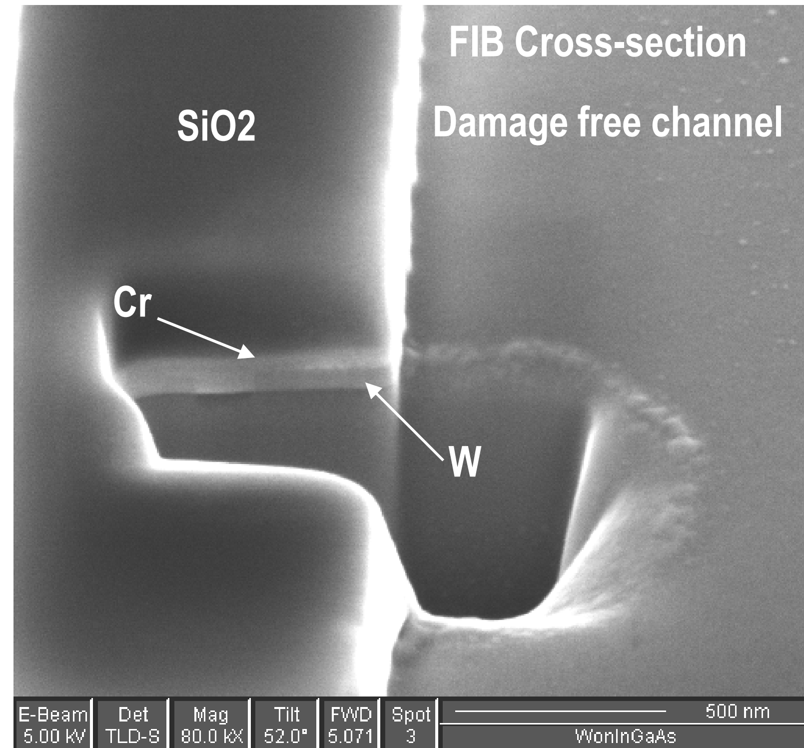


Key challenge in S/D process: gate stack etch

Requirement: avoid damaging semiconductor surface:

Approach: Gate stack with multiple selective etches*

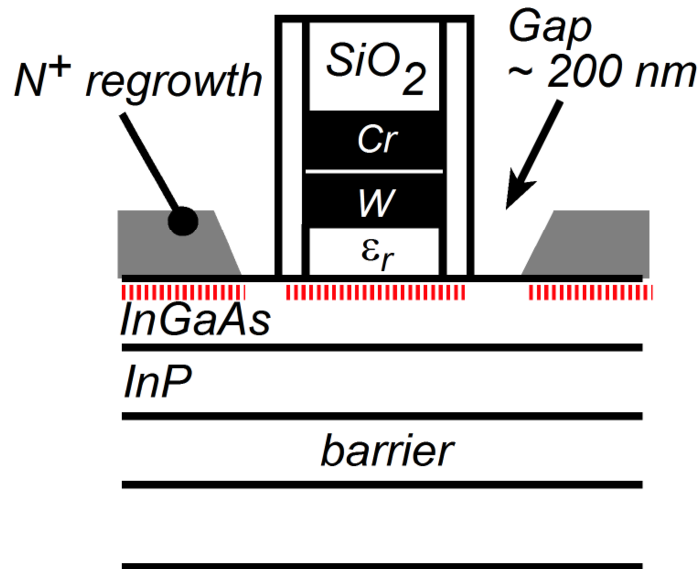


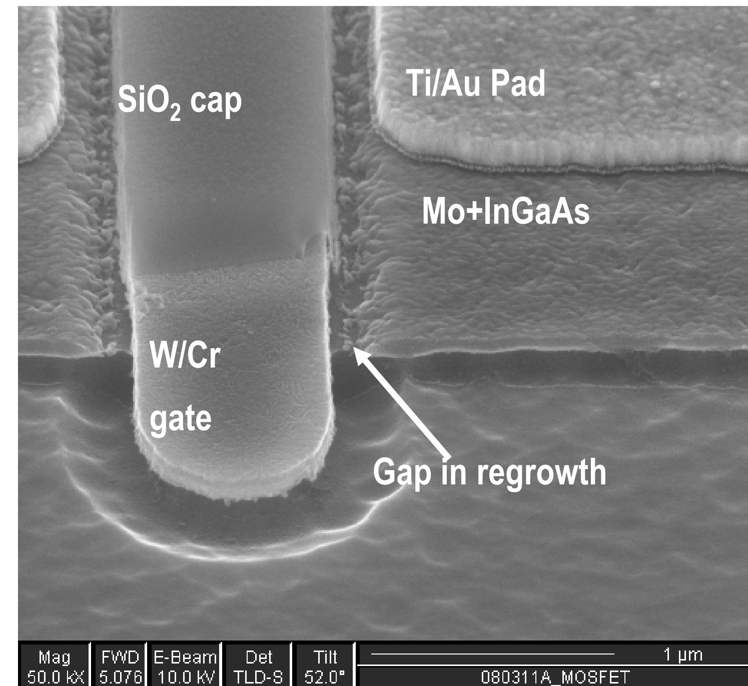


Process scalable to ~10 nm gate lengths

* Singisetti *et al*; Physica Status Solidi C, vol. 6, pp. 1394,2009

MBE Regrowth→ Gap Near Gate→ Source Resistance





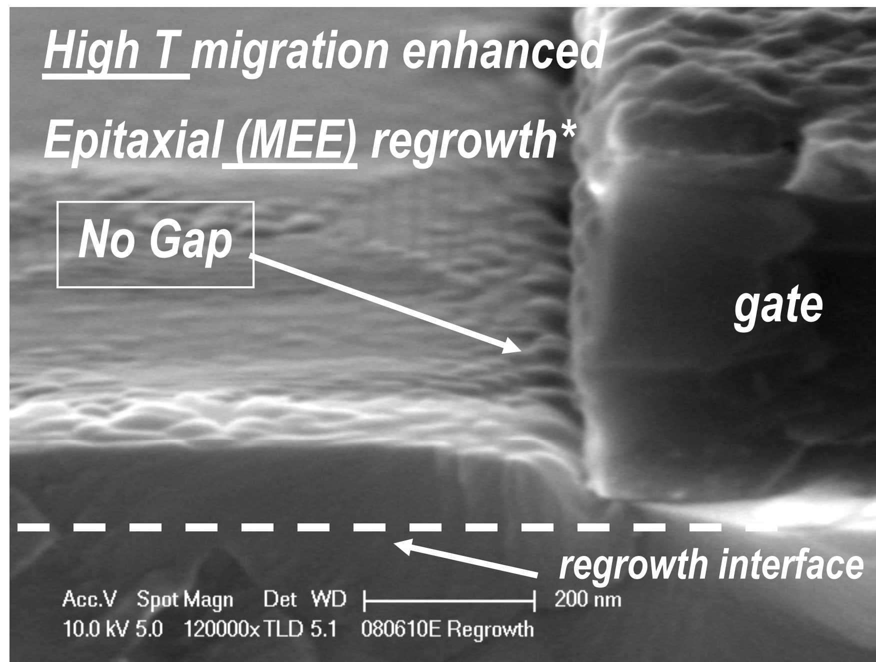
- *Shadowing by gate: No regrowth next to gate*

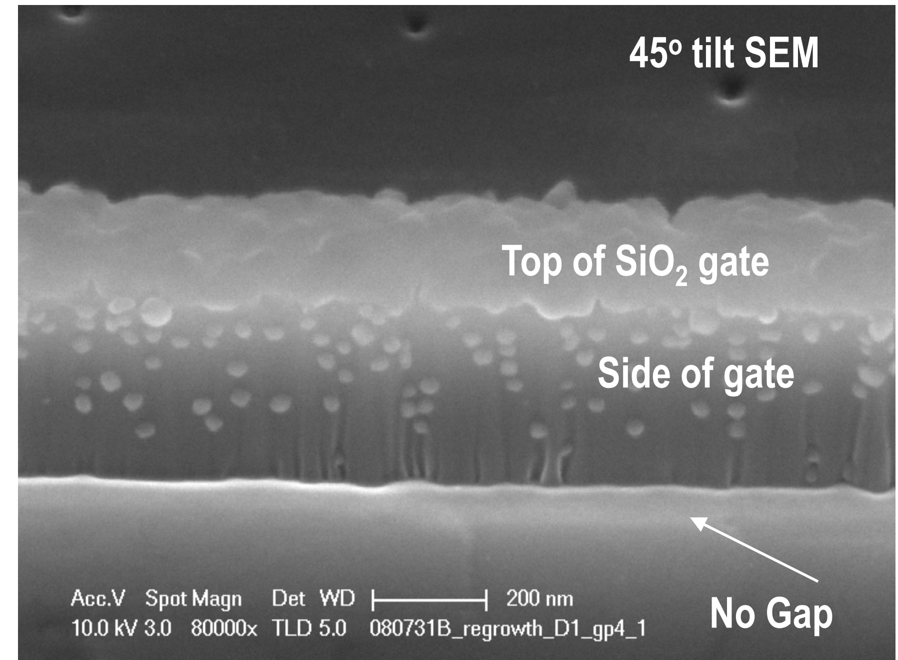
- *Gap region is depleted of electrons*

High source resistance because of electron depletion in the gap

MBE growth by Dr. Mark Wistey, device fabrication and characterization by U. Singisetti

Migration Enhanced Epitaxial (MEE) S/D Regrowth*





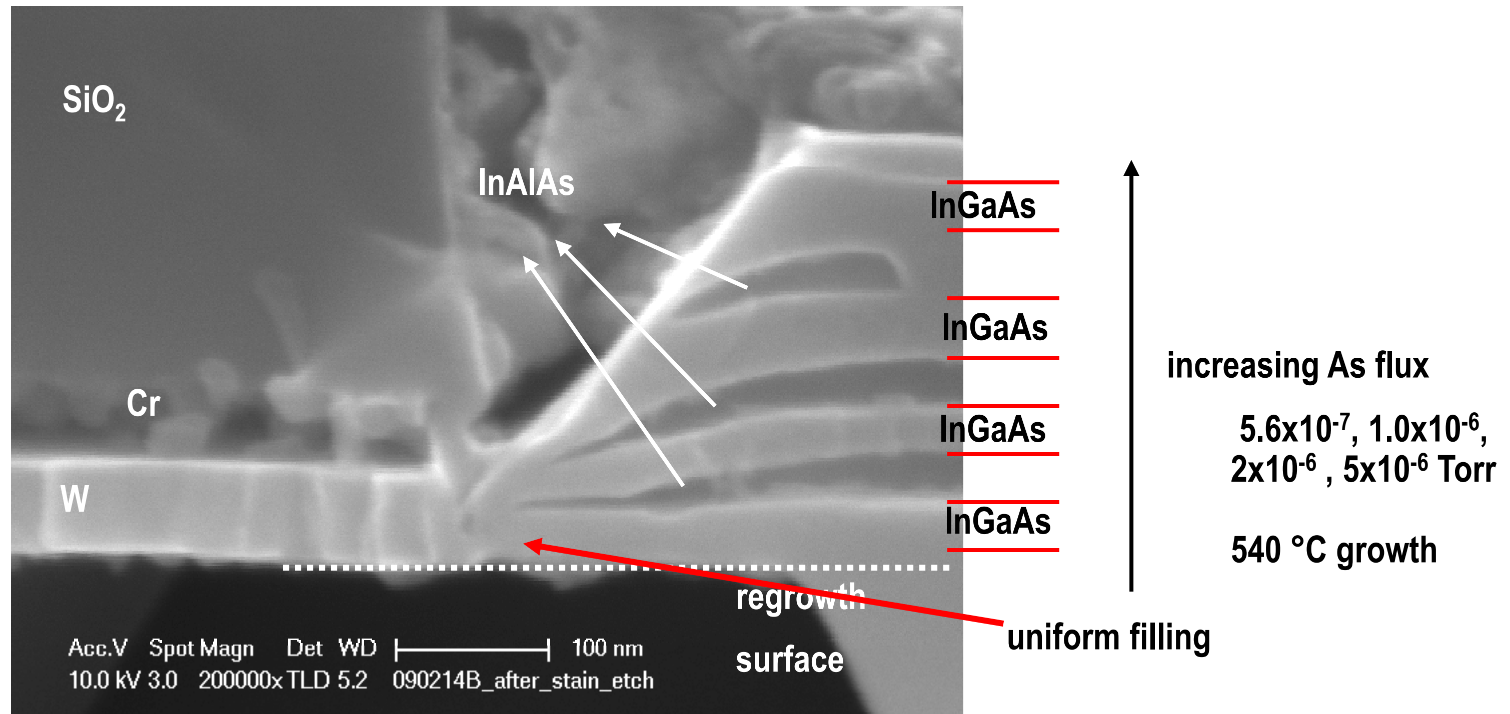
High temperature migration enhanced epitaxial regrowth

*Wistey, EMC 2008

Wistey, ICMBE 2008

MBE growth by Dr. Mark Wistey, device fabrication and characterization by U. Singisetti

Regrowth profile dependence on As flux*



multiple InGaAs regrowths with InAlAs marker layers

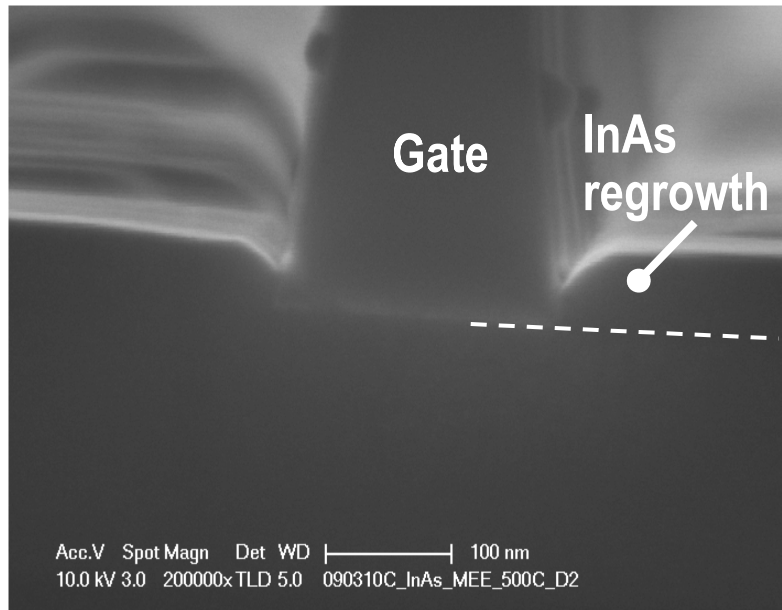
Uniform filling with lower As flux

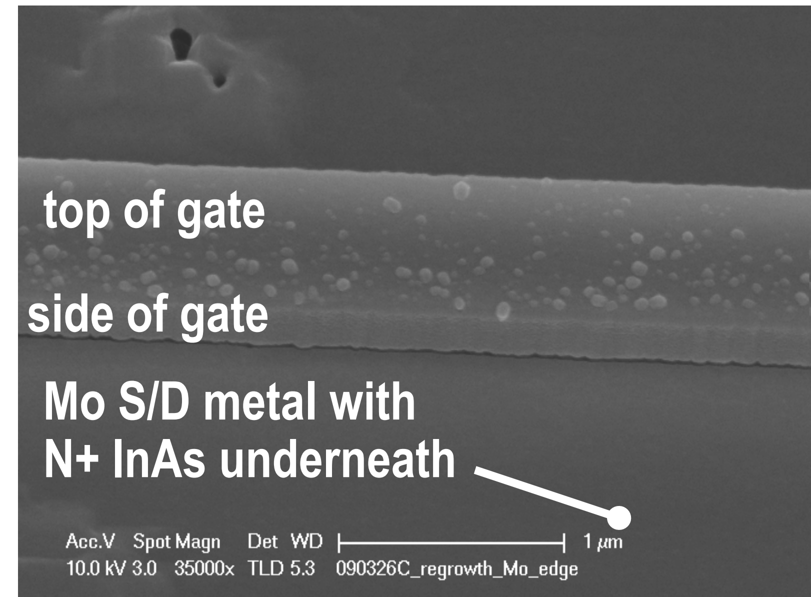
* Wistey *et al*, EMC 2009

Wistey *et al* NAMBE 2009

MBE growth by Dr. Mark Wistey, device fabrication and characterization by U. Singisetti

InAs source/drain regrowth





Improved InAs regrowth with low As flux for uniform filling[1]

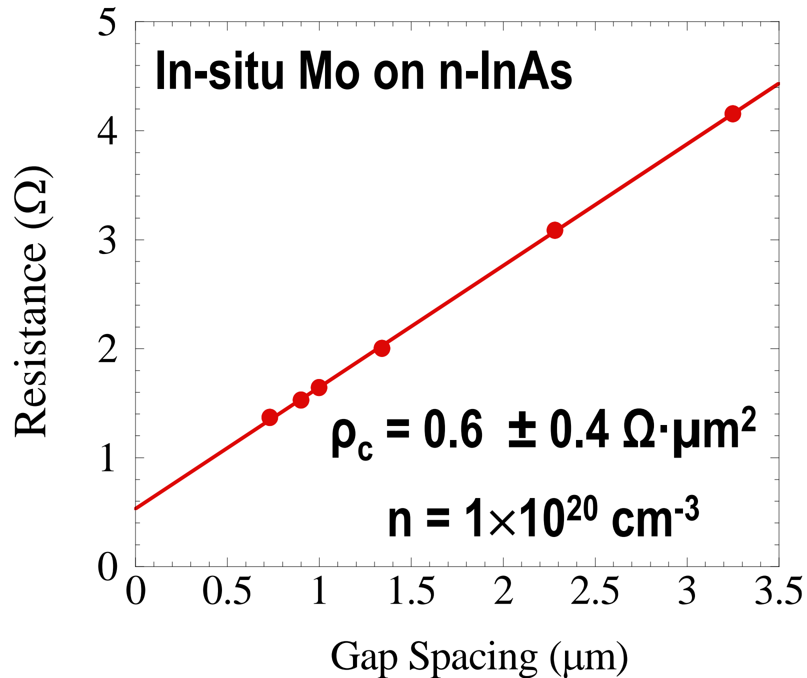
InAs less susceptible to electron depletion: Fermi pinning above E_c[2]

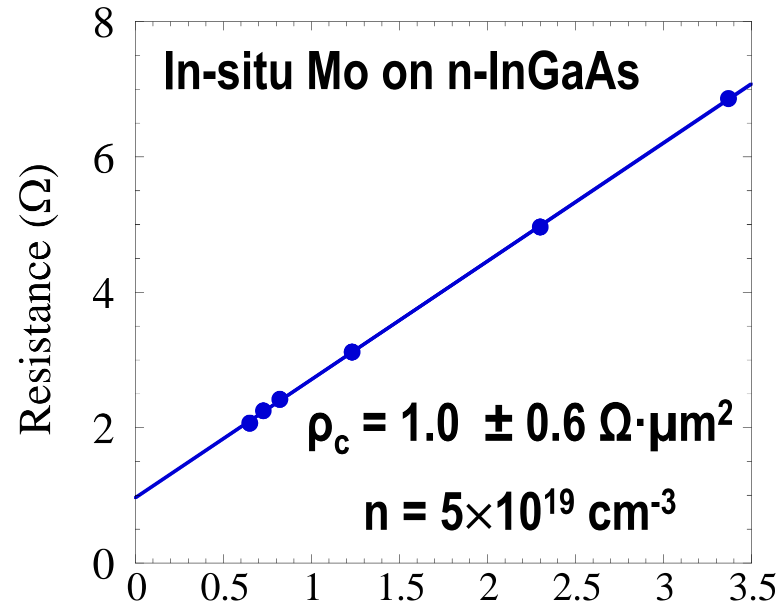
[1] Wistey *et al*, EMC 2009

Wistey *et al* NAMBE 2009.

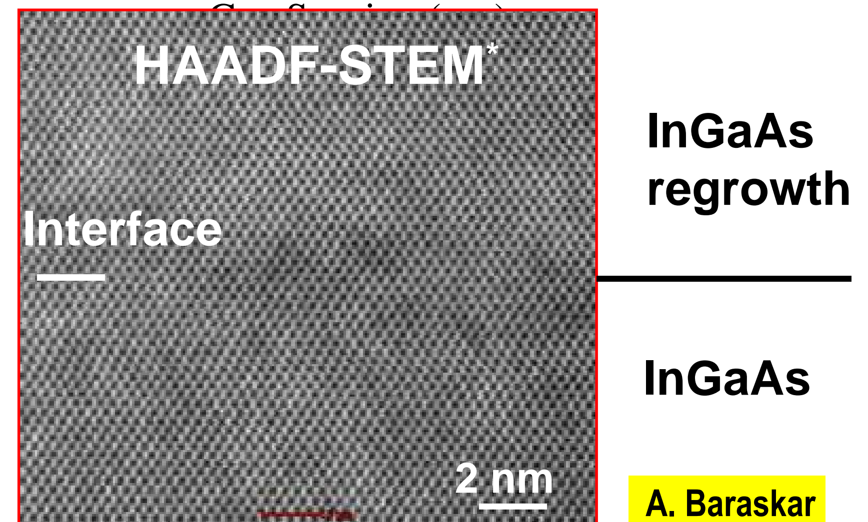
[2]Bhargava *et al* , APL 1997

In-Situ Refractory Ohmics on MBE Regrown N-InGaAs





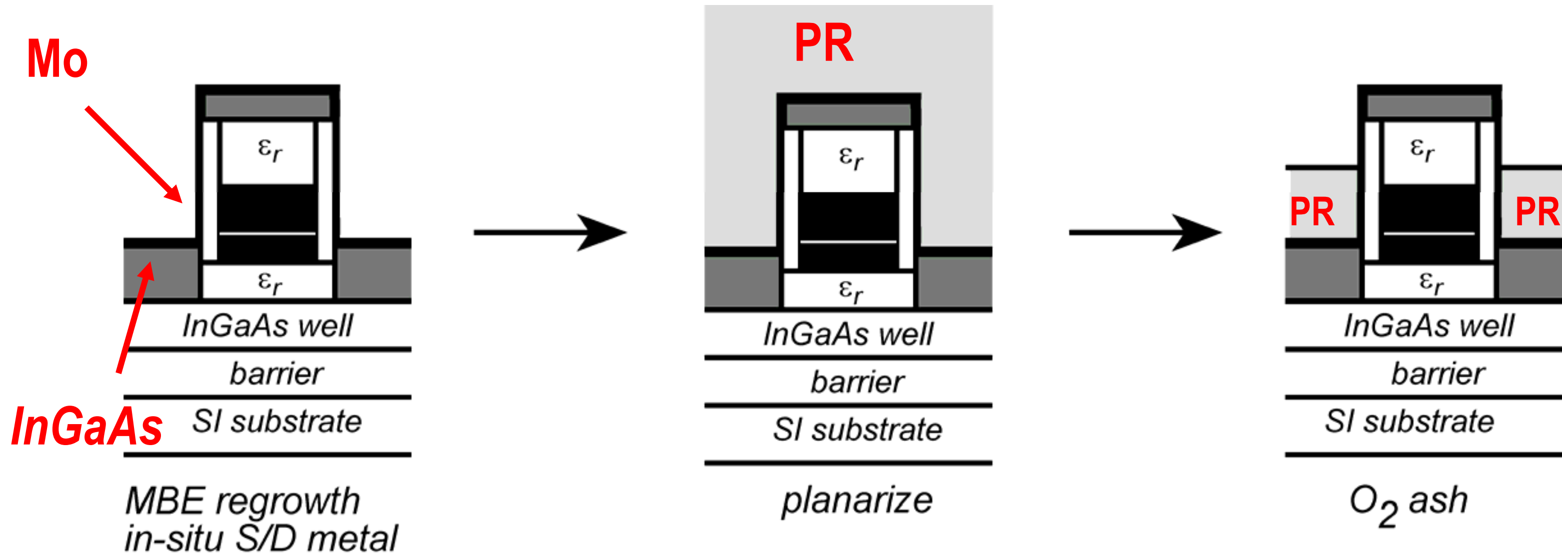
Contact resistivity to MEE regrown material is ~1.2 Ω-μm^2.

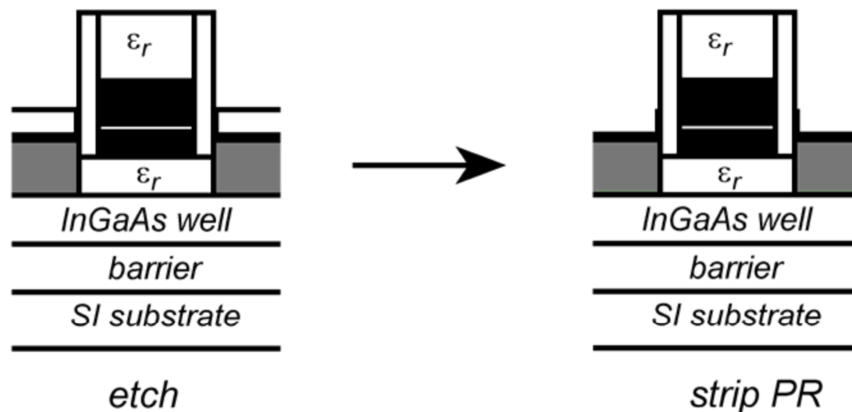


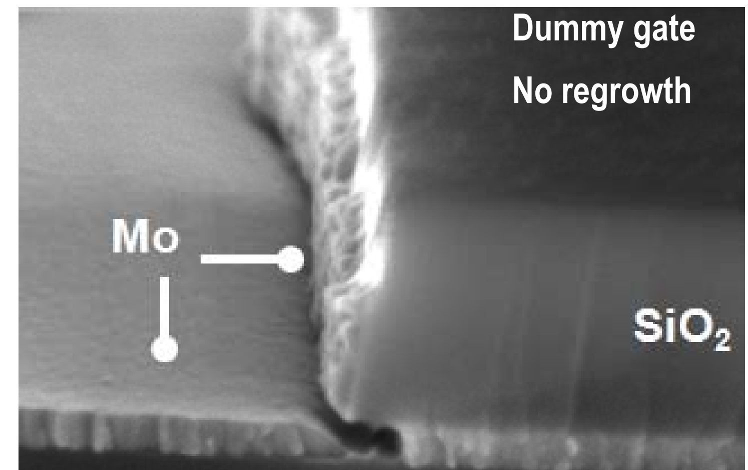
A. Baraskar

TEM by Dr. J. Cagnon, Stemmer Group, UCSB

Self-Aligned Contacts: Height Selective Etching*

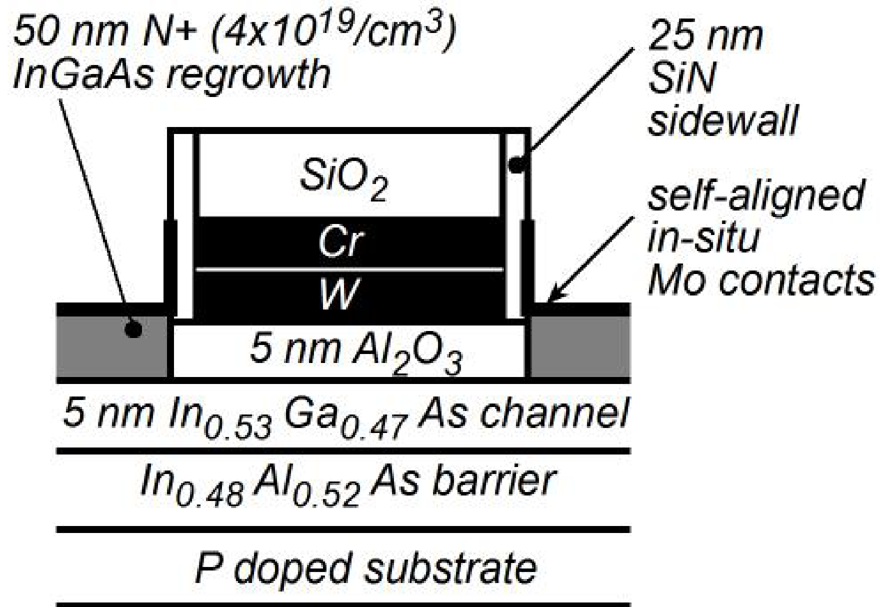


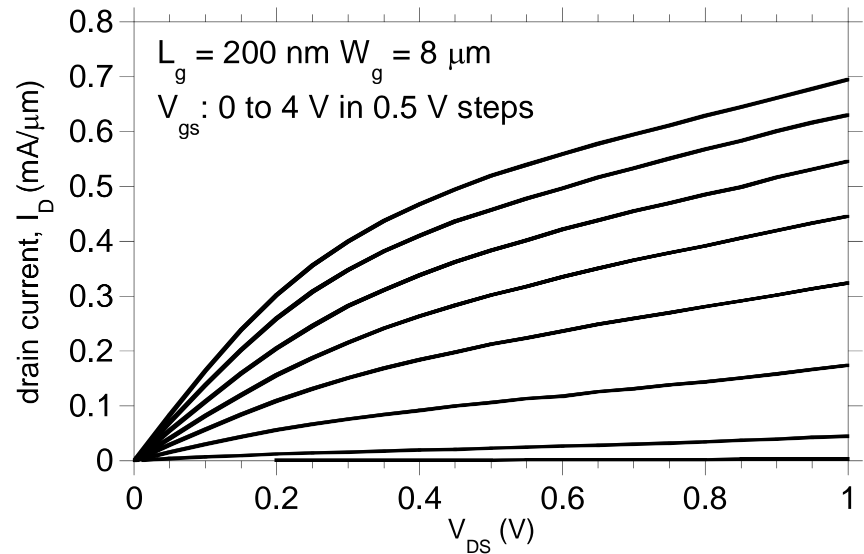


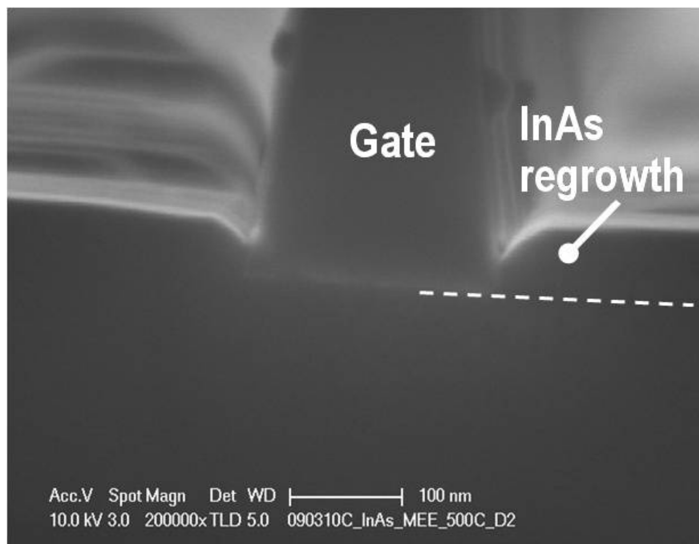


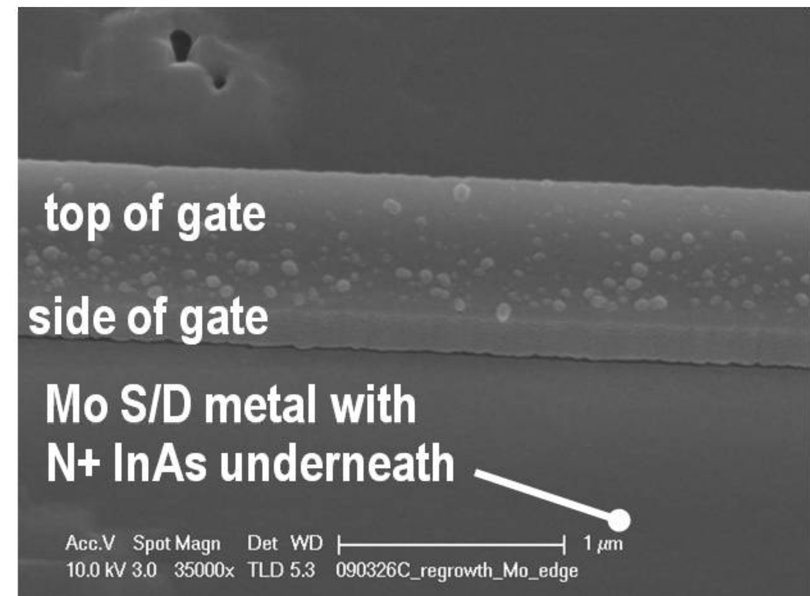
* Burek *et al*, J. Cryst. Growth 2009

Fully Self-Aligned III-V MOSFET Process

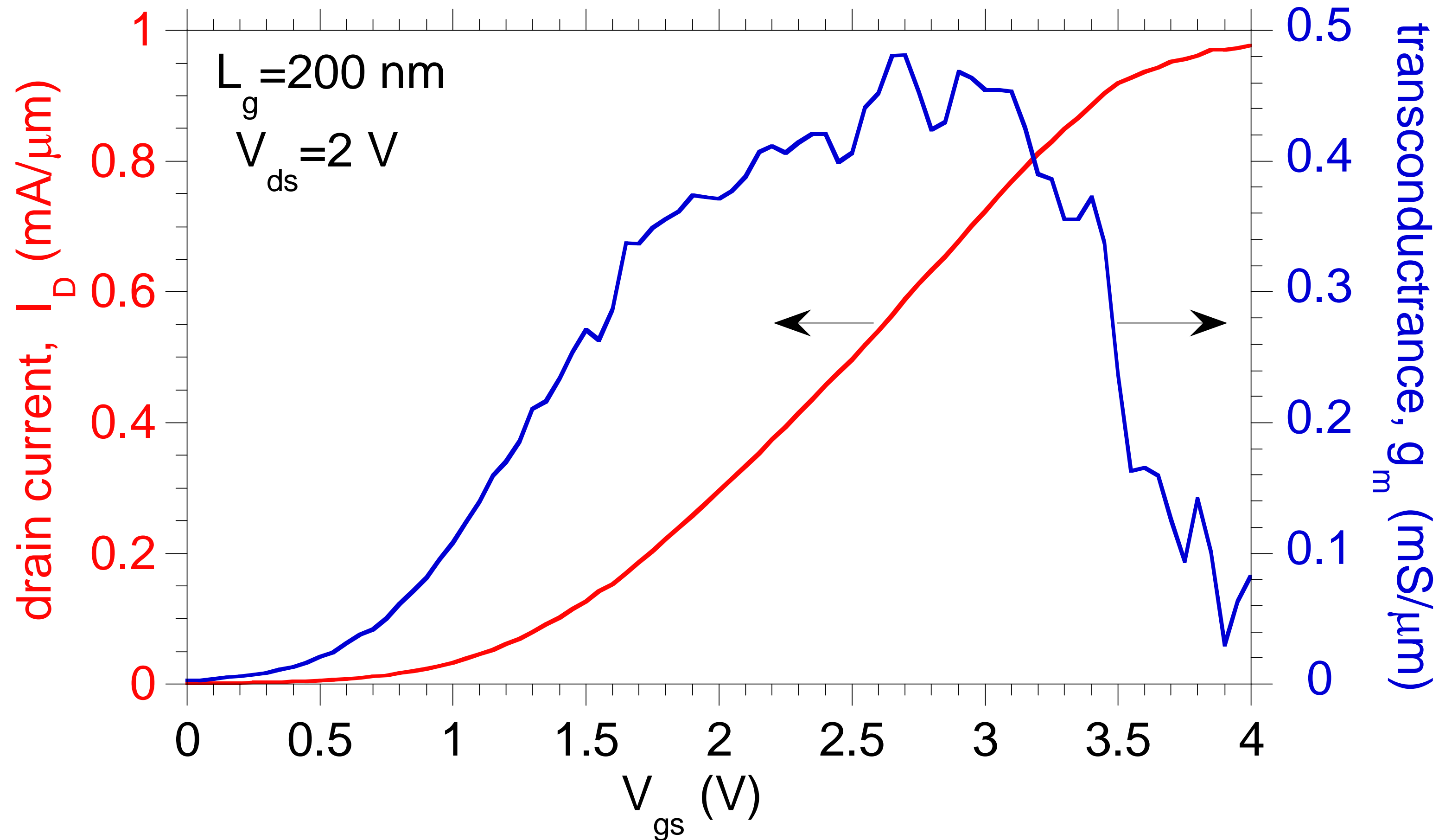








Drive current and transconductance

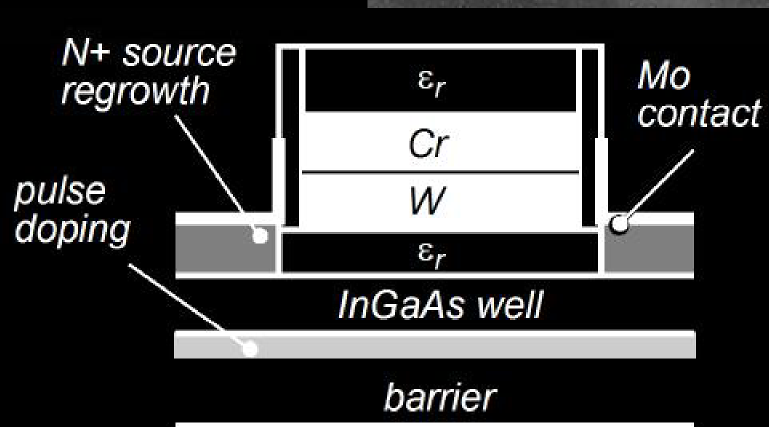


0.95 mA/µm peak I_d , ~0.45 mS/µm peak g_m

27 nm Self-Aligned Process Flow

Self-aligned structures at ~10 nm gate length can be fabricated

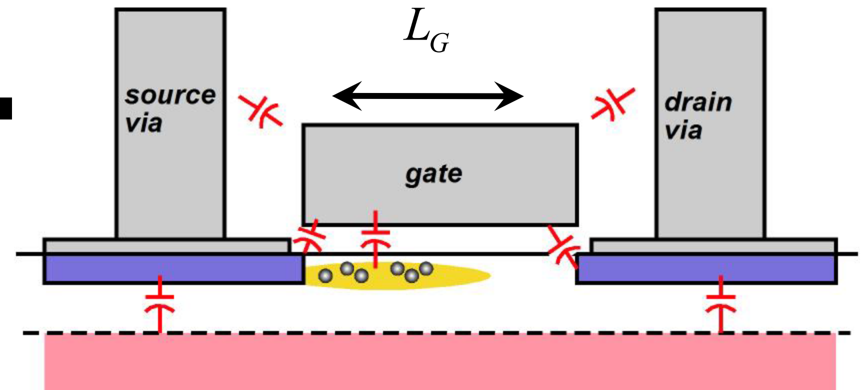
MEE regrowth has very narrow process window→ CBE or MOCVD ?



III-V FET Scaling & High-Current-Density Channels

FET Scaling Laws

Changes required to double device / circuit bandwidth.



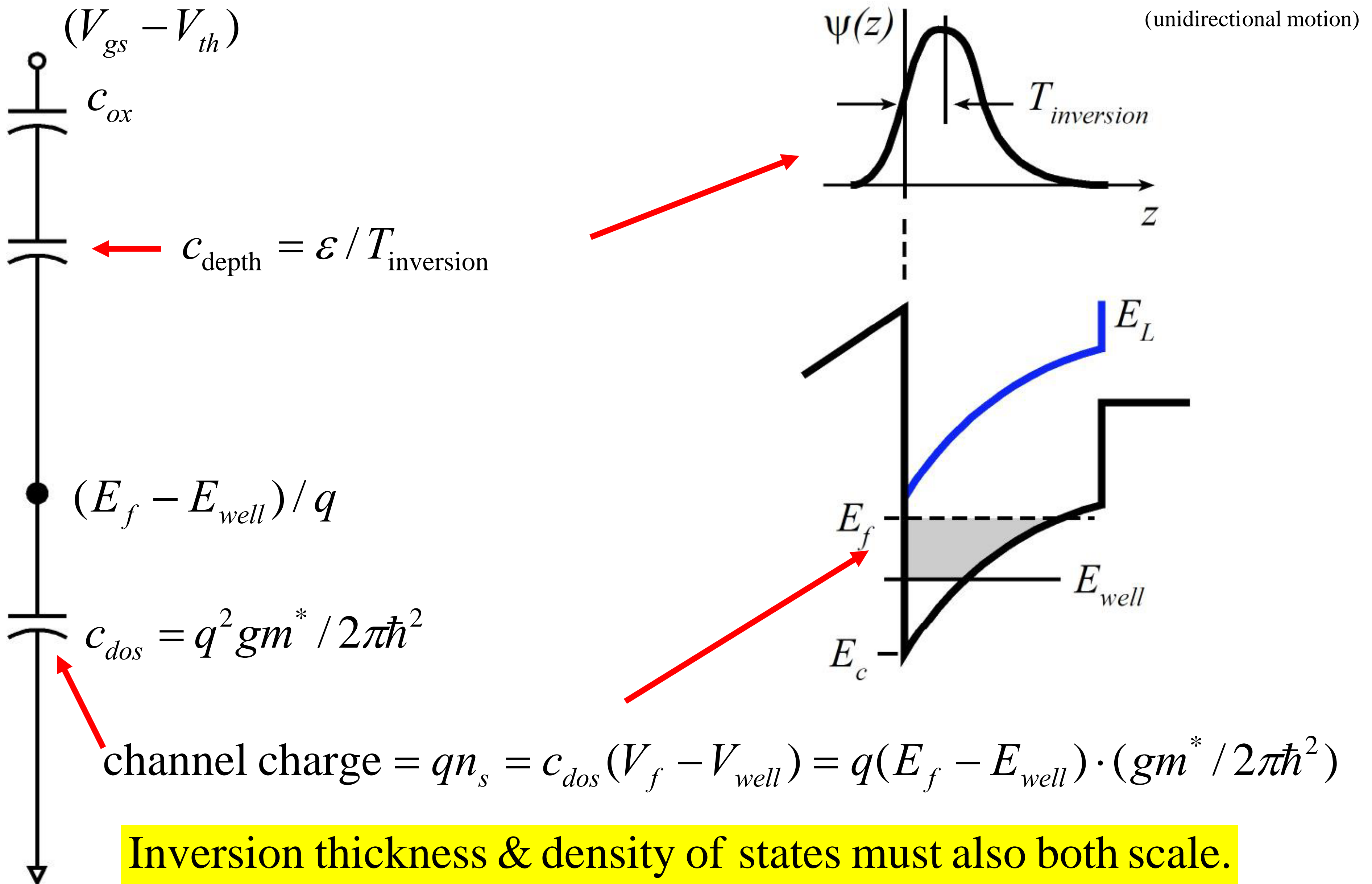
$(\text{gate width } W_G)$

laws in constant-voltage limit:

FET parameter	change
gate length	decrease 2:1
current density (mA/μm), g_m (mS/μm)	increase 2:1
channel 2DEG electron density	increase 2:1
electron mass in transport direction	constant
gate-channel capacitance density	increase 2:1
dielectric equivalent thickness	decrease 2:1
channel thickness	decrease 2:1
channel density of states	increase 2:1
source & drain contact resistivities	decrease 4:1

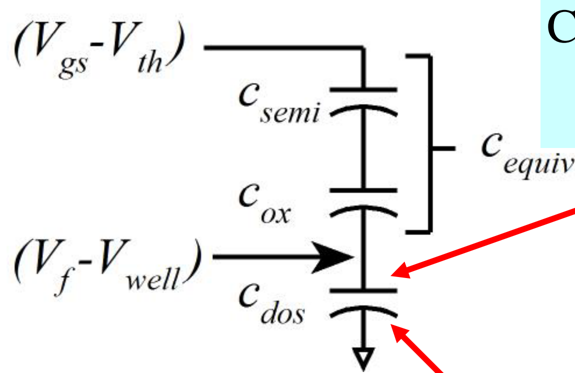
Current densities should double
Charge densities must double

Semiconductor Capacitances Must Also Scale



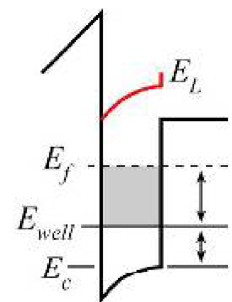
Inversion thickness & density of states must also both scale.

Calculating Current: Ballistic Limit



Channel Fermi voltage = voltage applied to c_{dos}

determines Fermi velocity v_f through $E_f = qV_f = m^* v_f^2 / 2$



mean electron velocity $= \bar{v} = (4/3\pi) v_f$

Channel charge : $\rho_s = c_{dos}\left(V_f - V_c\right) = \dfrac{c_{dos} c_{equiv}}{c_{equiv} + c_{dos}}\left(V_{gs} - V_{th}\right)$

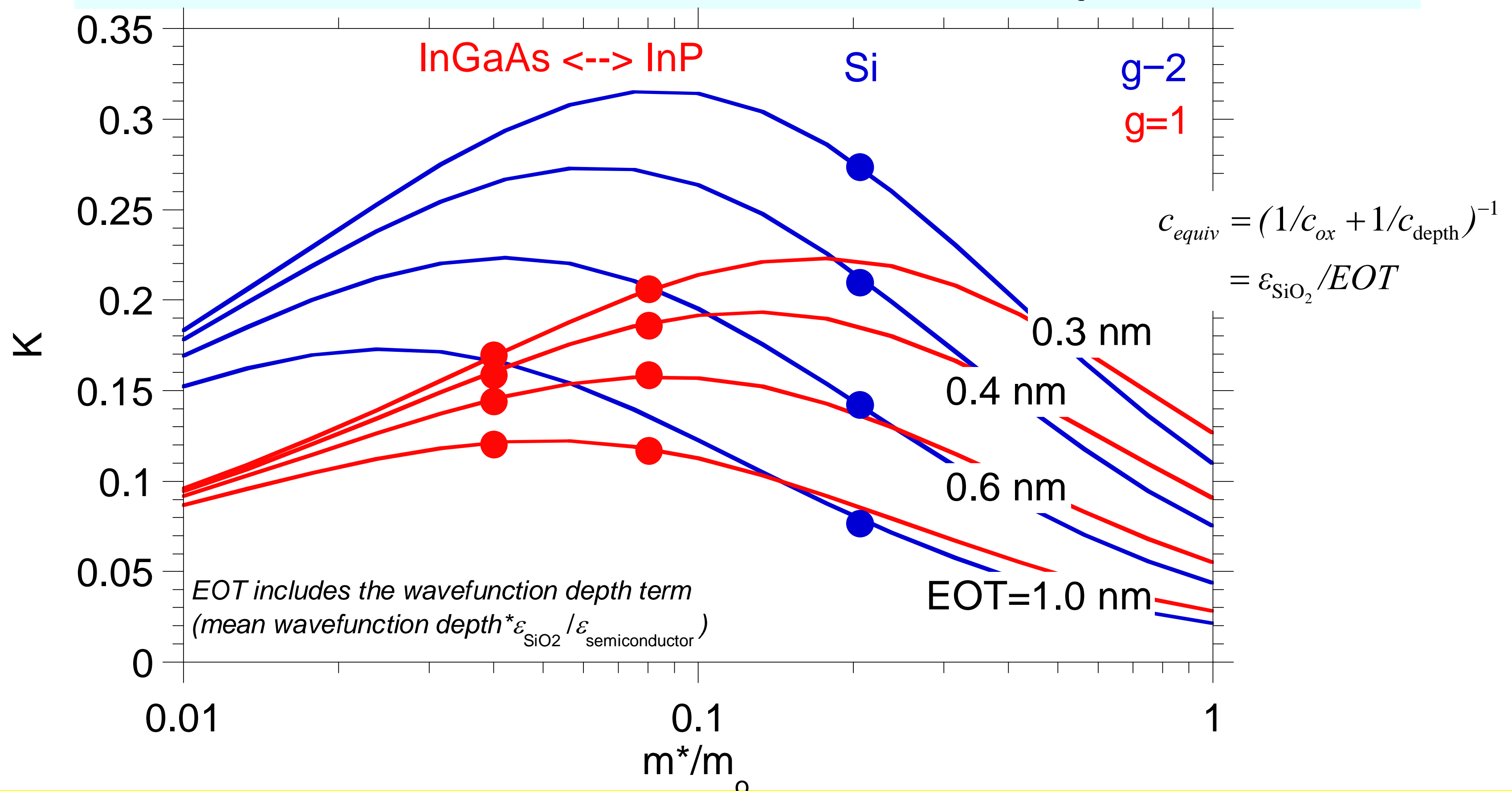
$c_{dos} = q^2 g m^* / 2\pi\hbar^2 = c_{dos,o} \cdot g \cdot (m^*/m_o)$, where g is the # of band minima

$$\Rightarrow \quad J = \left(84 \frac{\text{mA}}{\mu\text{m}}\right) \frac{g \cdot (m^*/m_o)^{1/2}}{\left(1 + (c_{dos,o}/c_{ox}) \cdot g \cdot (m^*/m_o)\right)^{3/2}} \left(\frac{V_{gs} - V_{th}}{1\,\text{V}}\right)^{3/2}$$

Do we get highest current with high or low mass ?

Drive Current Versus Mass, # Valleys, and EOT

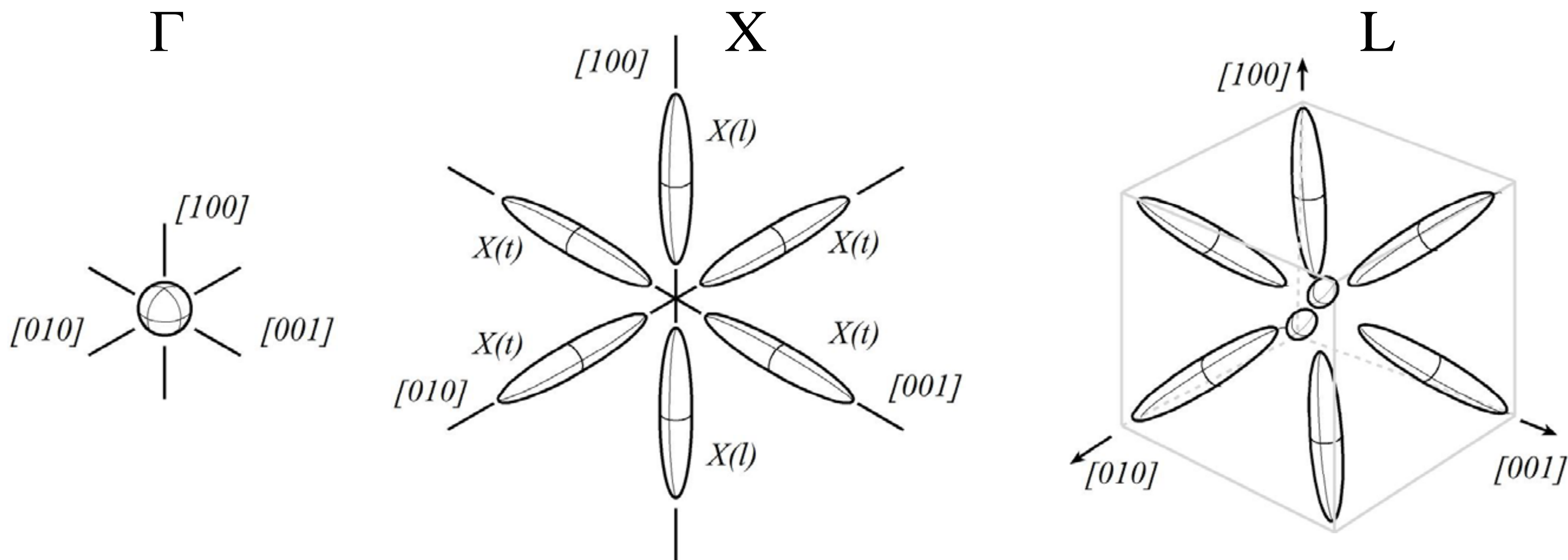
$$J = \underline{K} \cdot \left(84 \frac{\text{mA}}{\mu\text{m}} \right) \cdot \left(\frac{V_{gs} - V_{th}}{1\,\text{V}} \right)^{3/2} , \quad \text{where } \underline{K} = \frac{g \cdot \left(m^*/m_o \right)^{1/2}}{\left(1 + (c_{dos,o}/c_{equiv}) \cdot g \cdot (m^*/m_o) \right)^{3/2}}$$



Standard InGaAs MOSFETs have superior I_d to Si at large EOT.
Standard InGaAs MOSFETs have <u>inferior</u> I_d to Si at <u>small</u> EOT.

Solomon / Laux Density-of-States-Blottleneck → <u>III-V loses to Si.</u>

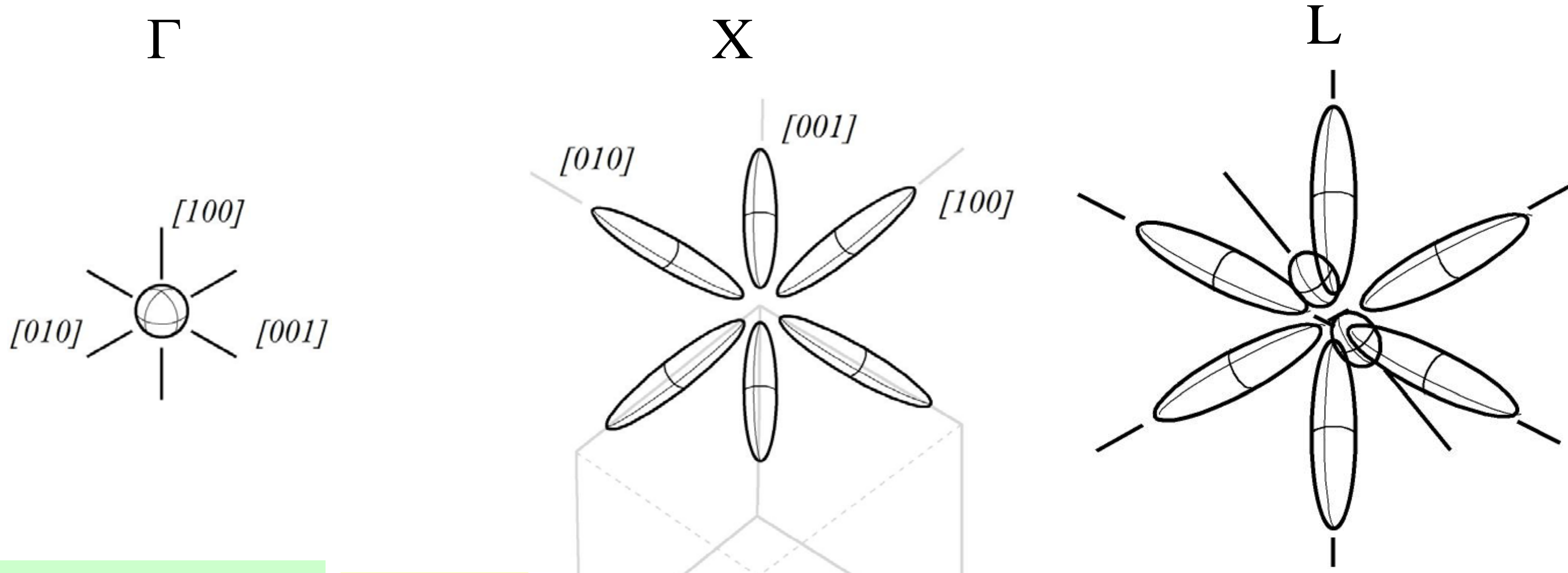
III-V Band Properties, normal {100} Wafer



material	substrate	Γ valley	X valley			L valley		
		m^*/m_o	m_l/m_o	m_t/m_o	$E_x - E_\Gamma$	m_l/m_o	m_t/m_o	$E_L - E_\Gamma$
$In_{0.5}Ga_{0.5}As$	InP	0.045	1.29	0.19	0.83 eV	1.23	0.062	0.47 eV
InAs	InP	0.026	1.13	0.16	0.87 eV	0.65	0.050	0.57 eV
GaAs	GaAs	0.067	1.30	0.22	0.47 eV	1.90	0.075	0.28 eV
Si	Si	---	0.92	0.19	(negative)			

L - valley transverse masses are comparable to Γ valleys

Consider Instead: Valleys in {111} Wafer

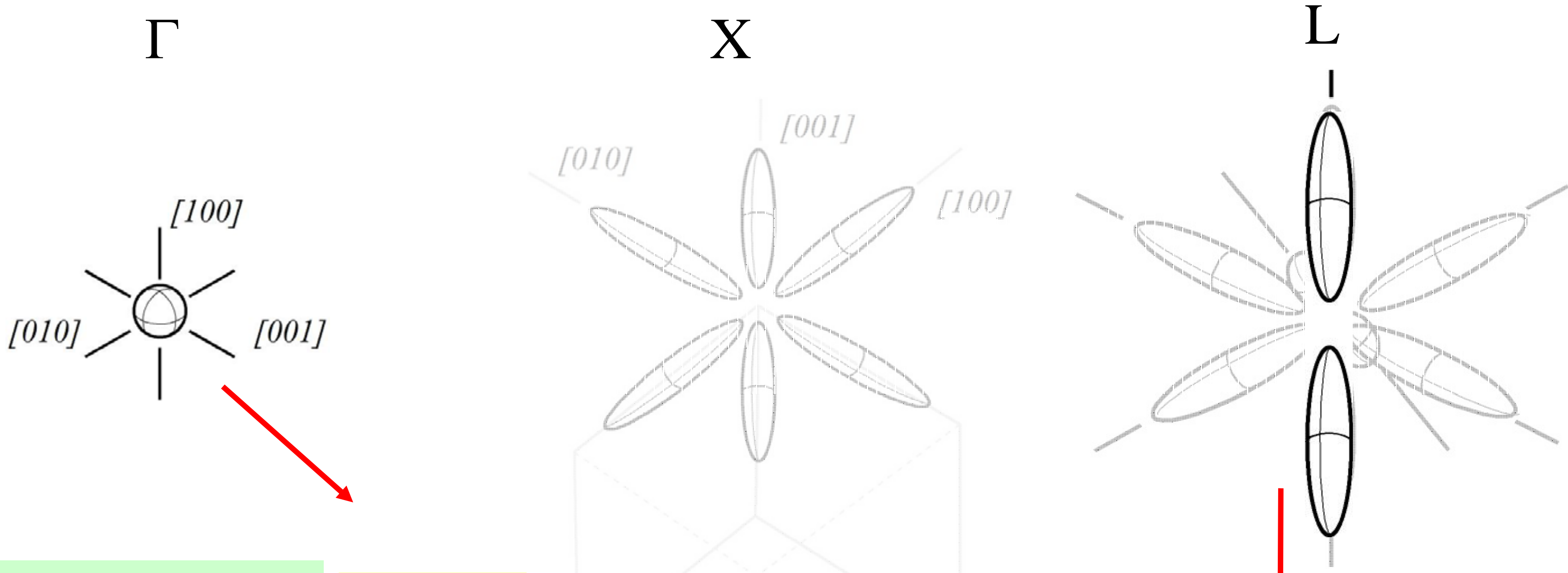


material	substrate	Γ valley m^*/m_o	X valley m_l/m_o	X valley m_t/m_o	X valley $E_x - E_\Gamma$	L valley m_l/m_o	L valley m_t/m_o	L valley $E_L - E_\Gamma$
$In_{0.5}Ga_{0.5}As$	InP	0.045	1.29	0.19	0.83 eV	1.23	0.062	0.47 eV
InAs	InP	0.026	1.13	0.16	0.87 eV	0.65	0.050	0.57 eV
GaAs	GaAs	0.067	1.30	0.22	0.47 eV	1.90	0.075	0.28 eV
Si	Si	---	0.92	0.19	(negative)			

Orientation : one L valley has high vertical mass

X valleys & three L valleys have moderate vertical mass

Valley in {111} Wafer: with Quantization in thin wells



material	substrate	Γ valley m^*/m_o	X valley m_l/m_o	m_t/m_o	$E_x - E_\Gamma$	L valley m_l/m_o	m_t/m_o	$E_L - E_\Gamma$
$In_{0.5}Ga_{0.5}As$	InP	0.045	1.29	0.19	0.83 eV	1.23	0.062	0.47 eV
InAs	InP	0.026	1.13	0.16	0.87 eV	0.65	0.050	0.57 eV
GaAs	GaAs	0.067	1.30	0.22	0.47 eV	1.90	0.075	0.28 eV
Si	Si	- - -	0.92	0.19	(negative)			

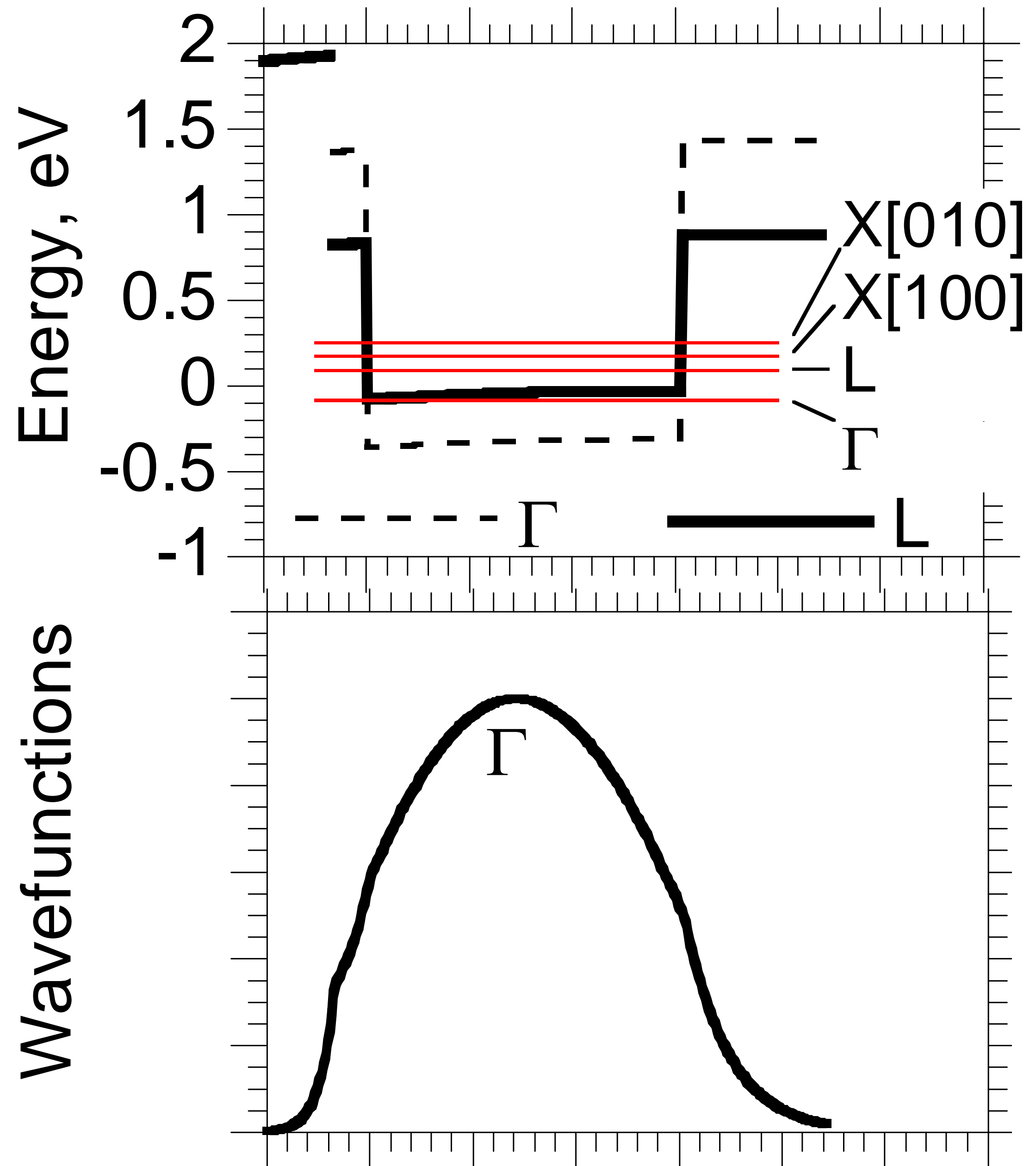
Selects L[111] valley; low transverse mass

{111} Γ-L FET: Candidate Channel Materials

material	Γ valley	L valley			Well thickness for
	m^* / m_o	m_l / m_o	m_t / m_o	$E_L - E_\Gamma$	$\Gamma - \mathrm{L}$ alignment
$In_{0.5}Ga_{0.5}As$	0.045	1.23	0.062	0.47 eV	1 nm (?)
GaAs	0.067	1.90	0.075	0.28 eV	2 nm
GaSb	0.039	1.30	0.10	0.07 eV	4 nm

Standard Approach Γ valleys in [100] orientation

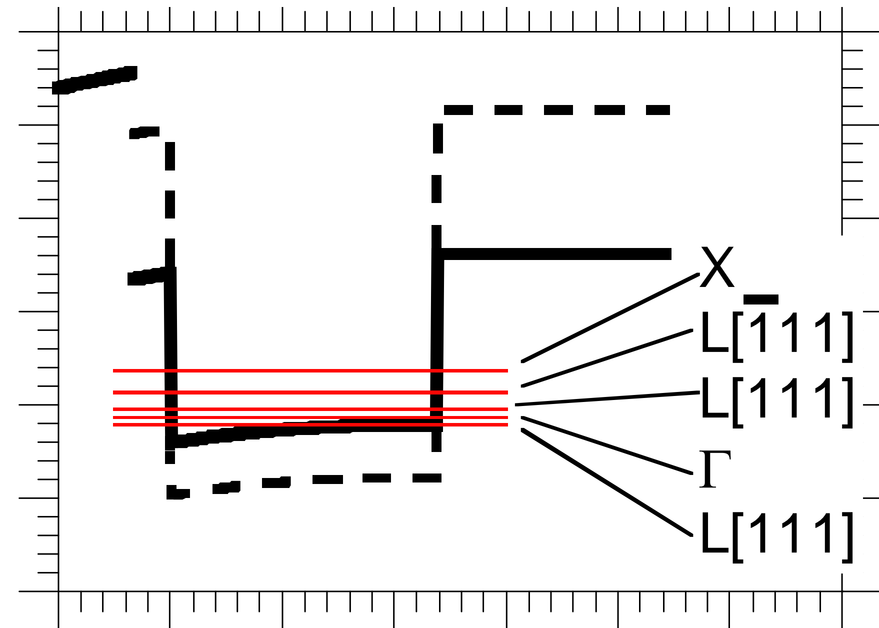
3 nm GaAs well
AlSb barriers



Relative Energies:
Γ=0 eV
L=177 meV
X[100]= 264 meV
X[010] = 337 meV

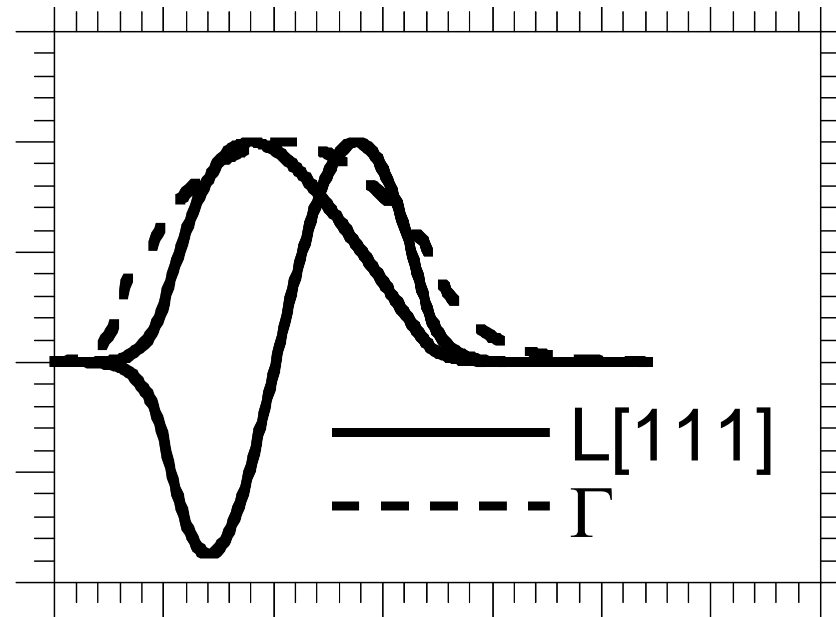
First Approach: Use both Γ and L valleys in [111]

2.3 nm GaAs well
AlSb barriers
[111] orientation



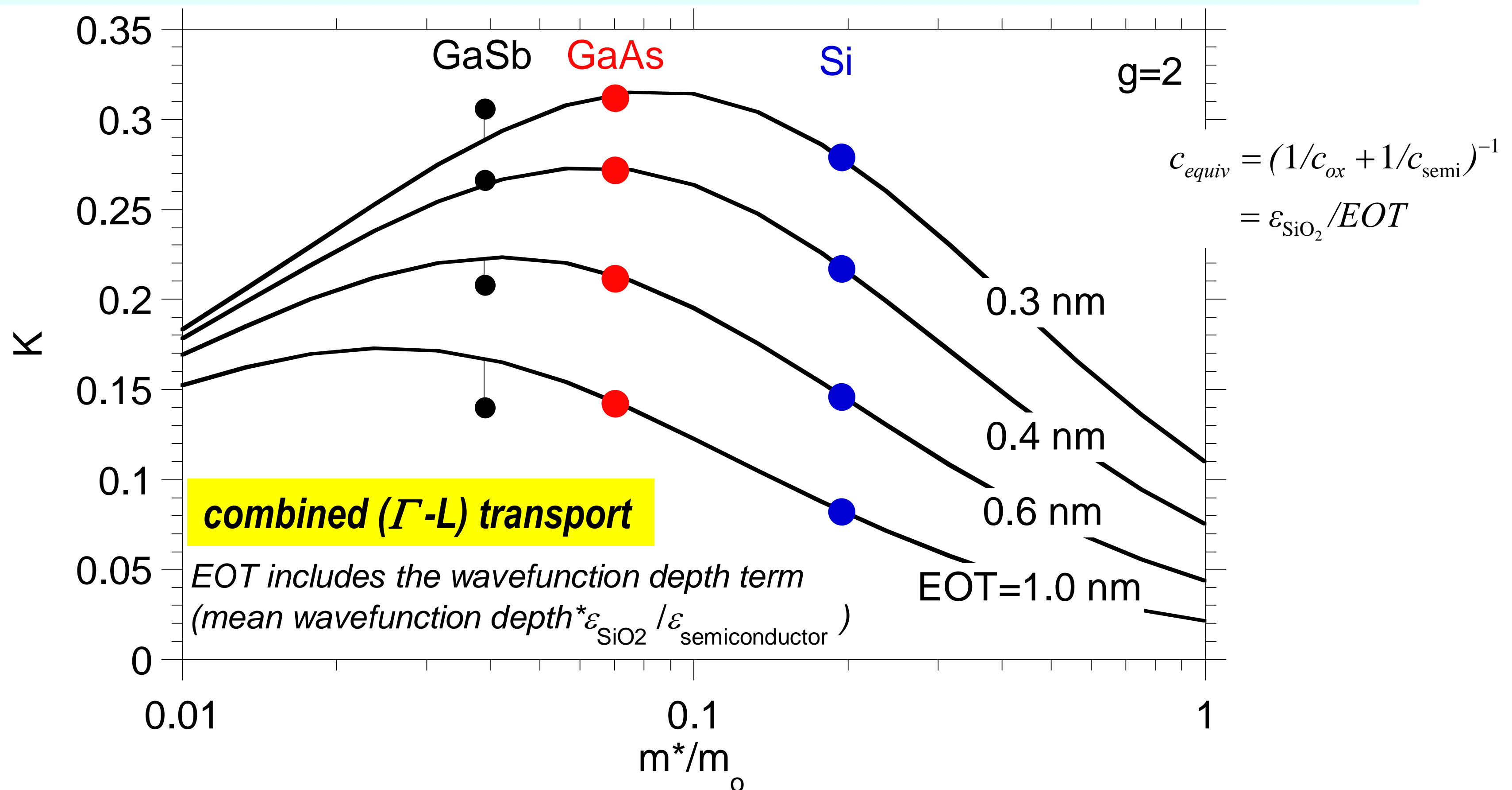
Relative Energies:
Γ= 41 meV
L[111] (1)= 0 meV
L[111] (2)= 84 meV

L[11-1] =175 meV
X=288 meV



Combined Γ-L wells in {111} orientation vs. Si

$$J = \underline{K}\cdot\left(84\,\frac{\text{mA}}{\mu\text{m}}\right)\cdot\left(\frac{V_{gs}-V_{th}}{1\,\text{V}}\right)^{3/2}\quad,\quad \text{where }\ \underline{K} = \frac{g\cdot\left(m^*/m_o\right)^{1/2}}{\left(1+(c_{dos,o}/c_{equiv})\cdot g\cdot(m^*/m_o)\right)^{3/2}}$$

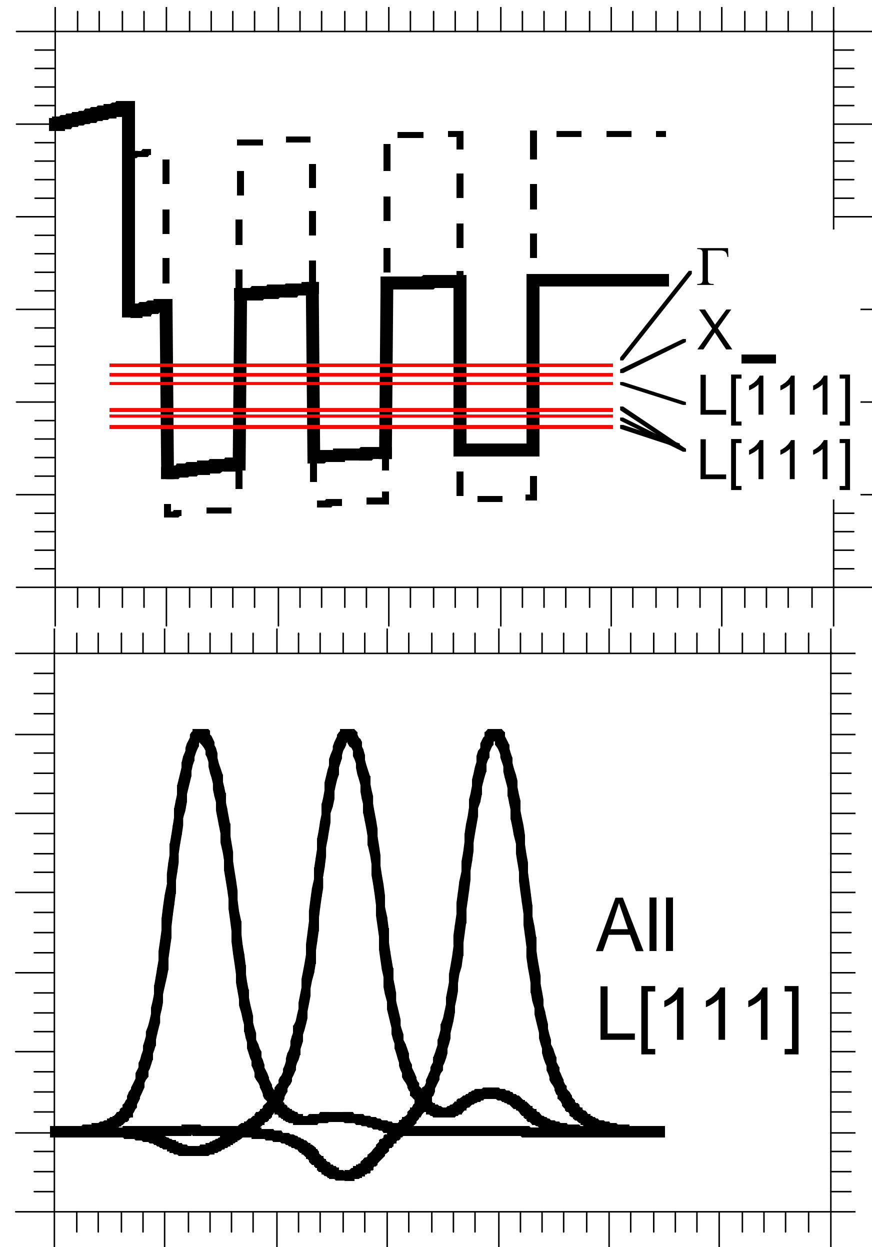


GaAs MOSFET with combined Γ and L transport, 2 nm well→ g=2, m^*/m_0=0.07

GaSb MOSFET with combined Γ and L transport, ~4 nm well→ m_Γ^*/m_0=0.039, m_L^*/m_0=0.1

2nd Approach: Use L valleys in Stacked Wells

Three 0.66 nm GaAs wells
0.66 nm AlSb barriers
[111] orientation



Relative Energies:
Γ=338 meV
L[111](1) = 0 meV
L[111](2)= 61 meV
L[111](3)= 99 meV
L[11-1] =232 meV
X=284 meV

Conclusion

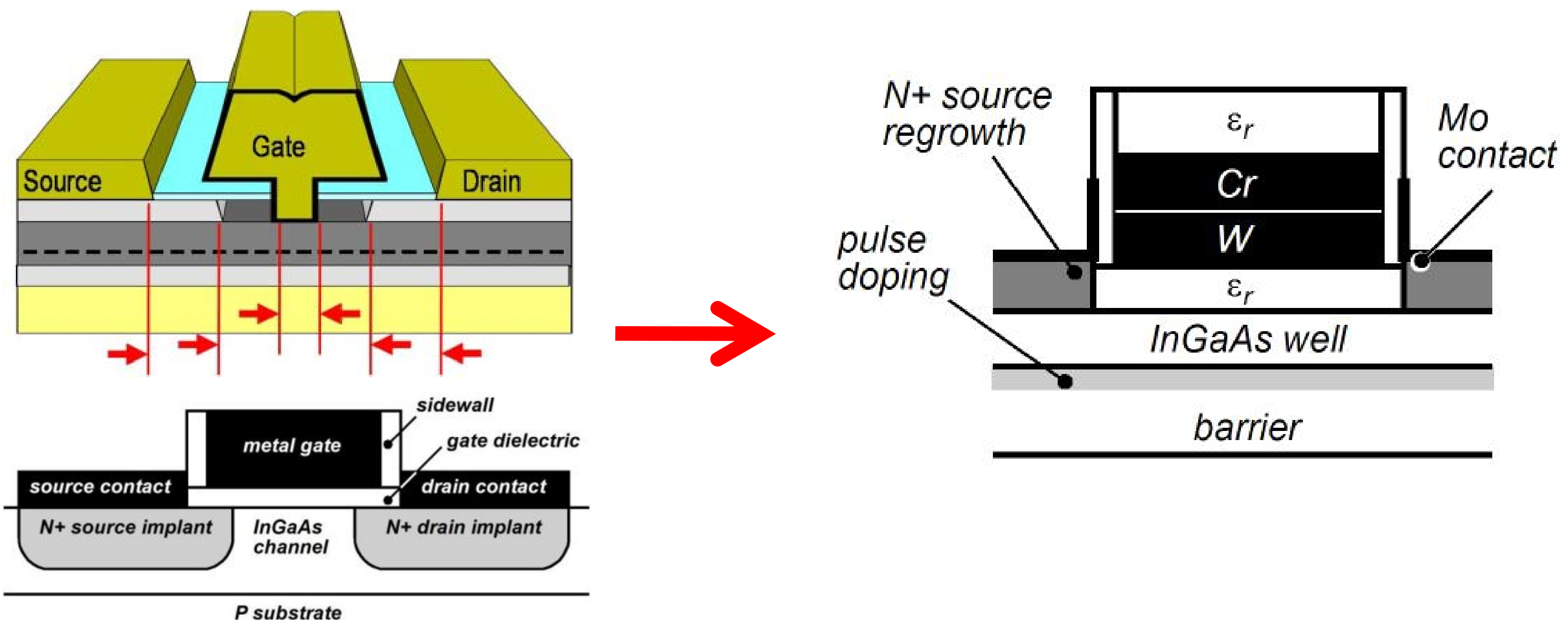
III-V MOS

With appropriate design, III-V channels can provide > current than Si
...even for highly scaled devices

But present III-V device structures are also unsuitable for 10 nm MOS
large access regions, low current densities, deep junctions

Raised S/D regrowth process is a path towards a nm VLSI III-V device

Gate dielectric still requires major progress...



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