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III-V FET Channel Designs for High Current Densities and Thin Inversion Layers

Mark Rodwell
University of California, Santa Barbara

Coauthors:

W. Frensley:
University of Texas, Dallas

S. Steiger, S. Lee, Y. Tan, G. Hegde, G. Klimek
Network for Computational Nanotechnology, Purdue University

E. Chagarov, L. Wang, P. Asbeck, A. Kummel,
University of California, San Diego

T. Boykin
University of Alabama, Huntsville

J. N. Schulman
The Aerospace Corporation, El Segundo, CA.

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rodwell@ece.ucsb.edu 805-893-3244, 805-893-5705 fax

Thin, high current density III-V FET channels

InGaAs, InAs FETs

THz & VLSI need high current

low m→ high velocities* ☺

FET scaling for speed requires increased charge density

low m →low charge density* ☹

Density of states bottleneck *(Solomon & Laux IEDM 2001)*

→ *For < 0.6 nm EOT, silicon beats III-Vs* ☹

Open the bottle !

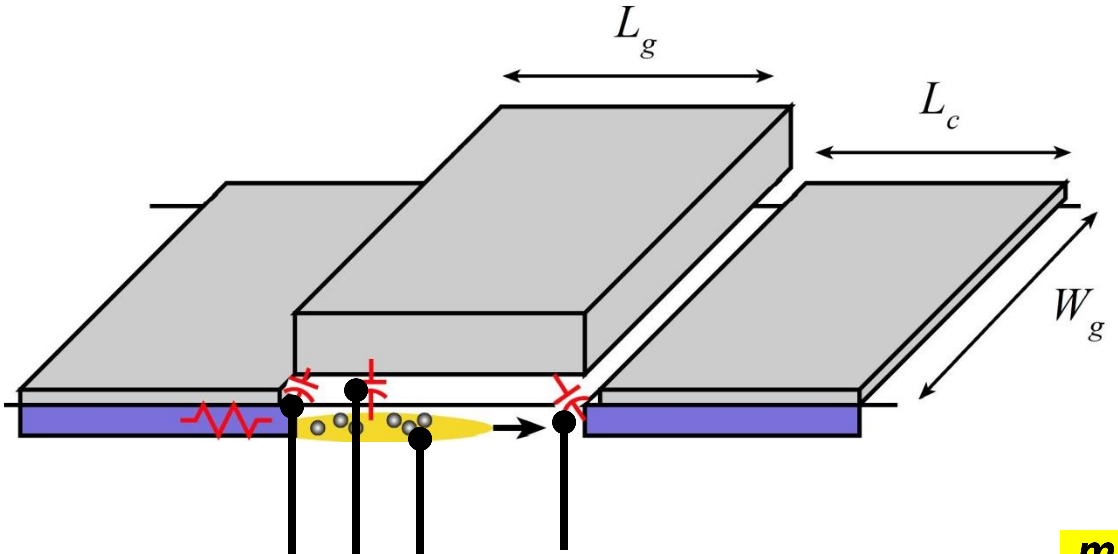
low transport mass → high $v_{carrier}$

multiple valleys or anistropic valleys → high DOS

Use the L valleys.

Simple FET Scaling

Goal: double transistor bandwidth when used in any circuit
→ reduce 2:1 all capacitances and all transport delays
→ keep constant all resistances, voltages, currents



gate-source, gate-drain fringing capacitances: 0.15-0.25 fF/μm

$$C_{gd}/W_g \sim \varepsilon$$

must increase gate capacitance/area

$$g_m/W_g \sim v \cdot (C_{gs}/L_g W_g)$$

$$C_{gs}/W_g = (C_{gs}/W_g L_g) \cdot L_g$$

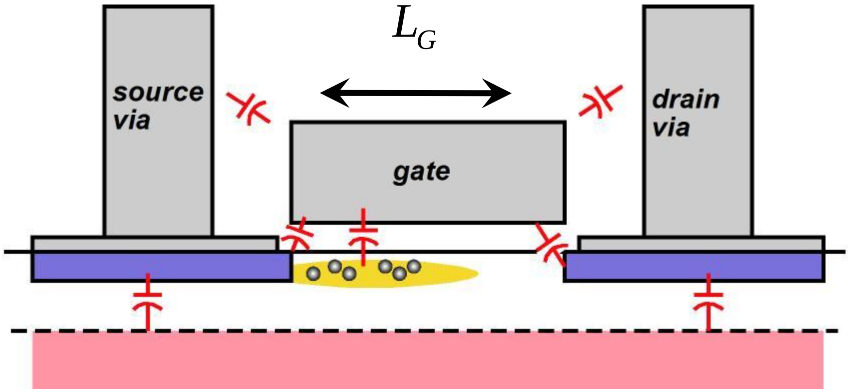
must reduce gate length

$$C_{gs,f}/W_g \sim \varepsilon$$

To double speed, we must double (g_m/W_g), (I_D/W_g), $(C_{gs}/L_g W_g)$, n_s.

FET Scaling Laws

Changes required to double device / circuit bandwidth.



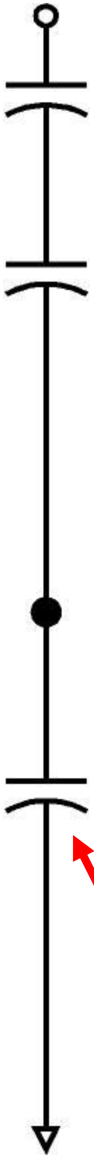
$(\text{gate width } W_G)$

laws in constant-voltage limit:

FET parameter	change
gate length	decrease 2:1
current density (mA/μm), g_m (mS/μm)	increase 2:1
channel 2DEG electron density	increase 2:1
electron mass in transport direction	constant
gate-channel capacitance density	increase 2:1
dielectric equivalent thickness	decrease 2:1
channel thickness	decrease 2:1
channel density of states	increase 2:1
source & drain contact resistivities	decrease 4:1

Current densities should double
Charge densities must double

Semiconductor Capacitances Must Also Scale



$(V_{gs}-V_{th})$

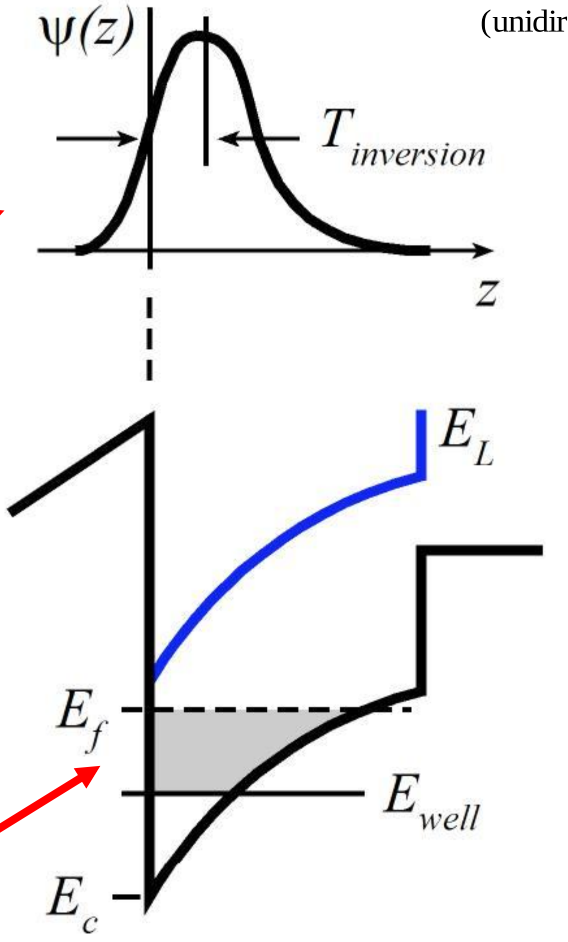
c_{ox}

$c_{\text{depth}} = \varepsilon / T_{\text{inversion}}$

$(E_f - E_{well})/q$

$c_{dos} = q^2 g m^* / 2\pi\hbar^2$

(unidirectional motion)

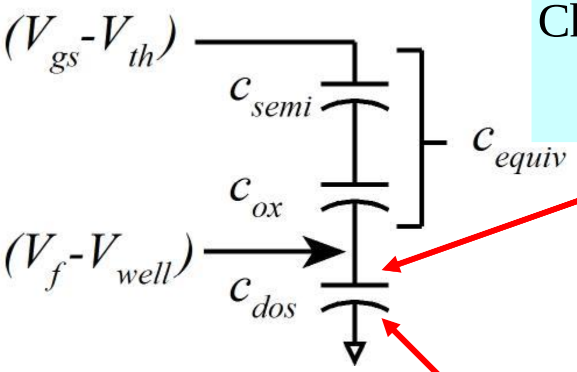


channel charge $= qn_s = c_{dos}(V_f - V_{well}) = q(E_f - E_{well}) \cdot (gm^* / 2\pi\hbar^2)$

Inversion thickness & density of states must also both scale.

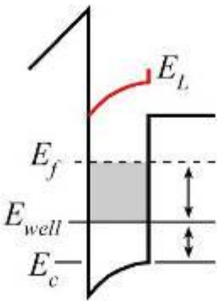
Calculating Current: Ballistic Limit

Natori



Channel Fermi voltage = voltage applied to c_{dos}

determines Fermi velocity v_f through $E_f = qV_f = m^* v_f^2/2$



mean electron velocity $= \bar{v} = (4/3\pi)v_f$

Channel charge : $\rho_s = c_{dos}\left(V_f - V_c\right) = \dfrac{c_{dos}c_{equiv}}{c_{equiv}+c_{dos}}\left(V_{gs}-V_{th}\right)$

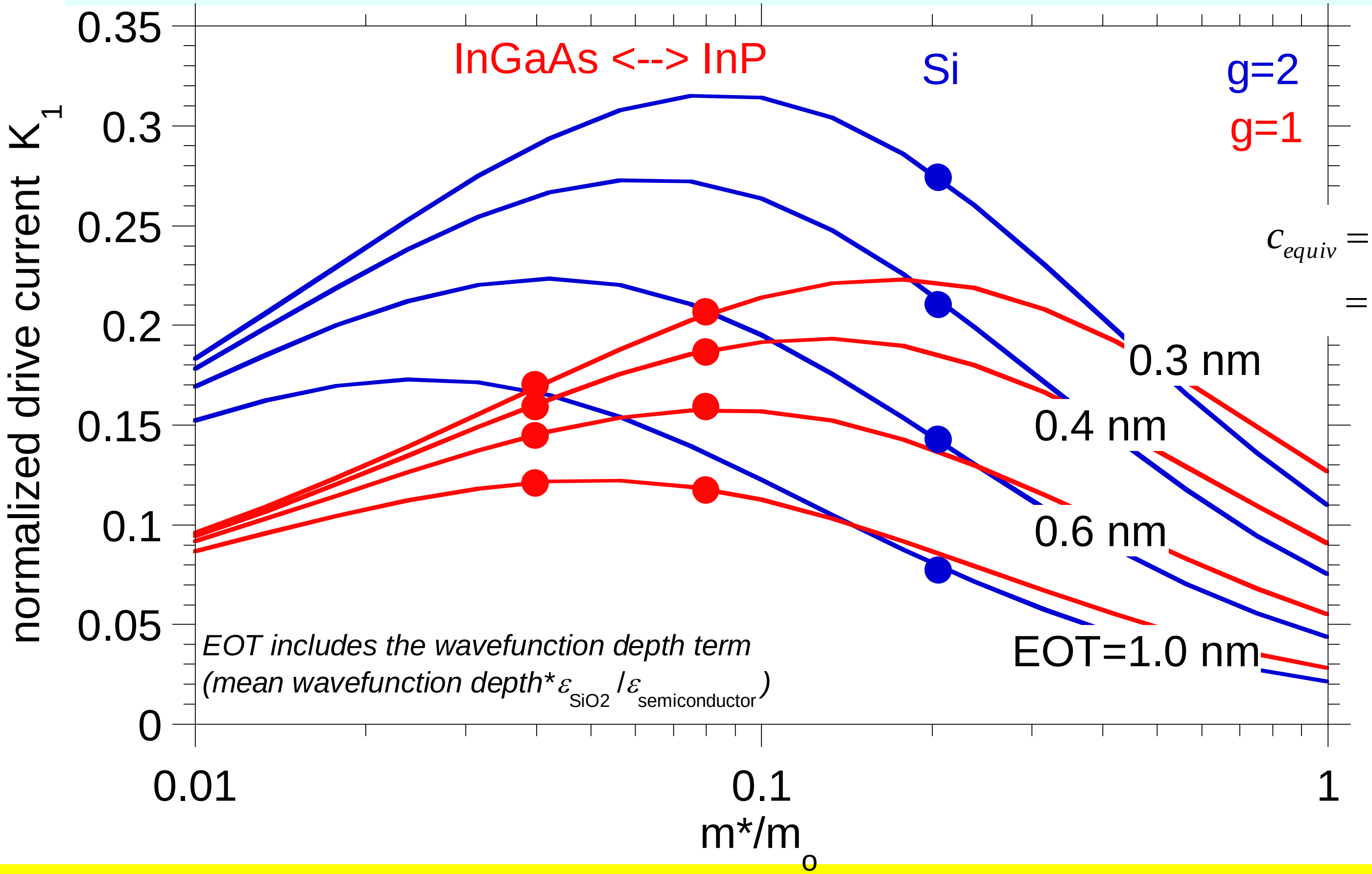
$c_{dos} = q^2 g m^*/2\pi\hbar^2 = c_{dos,o}\cdot g\cdot(m^*/m_o)$, where g is the # of band minima

$$\Rightarrow \quad J = \left(84\,\frac{\text{mA}}{\mu\text{m}}\right)\frac{g\cdot(m^*/m_o)^{1/2}}{\left(1+(c_{dos,o}/c_{ox})\cdot g\cdot(m^*/m_o)\right)^{3/2}}\left(\frac{V_{gs}-V_{th}}{1\,\text{V}}\right)^{3/2}$$

Do we get highest current with high or low mass ?

Drive current versus mass, # valleys, and EOT

$$J = \underline{K_1}\cdot\left(84\frac{\mathrm{mA}}{\mu\mathrm{m}}\right)\cdot\left(\frac{V_{gs}-V_{th}}{1\,\mathrm{V}}\right)^{3/2}, \quad \text{where } \underline{K_1} = \frac{g\cdot\left(m^*/m_o\right)^{1/2}}{\left(1+(c_{dos,o}/c_{equiv})\cdot g\cdot(m^*/m_o)\right)^{3/2}}$$



$$c_{equiv} = (1/c_{ox} + 1/c_{\mathrm{depth}})^{-1} = \varepsilon_{\mathrm{SiO_2}}/EOT$$

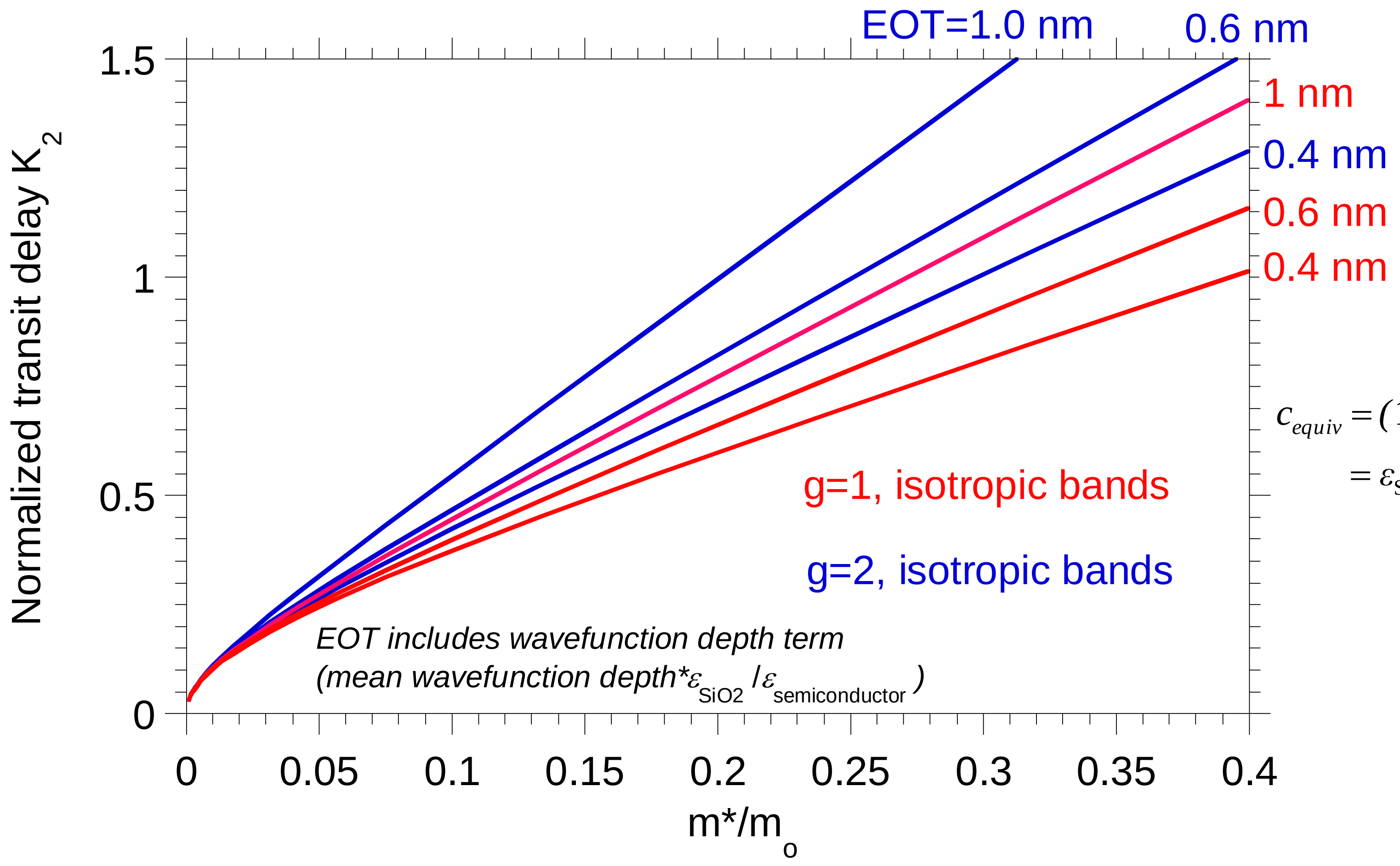
InGaAs MOSFETs: superior I_d to Si at large EOT.

InGaAs MOSFETs: <u>inferior</u> I_d to Si at <u>small</u> EOT.

Solomon / Laux Density-of-States-Bottleneck → III-V loses to Si.

Transit delay versus mass, # valleys, and EOT

$$\tau_{ch} \equiv \frac{Q_{ch}}{I_D} = \underline{K_2}\cdot\left(\frac{L_g}{2.52\cdot 10^7\ \text{cm/s}}\right)\cdot\left(\frac{1\,\text{Volt}}{V_{gs}-V_{th}}\right)^{1/2} \quad \text{where } \underline{K_2} = \left(\frac{m^*}{m_0}\right)^{1/2}\cdot\left(1+\frac{c_{dos,o}}{c_{eq}}\cdot g\cdot\frac{m^*}{m_o}\right)^{1/2}$$



g=1, isotropic bands

g=2, isotropic bands

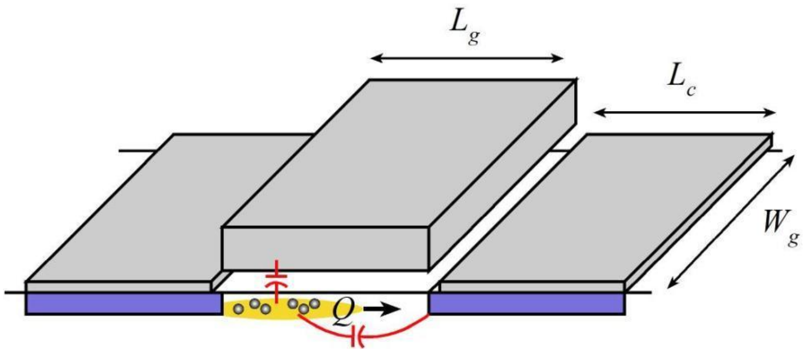
EOT includes wavefunction depth term
(mean wavefunction depth$\varepsilon_{SiO2}/\varepsilon_{semiconductor}$)*

$$c_{equiv} = (1/c_{ox} + 1/c_{semi})^{-1} = \varepsilon_{SiO_2}/EOT$$

Low m* gives lowest transit time, lowest C_{gs} at <u>any</u> EOT.

Low effective mass also impairs vertical scaling

Shallow electron distribution needed for high I_d, high g_m / G_{ds} ratio, low drain-induced barrier lowering.



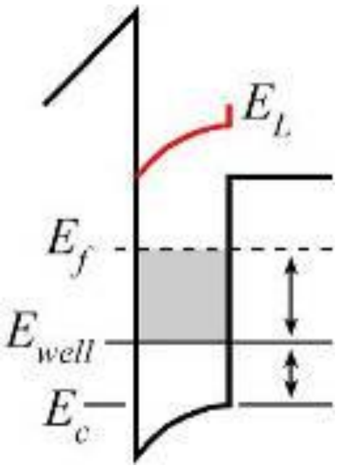
Energy of L^{th} well state $\propto L^2 / m^* T_{well}^2$.

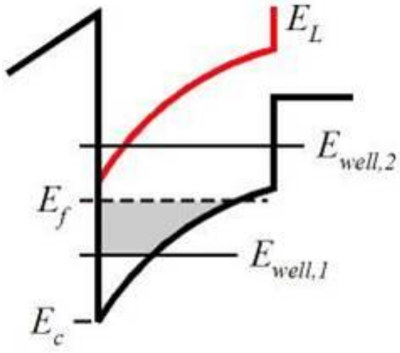
For thin wells,

only 1st state can be populated.

For <u>very</u> thin wells,

1st state approaches L-valley.



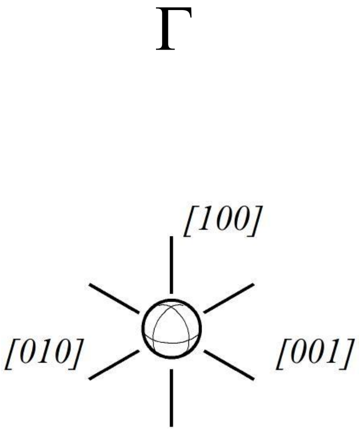


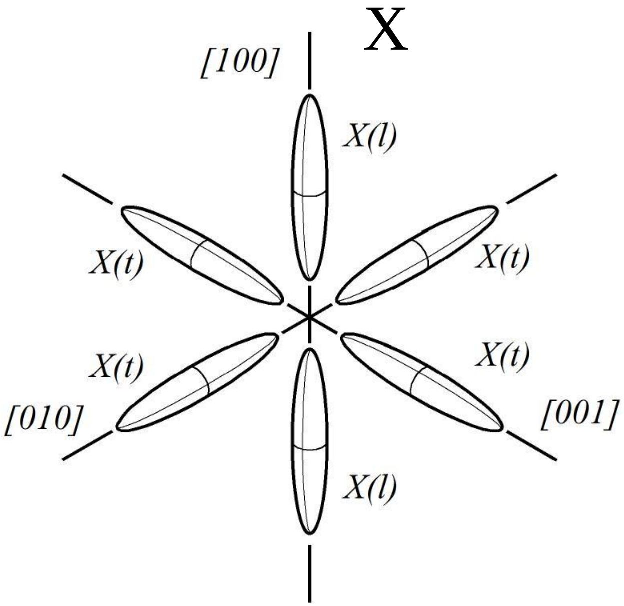
Only one vertical state in well.

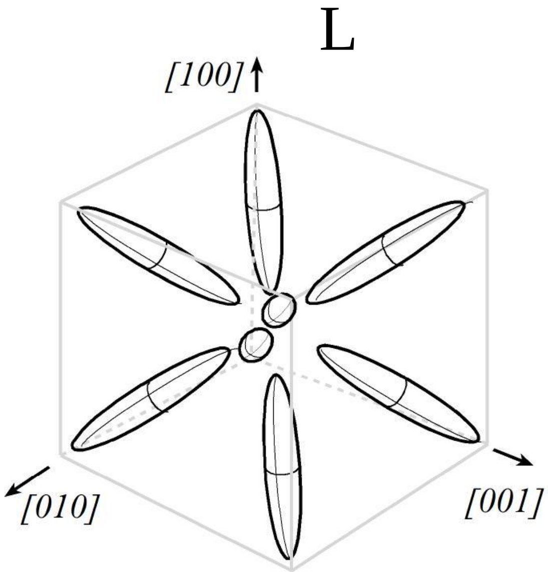
Minimum ~ 3 nm well thickness.

→ *Hard to scale below 10-16 nm L_g.*

III-V Band Properties, normal {100} Wafer



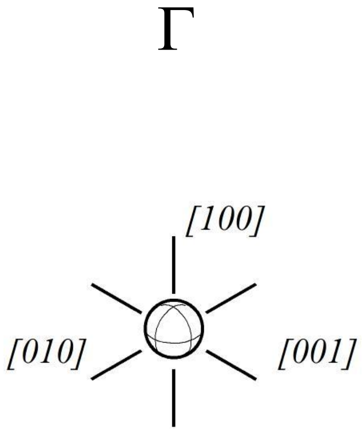


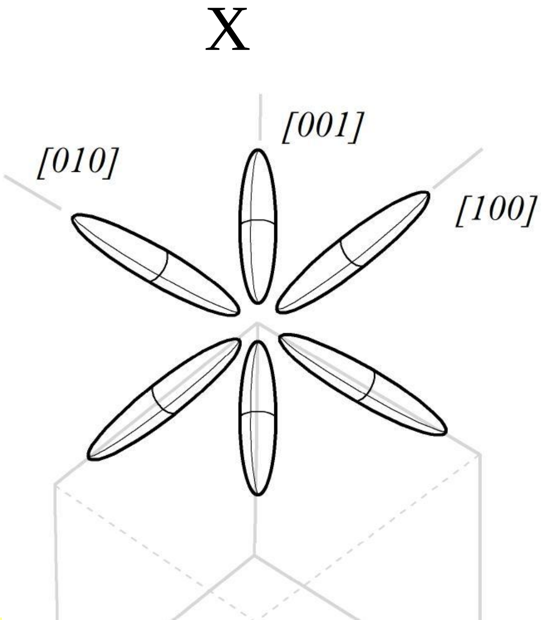


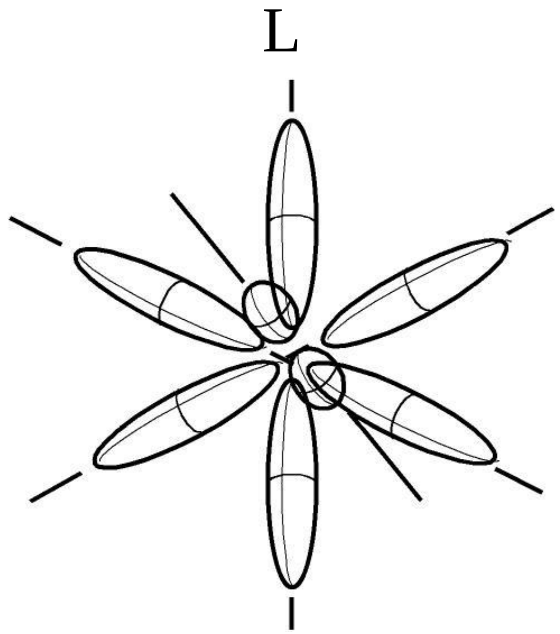
		Γ valley	X valley			L valley		
material	substrate	m^* / m_o	m_l / m_o	m_t / m_o	$E_x - E_\Gamma$	m_l / m_o	m_t / m_o	$E_L - E_\Gamma$
$In_{0.5}Ga_{0.5}As$	InP	0.045	1.29	0.19	0.83 eV	1.23	0.062	0.47 eV
InAs	InP	0.026	1.13	0.16	0.87 eV	0.65	0.050	0.57 eV
GaAs	GaAs	0.067	1.30	0.22	0.47 eV	1.90	0.075	0.28 eV
Si	Si	---	0.92	0.19	(negative)			

L - valley transverse masses are comparable to Γ valleys

Consider instead: valleys in {111} Wafer







		Γ valley	X valley			L valley		
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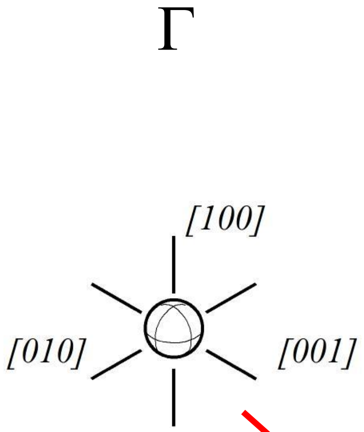
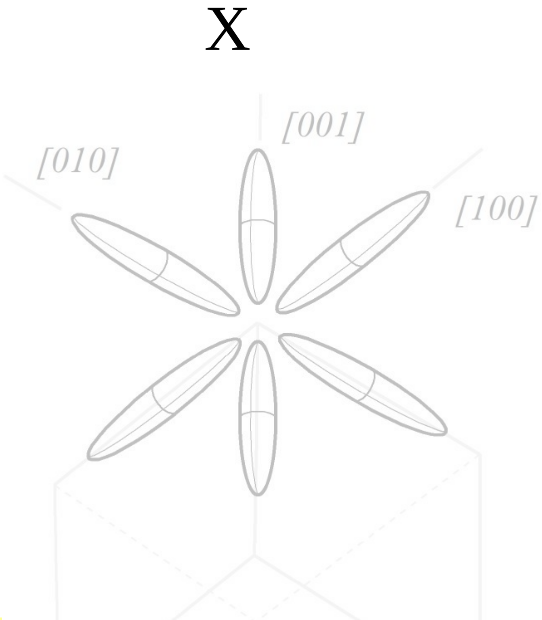
GaAs	GaAs	0.067	1.30	0.22	0.47 eV	1.90	0.075	0.28 eV
Si	Si	- - -	0.92	0.19	(negative)			

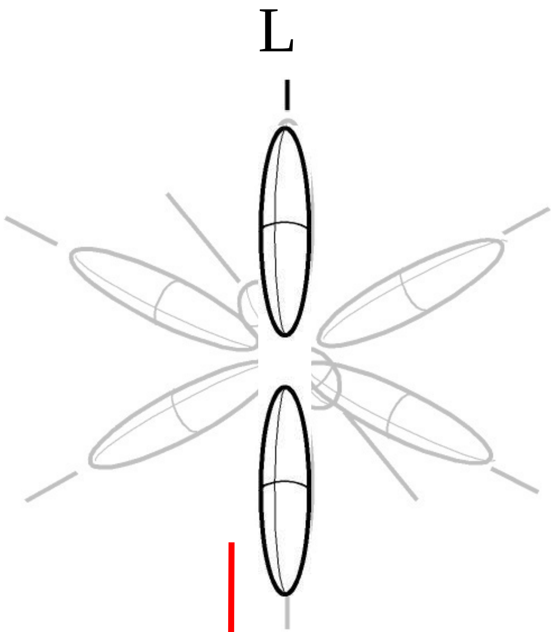
Orientation : one L valley has high vertical mass

X valleys & three L valleys have moderate vertical mass

Valley in {111} wafer: with quantization in thin wells







		Γ valley	X valley			L valley		
material	substrate	m^* / m_o	m_l / m_o	m_t / m_o	$E_x - E_\Gamma$	m_l / m_o	m_t / m_o	$E_L - E_\Gamma$
$In_{0.5}Ga_{0.5}As$	InP	0.045	1.29	0.19	0.83 eV	1.23	0.062	0.47 eV
InAs	InP	0.026	1.13	0.16	0.87 eV	0.65	0.050	0.57 eV
GaAs	GaAs	0.067	1.30	0.22	0.47 eV	1.90	0.075	0.28 eV
Si	Si	---	0.92	0.19	(negative)			

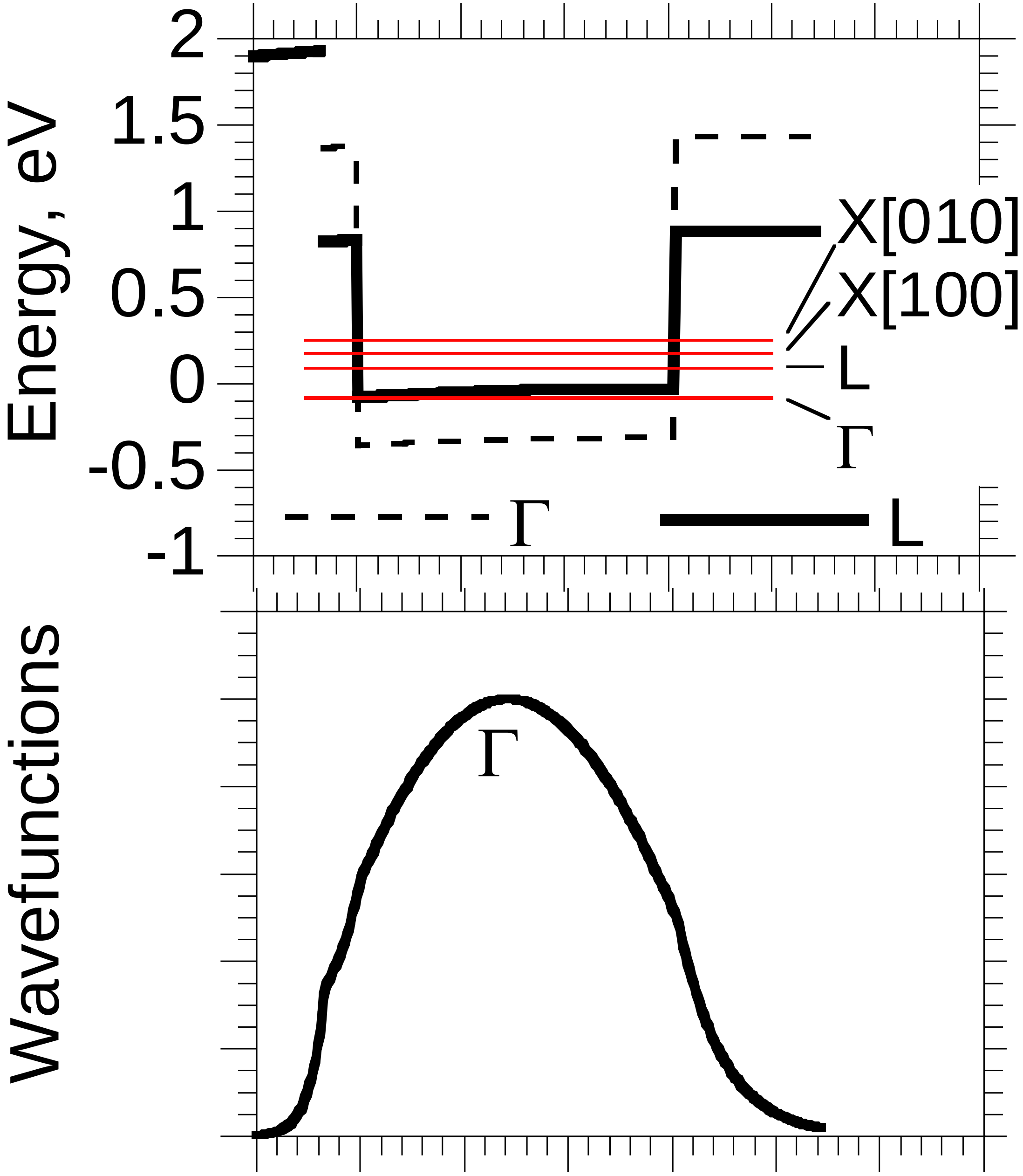
Selects L[111] valley; low transverse mass

{111} Γ-L FET: Candidate Channel Materials

material	Γ valley	L valley			Well thickness for $\Gamma - \mathrm{L}$ alignment
	m^* / m_o	m_l / m_o	m_t / m_o	$E_L - E_\Gamma$	
$\mathrm{In_{0.5}Ga_{0.5}As}$	0.045	1.23	0.062	0.47 eV	1 nm (?)
GaAs	0.067	1.90	0.075	0.28 eV	2 nm
GaSb	0.039	1.30	0.10	0.07 eV	4 nm
Ge		1.58	0.08	(negative)	---

Standard III-V FET: Γ valley in [100] orientation

3 nm GaAs well
AlSb barriers

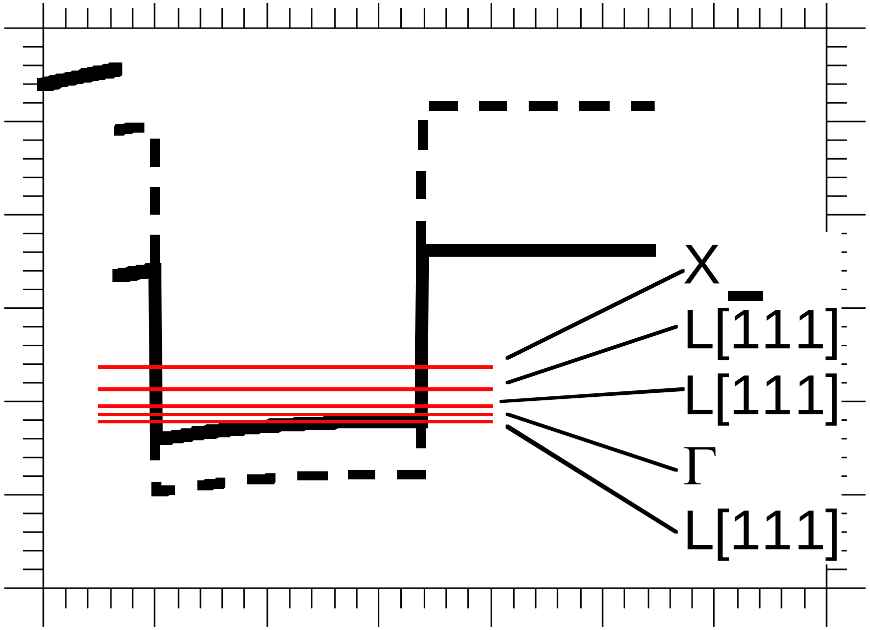


Γ=0 eV

L=177 meV
X[100]= 264 meV
X[010] = 337 meV

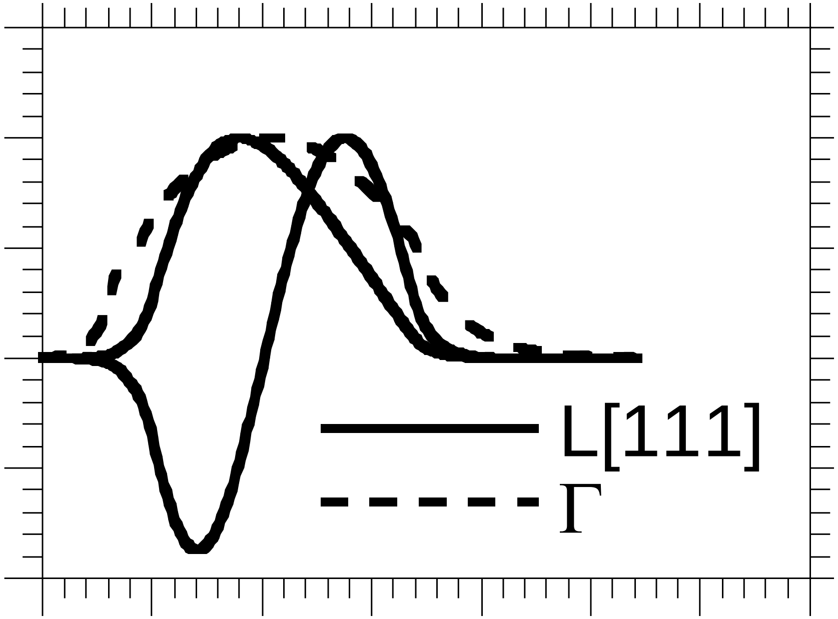
1st Approach: Use both Γ and L valleys in [111]

2.3 nm GaAs well
AlSb barriers
[111] orientation



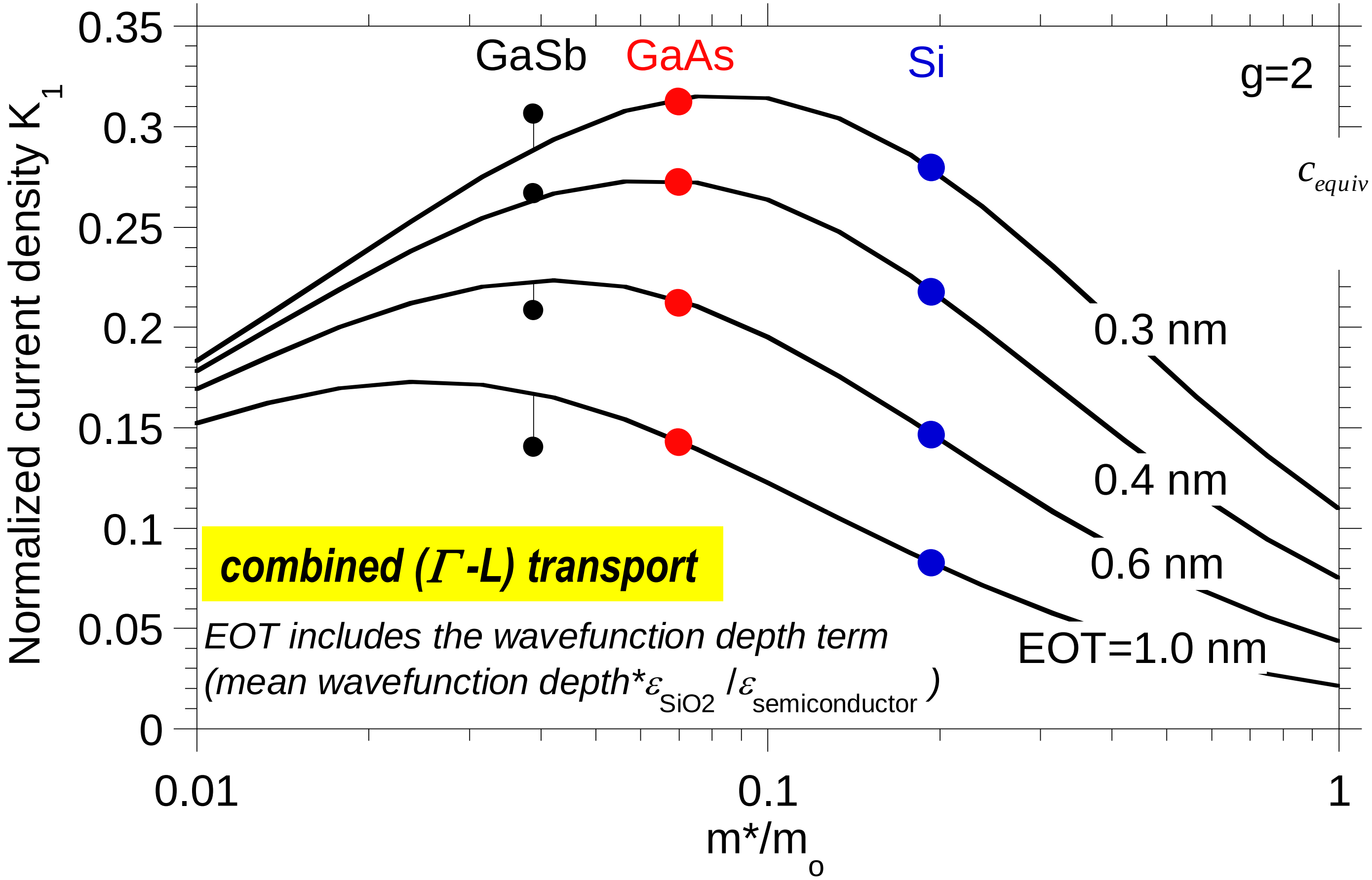
Γ= 41 meV
L[111] (1)= 0 meV
L[111] (2)= 84 meV

L[11$\bar{1}$] , etc. =175 meV
X=288 meV



Combined Γ-L wells in {111} orientation vs. Si

$$J = \underline{K_1} \cdot \left(84\,\frac{\text{mA}}{\mu\text{m}}\right) \cdot \left(\frac{V_{gs} - V_{th}}{1\,\text{V}}\right)^{3/2} \quad , \quad \text{where} \quad \underline{K_1} = \frac{g \cdot \left(m^*/m_o\right)^{1/2}}{\left(1 + (c_{dos,o}/c_{equiv}) \cdot g \cdot (m^*/m_o)\right)^{3/2}}$$



combined (Γ-L) transport

EOT includes the wavefunction depth term (mean wavefunction depth*$\varepsilon_{SiO2}/\varepsilon_{semiconductor}$)

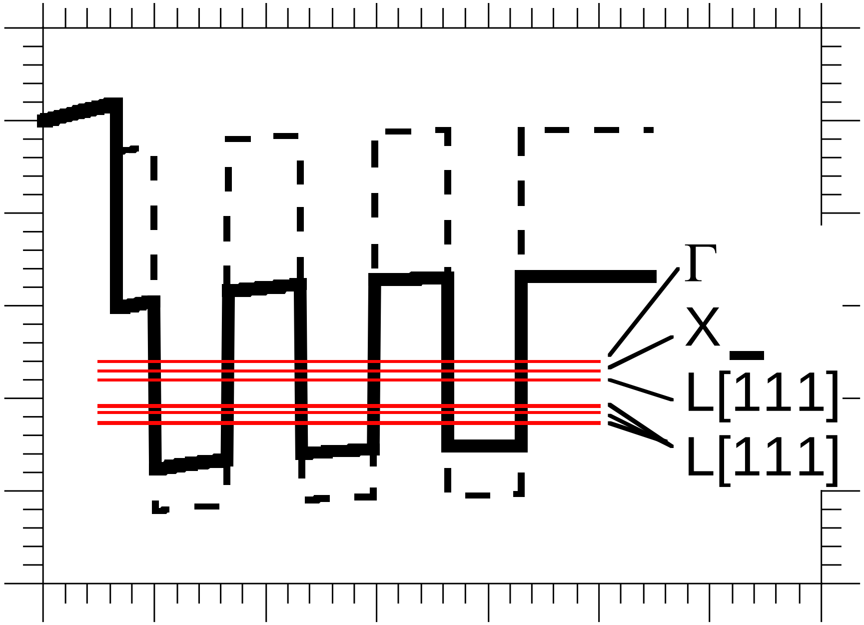
$$c_{equiv} = (1/c_{ox} + 1/c_{semi})^{-1}$$
$$= \varepsilon_{SiO_2}/EOT$$

2 nm GaAs Γ/L well→ g =2, m^*/m_0=0.07

4 nm GaSb Γ/L well→ m_{Γ}^*/m_0=0.039, $m_{L,t}^*/m_0$=0.1

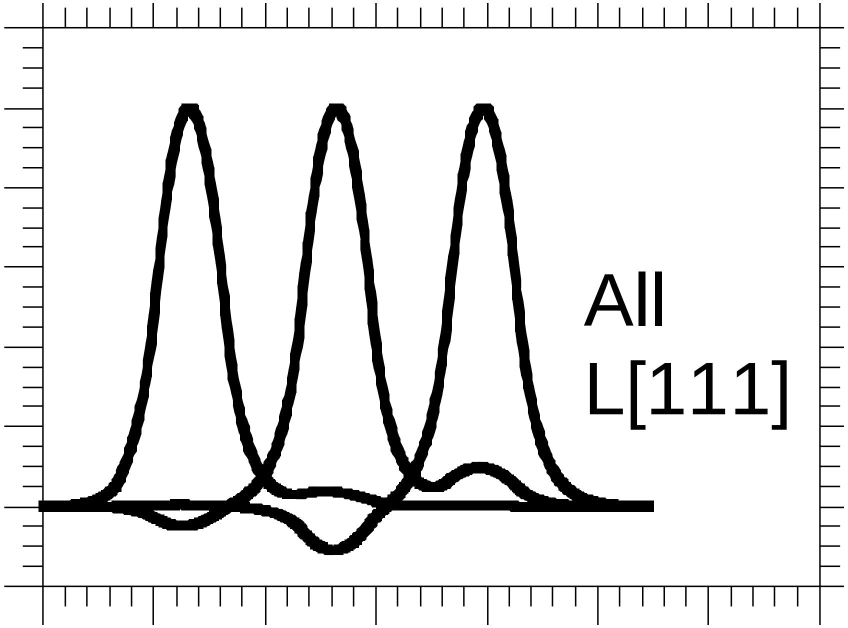
2nd Approach: Use L valleys in Stacked Wells

Three 0.66 nm GaAs wells
0.66 nm AlSb barriers
[111] orientation

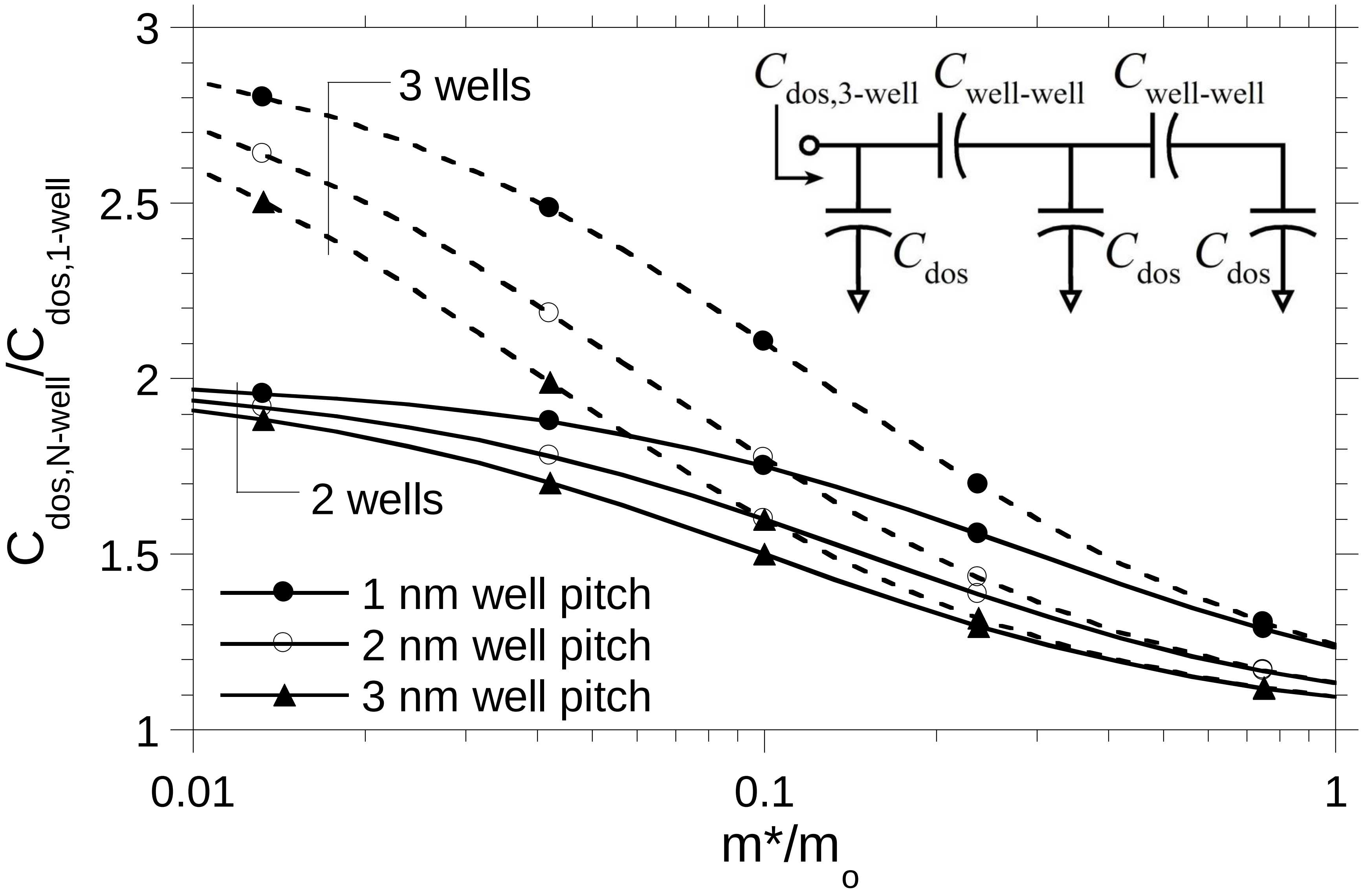


L[111](1) = 0 meV
L[111](2)= 61 meV
L[111](3)= 99 meV

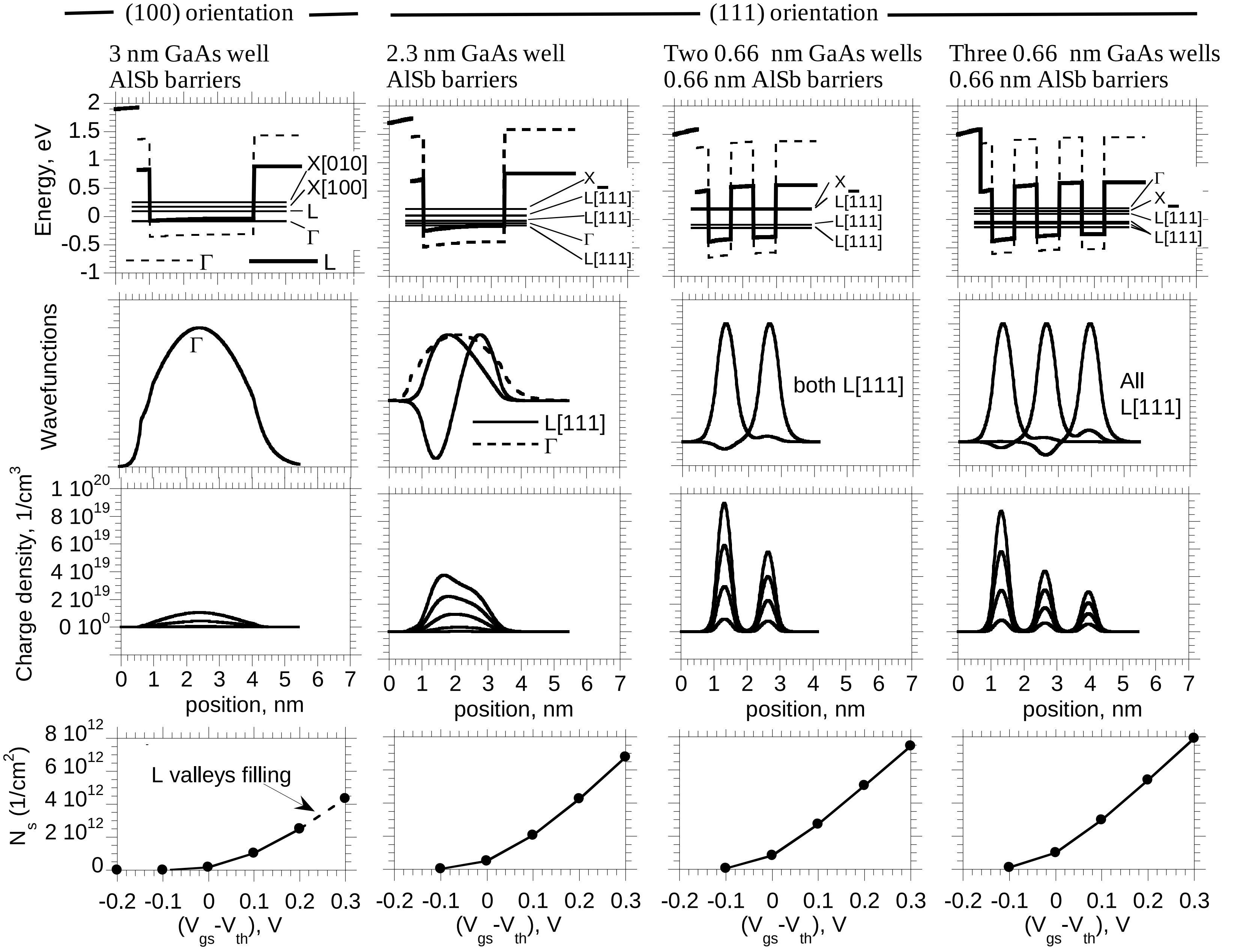
Γ=338 meV
L[11$\bar{1}$], etc =232 meV
X=284 meV



Increase in C_{dos} with 2 and 3 wells



3 High Current Density (111) GaAs/AlSb Designs



Concerns

Nonparabolic bands reduce bound state energies

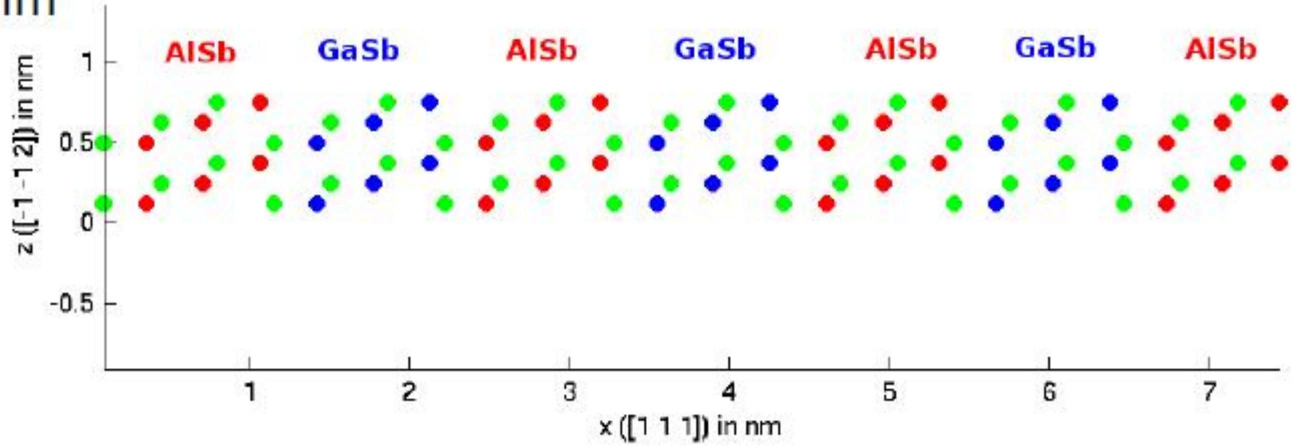
Failure of effective mass approximation:1-2 nm wells

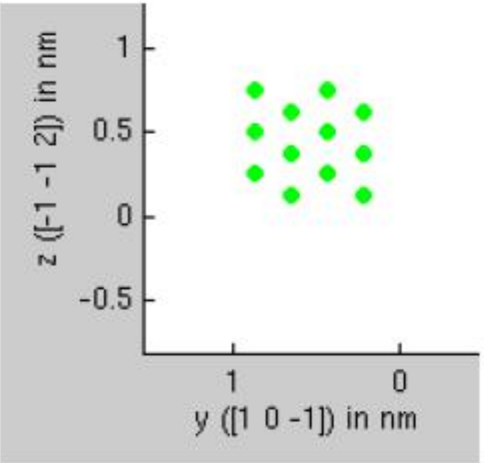
1-2 monolayer fluctuations in growth
→ scattering→ collapse in mobility

Sebastian Steiger

- Supervised by Profs. Gerhard Klimeck and Timothy Boykin
- Simulation software: OMEN3D by Hoon Ryu and Sunhee Lee
- TB parameters for AlSb and GaSb: Ganesh Hegde and Yaohua Tan

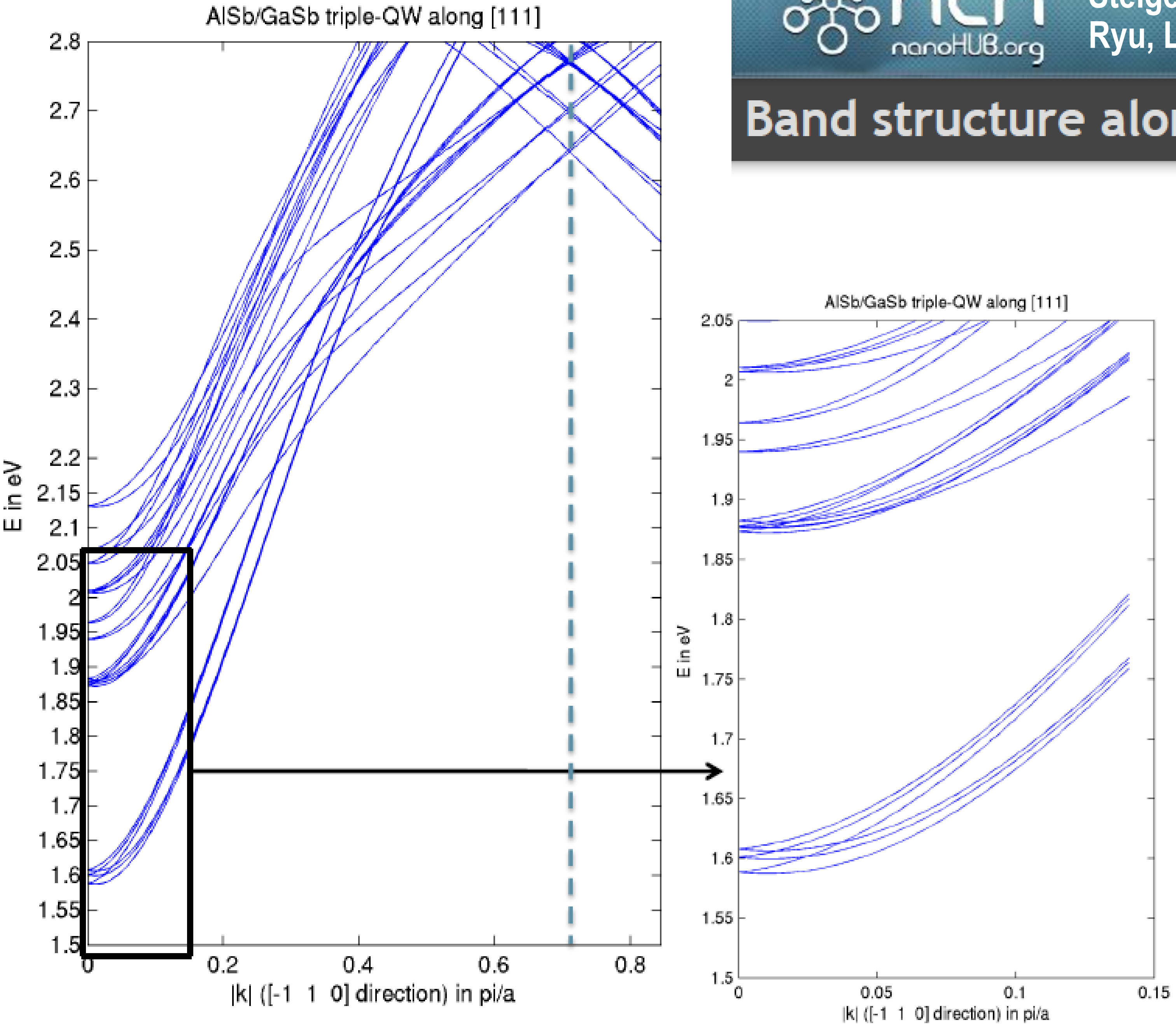
- AlSb-GaSb triple-QW
- QW extension ~1.2nm





- Non-primitive unit cell in lateral directions
- Therefore zone folding in E(k)

Band structure along [-1 1 0]



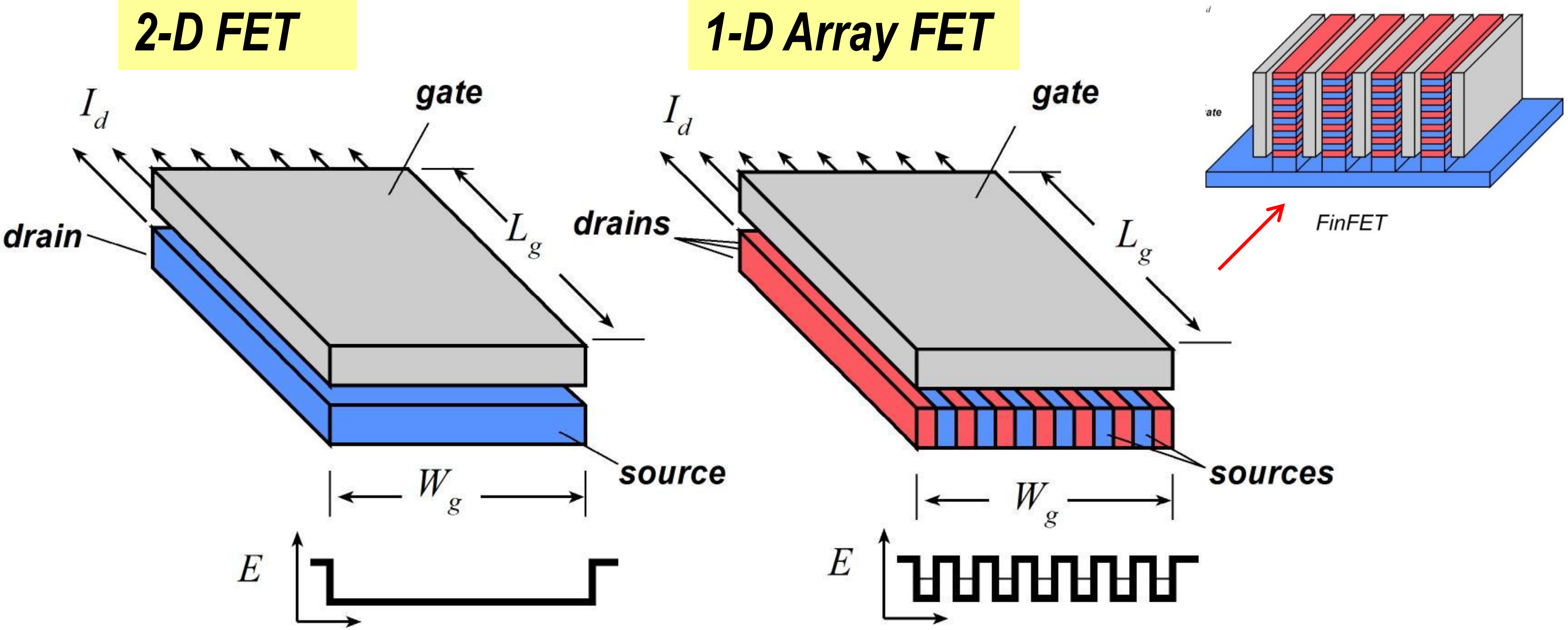
Effective masses:

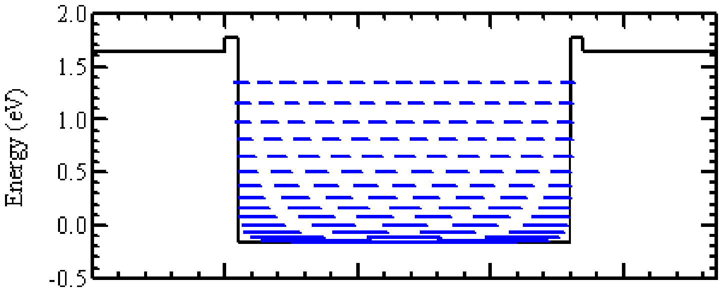
E=1.587: m*=0.0875
E=1.589: m*=0.0624
E=1.600: m*=0.0902
E=1.601: m*=0.0650
E=1.607: m*=0.0937
E=1.608: m*=0.0663
E=1.872: m*=0.0972
E=1.874: m*=0.0706
E=1.877: m*=0.1448
E=1.878: m*=0.1122
E=1.877: m*=0.1066
E=1.878: m*=0.0767
E=1.882: m*=0.1053
E=1.883: m*=0.0756
E=1.940: m*=0.1395
E=1.940: m*=0.1154
E=1.964: m*=0.0853
E=1.965: m*=0.0751

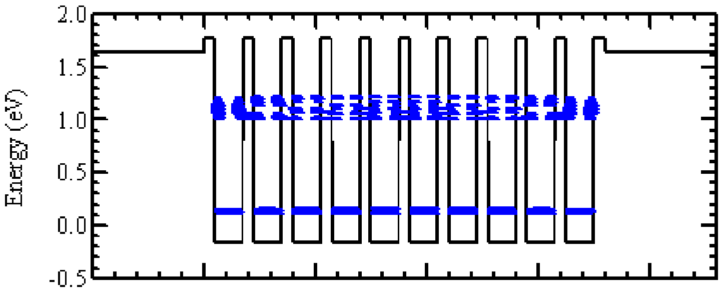
1-D FET array = 2-D FET with high transverse mass

2-D FET

1-D Array FET

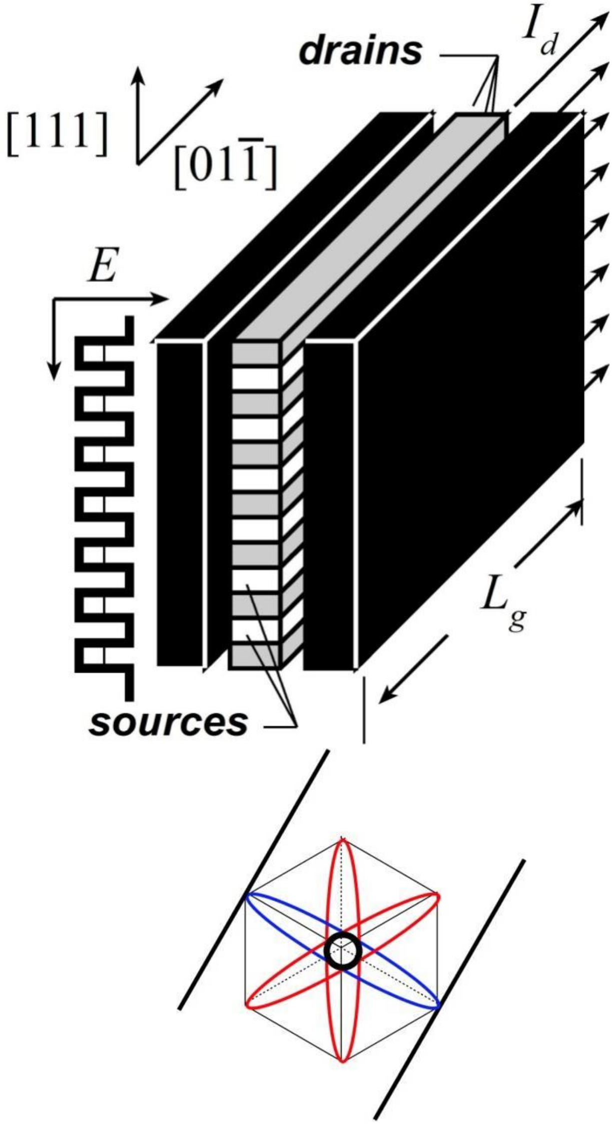


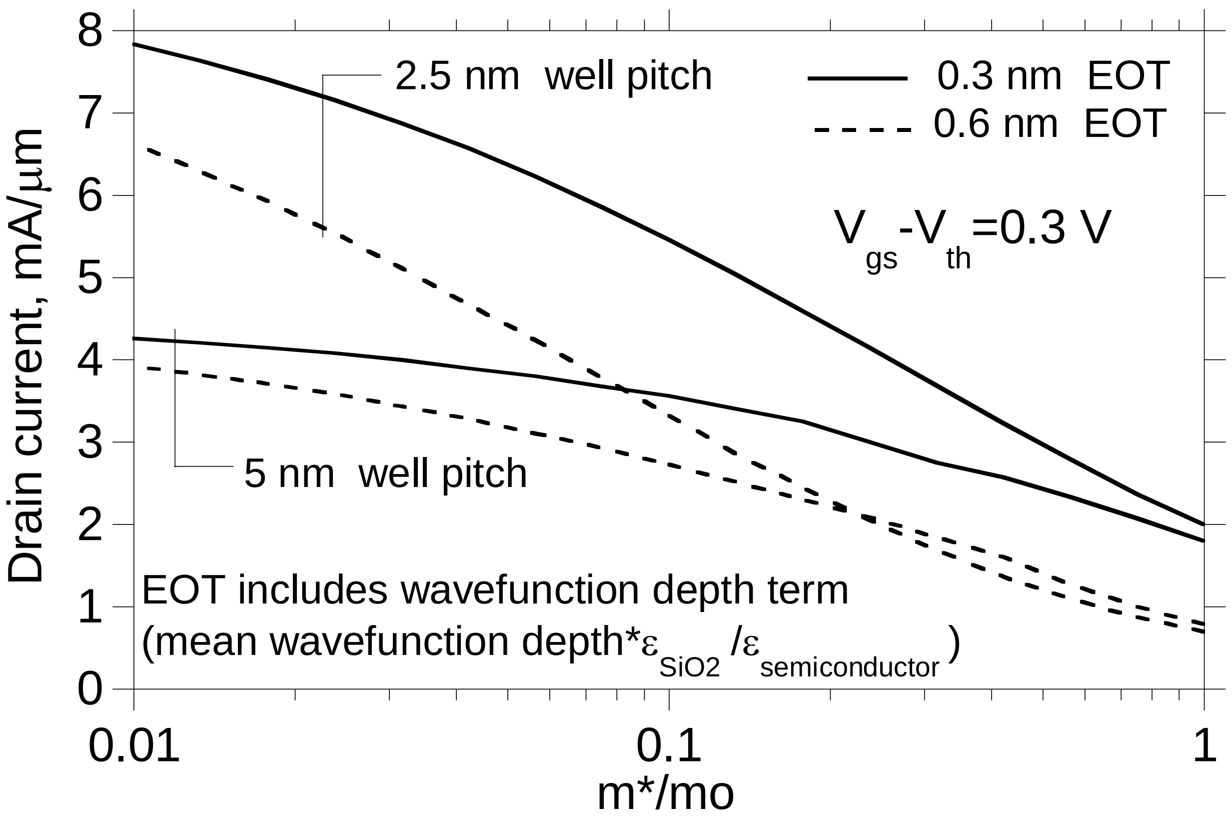




Weak coupling → narrow transverse-mode energy distribution→ high density of states

3rd Approach: High Current Density L-Valley MQW FINFETs

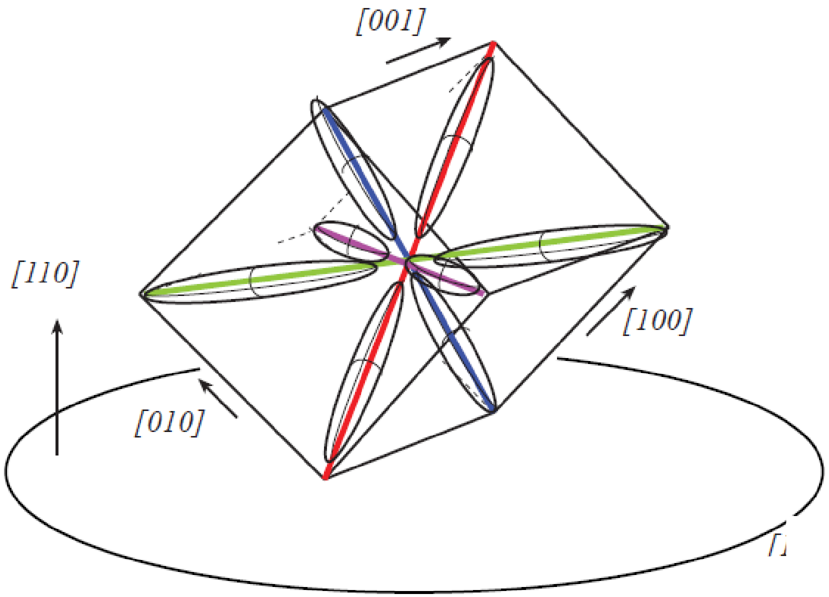


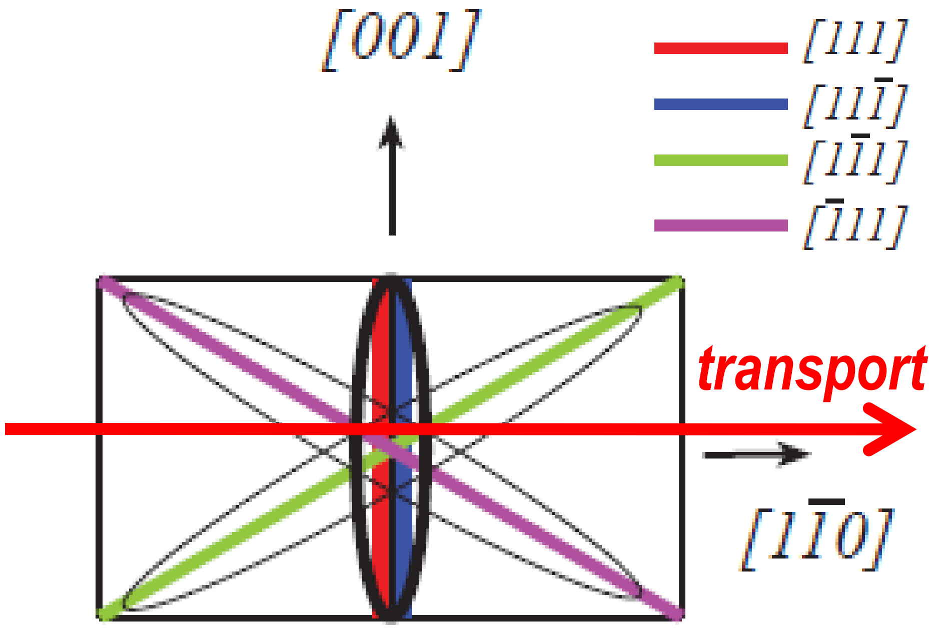


valley energies $E_{\min,i}=qV_{\min,i}=\dfrac{\hbar^2\pi^2}{2m^*W^2}i^2$ current $I=\sum_i\dfrac{gq^2}{\pi\hbar}\left(V_f-V_{\min,i}\right)$ charge : $Q_{ch}=\sum_i\dfrac{gl}{\pi\hbar}\cdot\sqrt{2m^*q\left(V_f-V_{\min,i}\right)}$ gate voltage : $V_{gs}=V_f+Q_{ch}/C_{ox}$

4th Approach: {110} Orientation→ Anisotropic Bands

P. Asbeck





L[111], L[11$\bar{1}$]: moderate vertical mass → valleys populate

High in-plane mass perpendicular to transport → high density of states

Low in-plane mass parallel to transport → high carrier velocity

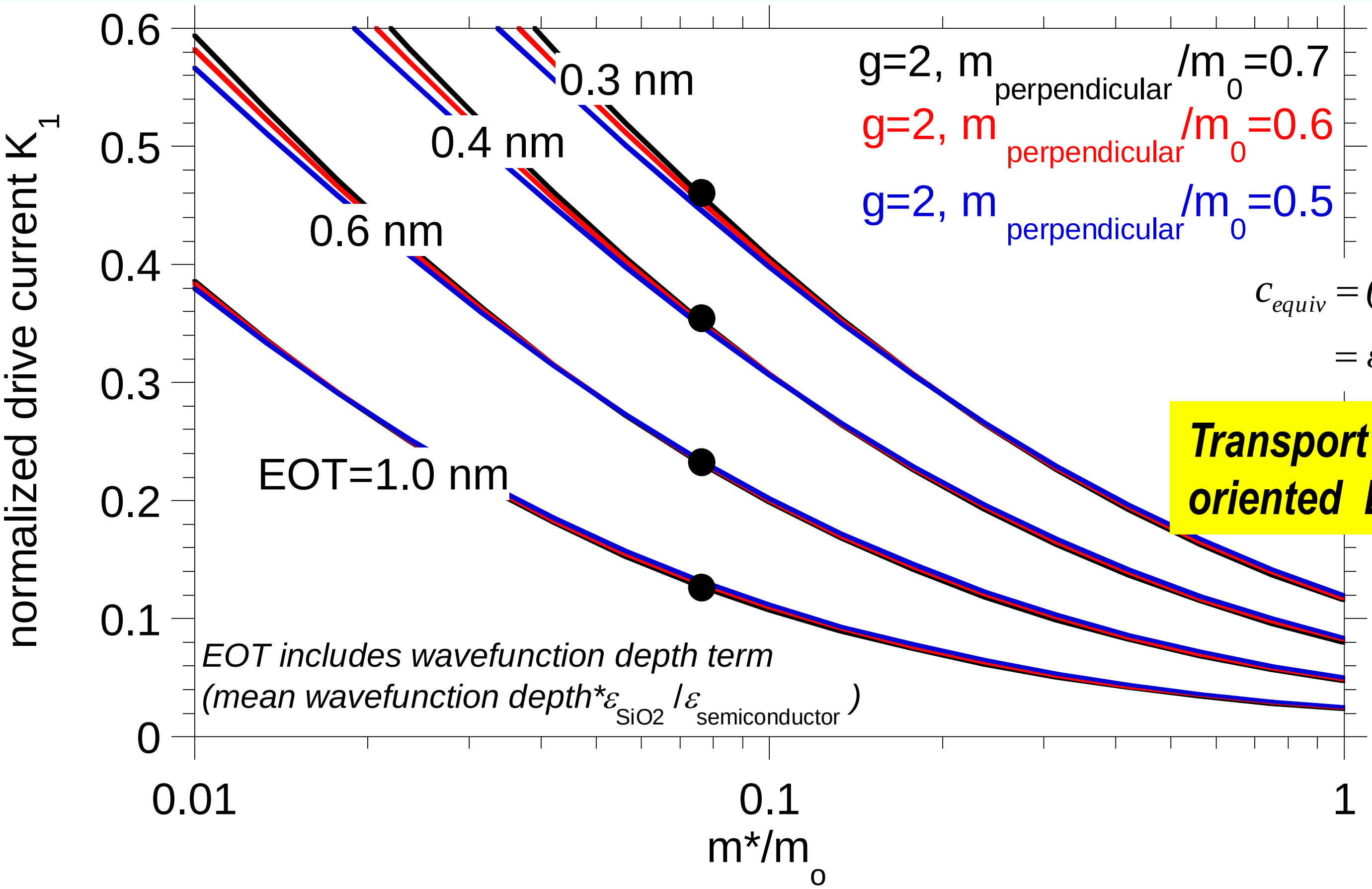
L[1$\bar{1}$1], [$\bar{1}$11]: low vertical mass → depopulate

High in-plane mass parallel to transport → low carrier velocity

Challenge: only moderate energy separation between desired and undesired valleys.

Anisotropic bands, e.g. {110}

$$J = \underline{K_1} \cdot \left(84\frac{\text{mA}}{\mu\text{m}}\right) \cdot \left(\frac{V_{gs}-V_{th}}{1\,\text{V}}\right)^{3/2}, \quad \text{where} \quad \underline{K_1} = \frac{g \cdot (m_\perp^{1/2}/m_o^{1/2})}{\left(1+(c_{dos,o}/c_{equiv}) \cdot g \cdot (m_\perp^{1/2} m_\parallel^{1/2}/m_o)\right)^{3/2}}$$



$$c_{equiv} = (1/c_{ox} + 1/c_{\text{semi}})^{-1}$$
$$= \varepsilon_{\text{SiO}_2}/EOT$$

Transport in {110} oriented L valleys

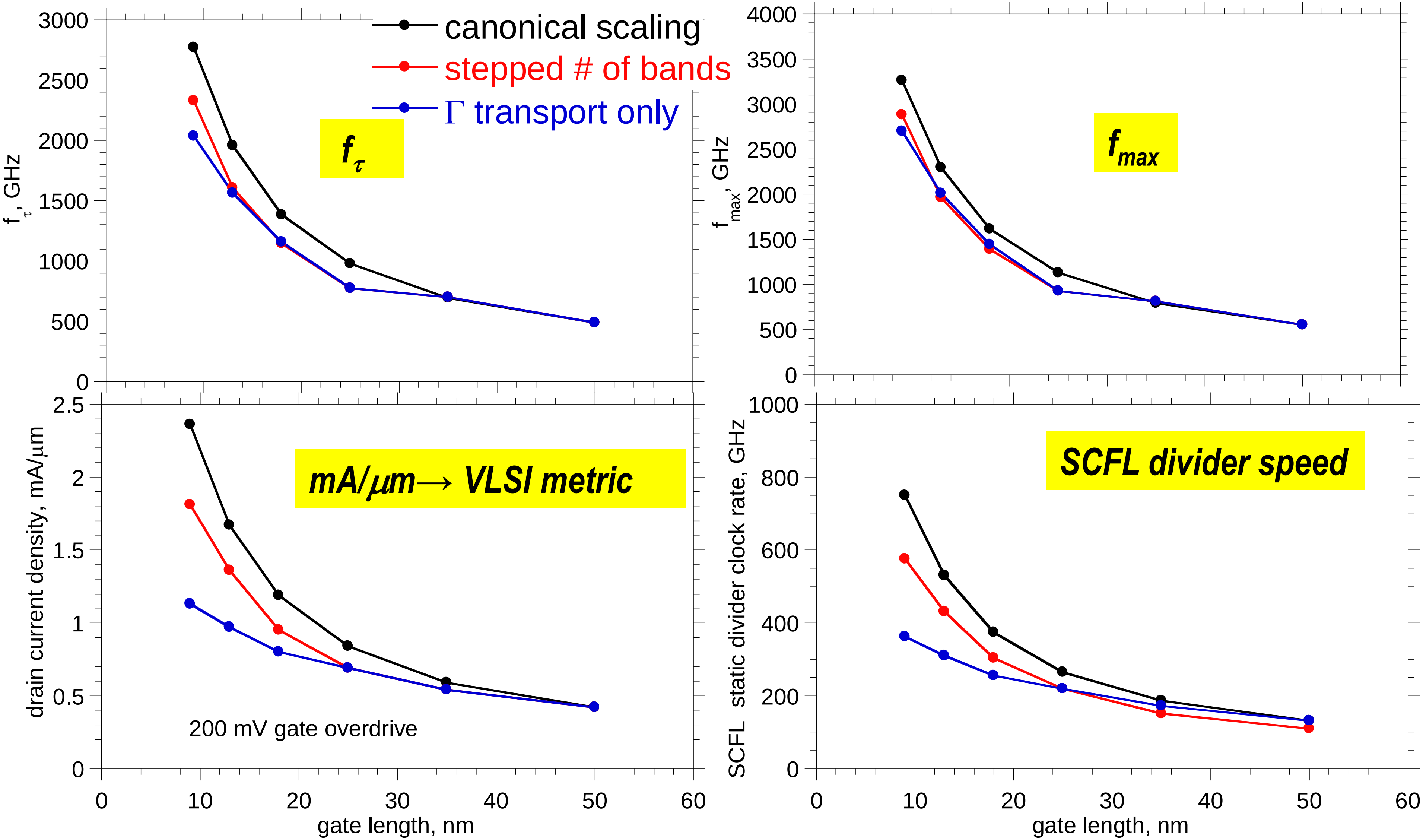
GaAs and Ge {110} MOSFETs with L-valley transport

GaAs: $n = 2, m_t/m_o = 0.075, m_l/m_o = 1.9$ Ge: $n = 2, m_t/m_o = 0.081, m_l/m_o = 1.58$

THz FET scaling: with & without increased DOS

Gate length	nm	50	35	25	18	13	9
Gate barrier EOT	nm	1.2	0.83	0.58	0.41	0.29	0.21
well thickness	nm	8.0	5.7	4.0	2.8	2.0	1.4
S/D resistance	Ω−µm	210	150	100	74	53	37
effective mass	*m_0	0.05	0.05	0.05	0.08	0.08	0.08
# band minima							
canonical		1	1.4	2	2.8	4	5.7
fixed DOS		1	1	1	1	1	1
stepped #		1	1	1	2	3	3

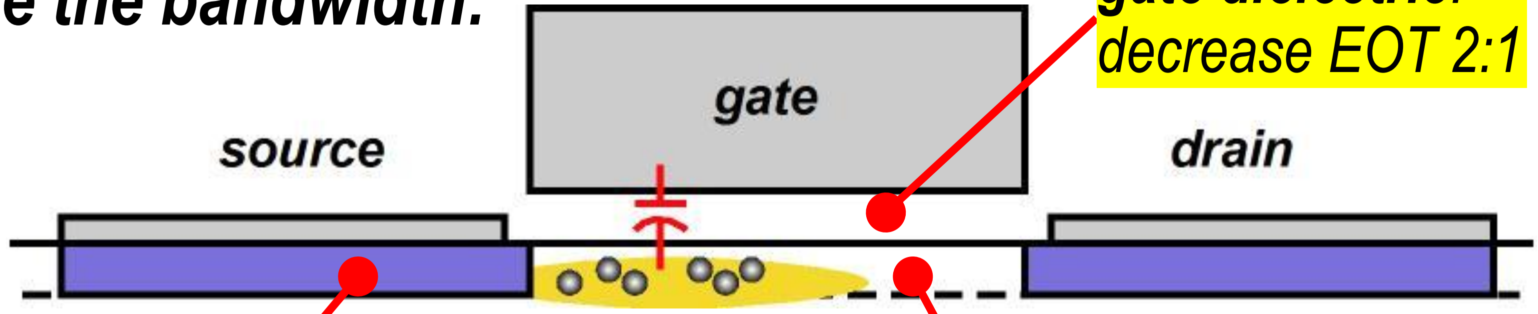
Scaled FET performance: fixed vs. increasing DOS



Increased density of states needed for high drive current, fast logic @ 16, 11, 8 nm nodes

10 nm / 3 THz III-V FETs: Challenges & Solutions

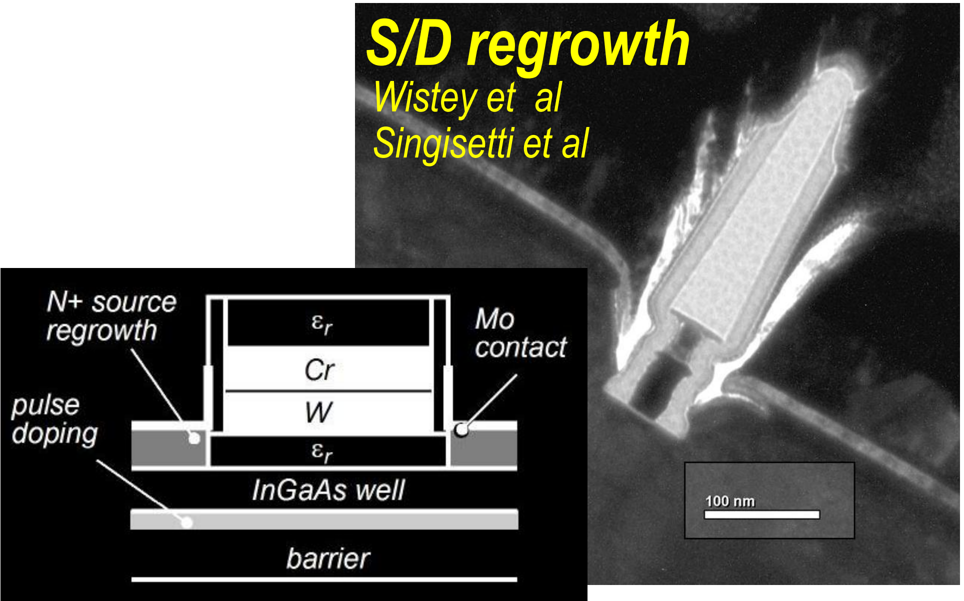
To double the bandwidth:



gate dielectric: *decrease EOT 2:1*

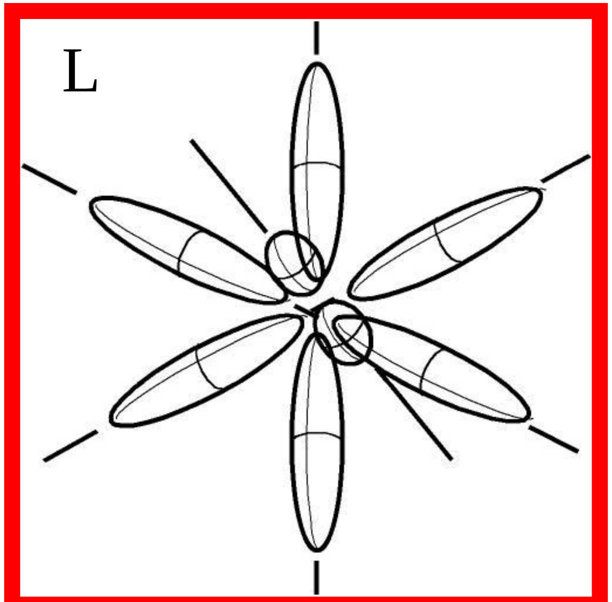
S/D access regions: *decrease resistivity 2:1*

channel: *keep same velocity, but thin channel 2:1 increase density of states 2:1*


S/D regrowth

Wistey et al

Singisetti et al



(end)

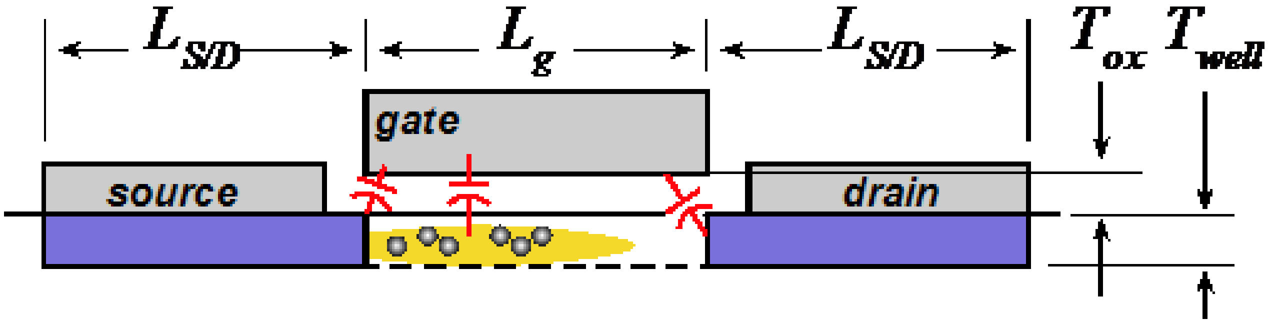
Bandstructure of the [111] AlSb/GaSb triple-QW

Sebastian Steiger
Network for Computational Nanotechnology (NCN)
Electrical and Computer Engineering
steiger@purdue.edu

- Supervised by Profs. Gerhard Klimeck and Timothy Boykin
- Simulation software: OMEN3D by Hoon Ryu and Sunhee Lee
- TB parameters for AlSb and GaSb: Ganesh Hegde and Yaohua Tan

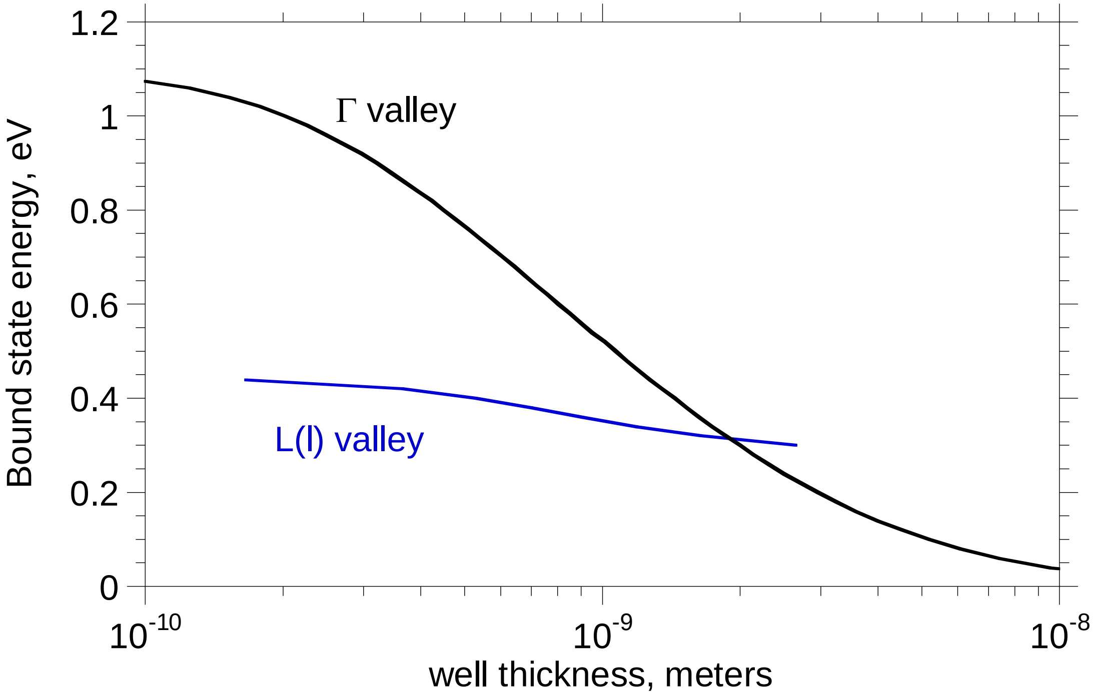
MOSFET Scaling Laws

Constant-voltage / constant-velocity scaling laws:
Changes required for $\gamma : 1$ increased bandwidth in an arbitrary circuit



parameter	law	parameter	law
gate length L_g, source-drain contact lengths $L_{S/D}$ (nm)	γ^{-1}	gate-channel capacitance C_{g-ch} $= [1/C_{ox} + 1/C_{semi} + 1/C_{DOS}]^{-1}$ (fF)	γ^{-1}
gate width W_g (nm)	γ^{-1}	transconductance $g_m \sim C_{g-ch} v_{injection} / L_g$ (mS)	γ^{0}
equivalent oxide thickness $T_{eq} = T_{ox} \varepsilon_{SiO_2} / \varepsilon_{oxide}$ (nm)	γ^{-1}	gate-source, gate-drain fringing capacitances $C_{gs,f} \propto \varepsilon W_g$, $C_{gd} \propto \varepsilon W_g$ (fF)	γ^{-1}
dielectric capacitance $C_{ox} = \varepsilon_{SiO_2} L_g W_g / T_{eq}$ (fF)	γ^{-1}	S/D access resistances R_s, R_d (Ω)	γ^{0}
		S/D contact resistivity R_s / W_g, R_d / W_g ($\Omega - \mu$m)	γ^{-1}
inversion thickness $T_{inv} \sim T_{well} / 2$ (nm)	γ^{-1}	S/D contact resistivity ρ_c ($\Omega - \mu$m^2)	γ^{-2}
semiconductor capacitance $C_{semi} = \varepsilon_{semi} L_g W_g / T_{inv}$ (fF)	γ^{-1}	drain current $I_d \sim g_m (V_{gs} - V_{th})$ (mA)	γ^{0}
DOS capacitance $C_{DOS} = q^2 n m^* L_g W_g / 2\pi\hbar^2$ (fF)	γ^{-1}	drain current density (mA/μm)	γ^{1}
electron density n_s (cm^{-2})	γ^{1}	temperature rise (one device, K)	$\sim W_g^{-1}$

2.0 nm GaAs well, AlAs barriers, on {111} GaAs



2 nm well : Γ and L(l) minima both populated.

$\Gamma: \ m^*/m_o = 0.067 \qquad \mathrm{L(l)}: \ m^*_{\mathrm{lateral}}/m_o = 0.075$

low m^* → high carrier velocity

two band minima → doubles c_{dos}

2 nm well → good electrostatics at ~ 5 - 7 nm L_g.

GaSb well, AlSb barriers, on {110} GaSb