High performance 110 nm InGaAs/InP DHBTs in dry-etched *in-situ* refractory emitter contact technology

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We report a 110 nm InP/$In_{0.53}Ga_{0.47}As$/InP double heterojunction bipolar transistor (DHBT) demonstrating a simultaneous f_t/f_{max} of 465/660 GHz and operating at power densities in excess of 50 mW/μm^2. To our knowledge this is the smallest junction width reported for a III-V DHBT. The narrow 110 nm emitter junction permits the devices to be biased simultaneously at high voltages and high current densities (J_e) with peak RF performance at 41 mW/μm^2 (J_e = 23.6 mA/μm^2, V_{ce} = 1.75 V). Devices incorporate low contact resistance, refractory, *in-situ* Mo emitter contact to a highly doped, regrown InGaAs cap. A low stress, sputter deposited, refractory, dry-etched W/$Ti_{0.1}W_{0.9}$ emitter metal process was developed demonstrating both high emitter yield and scalability to sub-100 nm junctions. Previously reported dry etch processes involving Ti/$Ti_{0.1}W_{0.9}$ metals could not be scaled below 180 nm junction widths due to high metal stress resulting in very low emitter yield [1, 2]. The emitter metal contacts reported here are 100 nm wide and the emitter-base junction width is 110 nm. On-wafer Through-Reflect-Line (TRL) calibration structures were used to measure the RF performance of devices from 140 - 180 GHz.

Lithographic and epitaxial scaling of key DHBT dimensions with improved contact resistivity is critical to achieving THz bandwidths [3]. Specific challenges include fabricating sub-100 nm emitter-base junctions, reducing base and emitter contact resistivity and high current density operation. For the DHBTs reported in this work, the InP emitter has been thinned to 50 nm, enabling an all wet etch process, even for small junction widths. The InGaAs base is 25 nm thick (doping gradient 7–4×10^{19} cm^{-3}) and the InP collector is 100 nm thick. The grade between the InGaAs base and InP collector includes an InGaAs setback, a thin 15 nm InGaAs/InAlAs chirped superlattice grade and InP pulse doping. The epitaxial structure (Table 1) was grown by IQE Inc on a 4" semi-insulating InP substrate. A highly doped InGaAs emitter cap (10 nm thick, $N_d = 5 \times 10^{19}$ cm^{-3}) was grown at UCSB and blanket, *in-situ* Mo contact metal was deposited [4]. A W/TiW (200 nm/300 nm) metal stack was then blanket sputtered. Mo and W/TiW are refractory and should withstand high current densities without contact degradation or electromigration. The stack was etched in the field with SF_6/Ar ICP [1]. The stack was selected to obtain both low stress and vertical etch profile. The vertical emitter metal profile along with undercut at the W/TiW interface acted as the shadow mask for lifted-off base contacts. A dual sidewall process employing 50 and 30 nm sidewalls was used [2]. The emitter semiconductor was completely wet etched. Remaining process features are as in [2].

Transmission Line Model (TLM) measurements show base R_{sh} = 732 Ω/□ and ρ_c = 4 Ω-μm^2 and collector R_{sh} = 12 Ω/□ and ρ_c = 9 Ω-μm^2. Emitter access resistance R_{ex} = 3.6 Ω-μm^2 was extracted from RF data. HBTs with an emitter area A_{je} = 0.11μm × 3.5μm, have DC common emitter current gain β = 18, with common emitter breakdown voltage $V_{BR,CEO}$ = 2.5 V (J_e = 1 kA/cm^2). Kirk effect is observed at J_e = 32 mA/μm^2 (V_{ce} = 1.75 V) when f_t falls to 95% of its peak value. H_{21} reduction from self heating is not significant until 48 mW/μm^2 (J_e = 30 mA/μm^2, V_{ce} = 1.6 V) and the device can be biased without destruction above 55 mW/μm^2.

RF performance of the devices was measured using on-wafer, thin-film microstrip TRL structures for calibration on an Agilent N5242A PNA-X Network Analyzer with Oleson Microwave Labs frequency multiplier heads for 140 - 180 GHz characterization. After calibration, the line and through standards were remeasured and showed a return loss better than -30 and -35 dB, and insertion loss better than -1.5 and -0.1 dB respectively. S_{12} and S_{21} showed less than 2° deviation from linear phase. HBTs embedded in the same calibration environment were then measured. Peak RF performance was obtained at I_c = 9.1 mA and V_{ce} = 1.75V (V_{cb} = 0.7V, J_e = 23.6 mA/μm^2, P = 41.3 mW/μm^2, C_{cb}/I_c = 0.43 psec/V). Extrapolations from -20 dB/dec fit indicate f_t = 465 GHz and f_{max} = 660GHz. DC – 67 GHz measurements were also carried out on a similar sized device with lumped pad structure using off-wafer, probe-tip Line-Reflect-Reflect-Match (LRRM) calibration and parasitic de-embedding on an Agilent E8361A PNA [2]. A small-signal hybrid-π equivalent circuit was extracted from the RF data. In these devices, the current and power densities have increased compared to [1,2] which could be attributed to increased current and heat spreading from the narrower emitters, reduced R_{ex}, and thinner setback and grade layers.

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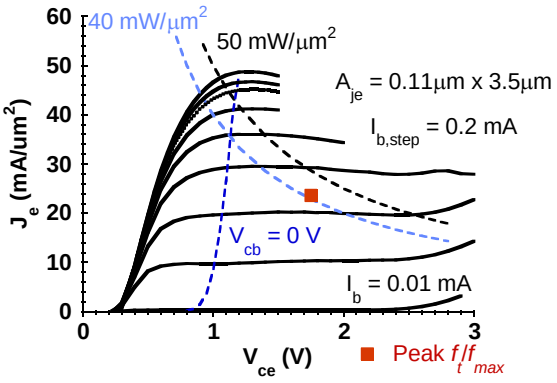

Fig 1: Common-Emitter characteristics (DC *I-V*) of 110 nm DHBT

Thickness	Material	Doping	Comment
10 nm	InGaAs	4×10¹⁹:Si	Emitter Cap
10 nm	InP	4×10¹⁹:Si	Emitter
10 nm	InP	1×10¹⁸:Si	Emitter
30 nm	InP	8×10¹⁷:Si	Emitter
25 nm	InGaAs	7-4×10¹⁹:C	Base
7.5 nm	InGaAs	9×10¹⁶:Si	SetBack
15 nm	InGaAs/InAlAs	9×10¹⁶:Si	Grade
3 nm	InP	5×10¹⁸:Si	Δ-Doping
74.5 nm	InP	9×10¹⁶:Si	Collector
7.5 nm	InP	1×10¹⁹:Si	Sub-Collector
7.5 nm	InGaAs	2×10¹⁹:Si	Sub-Collector
300 nm	InP	2×10¹⁹:Si	Sub-Collector

Table 1: DHBT layer structure

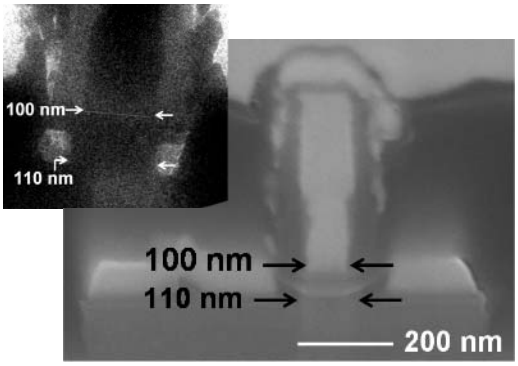

Fig 2: Cross-sectional SEM and TEM of emitter and base mesas of DHBT with 100 nm emitter metal contact and 110 nm emitter-base junction

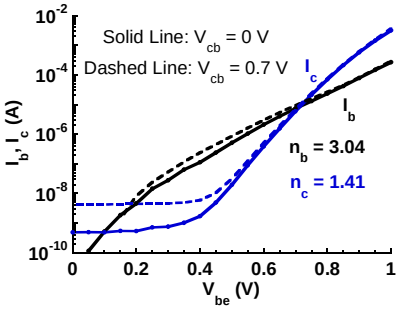

Fig 3: Gummel Plot of 110 nm DHBT

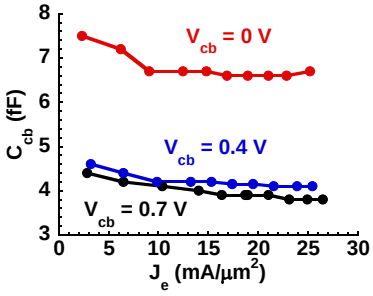

Fig 4: Variation in C_{cb} with V_{cb} and J_e

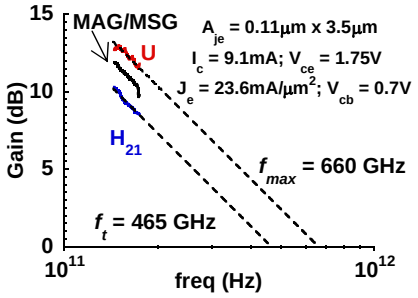

Fig 5: Measured RF gains for peak f_t/f_{max} in 140-180 GHz band using on-wafer microstrip TRL for DHBT with A_{je} = 0.11 μm × 3.5 μm

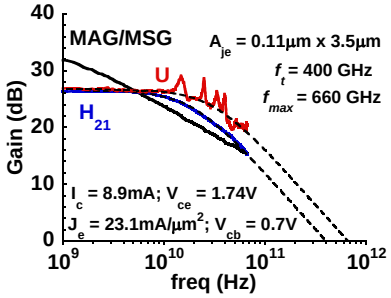

Fig 6: Measured RF gains for peak f_t/f_{max} in DC - 67 GHz band using off-wafer LRRM in a lumped pad structure for DHBT with A_{je} = 0.11 μm × 3.5 μm

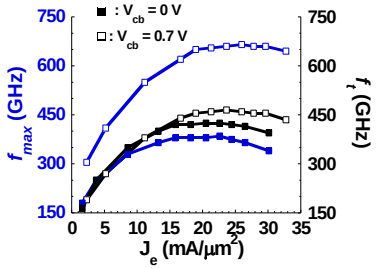

Fig 7: f_t/f_{max} dependence on V_{cb} and J_e for 110 nm DHBT

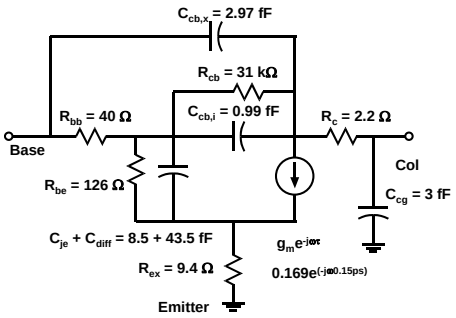

Fig 8: Hybrid-π equivalent circuit at peak RF performance from DC – 67 GHz RF data

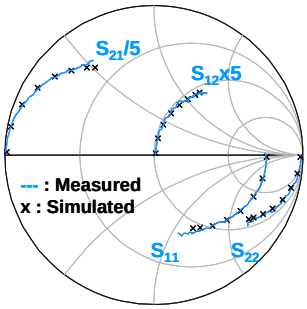

Fig 9: 1 - 67 GHz measured and simulated S-Parameters from equivalent circuit model in Fig 8