A 305–330+ GHz 2:1 Dynamic Frequency Divider Using InP HBTs

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***Abstract*—This letter presents an inductor-loaded 2:1 regenerative frequency divider operating up to 331.2 GHz in an InP HBT process, which, to the best of authors' knowledge, is the fastest frequency divider reported thus far. On-wafer measurement shows that the divider is operating from 304.8 GHz to 331.2 GHz, with output power from −27 dBm to −12.3 dBm (no probe loss correction), while dissipating 85.5 mW from −4.1 V and −3.3 V supplies.**

***Index Terms*—Dynamic frequency dividers, InP heterojunction bipolar transistors (HBT), regenerative frequency dividers.**

I. Introduction

SUBMILLIMETER-WAVE and terahertz (THz) frequency bands covering 300 GHz to 3 THz have applications in security/medical imaging systems, radar, chemical/bio sensors, and high-rate data communications. High-speed frequency dividers are a critical building block for phase-locked loops and frequency synthesis, and present a significant challenge to the implementation of such THz radio systems.

To overcome the bandwidth limitation of static frequency dividers, the use of dynamic frequency dividers has been proposed [1]–[12]. Regenerative dividers up to 168 GHz have been demonstrated in SiGe and HEMT technologies. Clocked-inverter type dividers up to 150 GHz have been reported in an InP HBT technology [12], and injection-locked frequency dividers up to 137 GHz in CMOS technology [11].

In this letter, the design and characterization of a regenerative divide-by-two circuit operating beyond 300 GHz is reported in an InP HBT technology.

II. InP HBT Technology

In this letter, a 0.25 μm emitter width InP HBT technology was used. Circuits were fabricated on 4-inch InP substrates with device layers grown by molecular beam epitaxy. The epitaxy utilized a 30 nm carbon-doped base layer and a 150 nm N-InP collector region. The emitter contact is patterned using electron-beam lithography and formed using an Au-based electroplating process. The HBT IC process includes thin-film resistors (50 Ω/sq), MIM capacitors, and 3-levels of interconnect (M1–M3), with a 10 μm thick BCB layer between M2 and M3. S-parameter measurements of a 4×0.25 μm^2 HBT demonstrated an extrapolated current gain cutoff frequency (f_T) of 375 GHz and an extrapolated maximum frequency of oscillation $(f_{\max})$ of >650 GHz, at $I_C = 9$ mA and $V_{CE} = 1.8$ V.

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III. Design of the Dynamic Frequency Divider

The dynamic frequency divider in this letter is based on a regenerative feedback loop formed by an active mixer [2]. Fig. 1 shows its simplified schematic, where $Q_1 - Q_6$ form a double-balanced active mixer. The mixer output is fed back to its upper-level input $(Q_3 - Q_6)$ via emitter followers $(Q_7 - Q_8)$. The divider input at $\mathrm{RF_{in}}$ at frequency f_{in} is applied to the lower-level mixer input $(Q_1 - Q_2)$. The feedback loop can sustain a stable oscillation at $f_{\mathrm{in}}/2$, under proper amplitude and phase conditions [3]. Even harmonics $(f_{\mathrm{in}}, 2f_{\mathrm{in}}, \ldots)$ are suppressed by the double-balanced mixer, and odd harmonics $(3f_{\mathrm{in}}/2, 5f_{\mathrm{in}}/2, \ldots)$ filtered out by the low-pass characteristics of the loop. At 330 GHz, a quarter wave-length is only 144 μm for $\varepsilon_{r,eff} = 2.5$ (e.g., a 20-μm-long transmission line introduces 12.5° of phase delay). Simple circuit topology is thus preferred to minimize wiring delays.

In previously reported regenerative dividers, either resistors [4]–[7], [9] or trans-impedance stages [2], [8], [10] have been used as a mixer load. In this letter, short transmission lines $(L_1 - L_2)$ are used as an inductive load. This not only yields compact layout, but also increases the maximum divider operating frequency by more than 20%, according to simulation. Inductive loads, however, may limit the divider bandwidth due to reduced loop gain at lower frequencies. L_5 and L_6 provide impedance matching between the lower and upper differential pairs, thus improving the divider input sensitivity. Transmission lines $L_1 - L_4$ were adjusted for optimum divider bandwidth. The divider input and output are single-ended for testing convenience. The unused input port is ac-grounded by a MIM capacitor (C_3), which provides 3 dB lower input power sensitivity compared to a 50-ohm termination. All passive elements and wirings are modeled by either 2.5-D electromagnetic simulations or equivalent circuit models. Bias currents of the mixer core (I_{EE}) and emitter followers (I_{EF}) can be separately adjusted by tuning V_{EE} and V_{EF}.

Inverted-microstrip lines (IMSL) are used for the divider design. A large continuous ground plane in M3 is thus guaranteed, with M1 and M2 available for low-inductance local wiring. With a normal microstrip line structure, ground holes in M1 or M2 are inevitable, which will reduce the divider bandwidth due

TABLE I
COMPARISON OF MILLIMETER-WAVE DYNAMIC FREQUENCY DIVIDERS

Ref. (year)	Type	Technology	Div. Ratio	**Max. operating freq. [GHz]**	Min. operating freq. [GHz]	Power Supply [V]	DC power[1] [mW]	Die area[2] [mm^2]
[4] (2003)	Regenerative	SiGe (f_T = 207G)	2	**100**	14	-3.8	285	-
[5] (2006)	Regenerative	SiGe:C (f_T = 200G)	2	**103**	24	+5.2	195	1×0.5
[6] (2003)	Regenerative	mHEMT (f_T = 220G)	2	**108**	86	-	360	1×0.75
[7] (2003)	Regenerative	SiGe (f_T = 200G)	2	**110**[*]	35	-5	310	0.55×0.45
[8] (2009)	Regenerative	SiGe (f_T = 210G)	2	**136**[*]	74	-3.3	118.8	1.78×0.63
[11] (2009)	Injection locking	65 nm CMOS	2	**137**	128.24	+1.1	5.5[1A]	0.6×0.5
[12] (2003)	Clocked inverter	InP HBT (f_T = 245G)	2	**150**[*]	120	-5.5	357	1.5×1.5
[9] (2006)	Regenerative	SiGe (f_T = 225G)	4	**160**	80	-5.5	650	0.55×0.45
[10] (2009)	Regenerative	SiGe:C (f_T = 215G)	2	**168**	51	+4	105[1B]	0.58×0.48
This work	Regenerative	InP HBT (f_T = 375G)	2	**331.2**	304.8[*]	-4.1 / -3.3	85.5	0.64×0.62

[1] Including power consumption of the output buffer. [1A] Excluding the bias circuit and buffers. [1B] Excluding the interstage buffer.

[2] Including pads.

[*] Measurement limited by available test setup

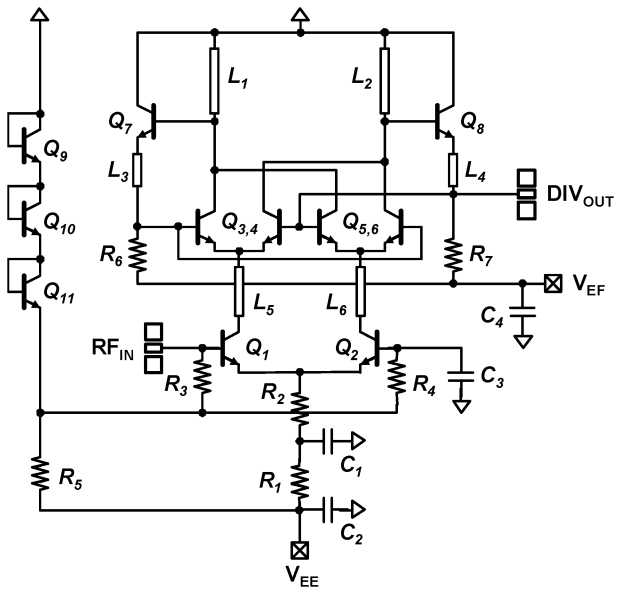

Fig. 1. Simplified schematic of the dynamic frequency divider. All HBTs are $3 \times 0.25\ \mu\mathrm{m}^2$, except for Q_7 and Q_8 whose emitter area is $6 \times 0.25\ \mu\mathrm{m}^2$. Transmission line parameters (L/W) are $L_1 = L_2 = 45\ \mu\mathrm{m}/5\ \mu\mathrm{m}$, $L_3 = L_4 = 25\ \mu\mathrm{m}/2.5\ \mu\mathrm{m}$, and $L_5 = L_6 = 80\ \mu\mathrm{m}/2.5\ \mu\mathrm{m}$. $R_1 = 40\ \Omega$, $R_2 = 100\ \Omega$, $R_3 = R_4 = 250\ \Omega$, $R_5 = 400\ \Omega$, and $R_6 = R_7 = 300\ \Omega$. All bypass capacitors $(C_1 - C_4)$ are radial stubs in a MIM stack with the first series resonance around 320 GHz.

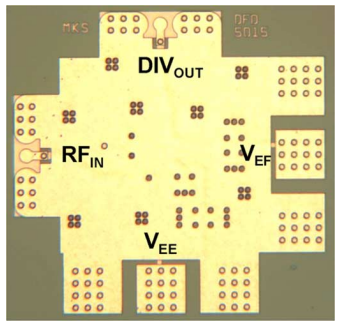

Fig. 2. Chip photograph of the dynamic frequency divider $(640 \times 620\ \mu\mathrm{m}^2)$. The entire circuit area is covered by a continuous M3 ground plane.

Fig. 3. On-wafer divider test setup. GGB waveguide probes were used.

to extra ground inductances. For compact layout, narrow lines $(W \leq 5\ \mu\mathrm{m})$ are exclusively used except for the output 50-ohm lines $(W = 16\ \mu\mathrm{m})$, at the cost of slightly higher line losses (~2 dB/mm at 320 GHz). An IMSL-to-pad transition is designed for low insertion loss $(S_{21} \approx -1\ \mathrm{dB})$ across the full divider bandwidth.

Simulation shows that the divider is operating from 270 GHz to 340 GHz at an input power of $P_{\mathrm{in}} = 0\ \mathrm{dBm}$ (single-ended). Initial HBT models used in the design cycle were based on projected transistor performance determined from the transistor geometry and epitaxy design. After fabrication, the HBT models were revised to match measured transistor data, and these models were used to re-simulate the divider (Section IV). The divider chip photo is shown in Fig. 2.

IV. MEASUREMENT RESULTS

The frequency divider was characterized using the on-wafer test setup shown in Fig. 3. The divider input is driven by a WR-3 diode multiplier module from Virginia Diodes, Inc. The output of the divider is measured by a spectrum analyzer with a WR-5 harmonic mixer from OML, Inc.

The divider is biased at $V_{EE} = -4.1\ \mathrm{V}$ $(I_{EE} = 9.1\ \mathrm{mA})$ and $V_{EF} = -3.3\ \mathrm{V}$ $(I_{EF} = 14.6\ \mathrm{mA})$, consuming 85.5 mW of dc power (P_{dc}). The divider input frequency (f_{in}) was swept from 302 GHz to 340 GHz, and the resulting divider output power (P_{out}) is plotted in Fig. 4. Output power from the diode multiplier module was separately characterized, and superimposed on the same plot as divider input power (P_{in}). The measured divider bandwidth is from $f_{\mathrm{in}} = 304.8$ GHz to 331.2 GHz, with

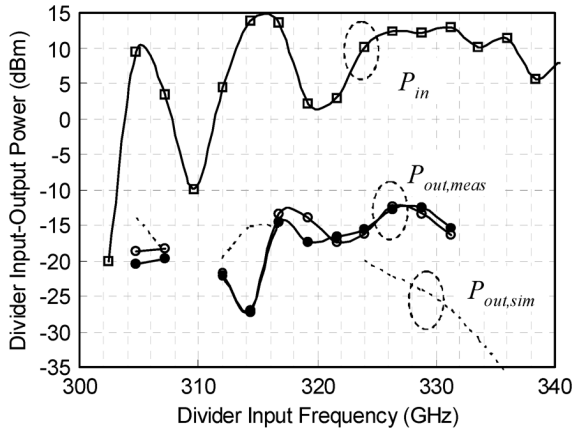

Fig. 4. Measured divider input and output power (no probe loss correction) from two samples at $V_{EE} = -4.1$ V ($I_{EE} = 9.1$ mA) and $V_{EF} = -3.3$ V ($I_{EF} = 14.6$ mA). Input and output probe losses are expected to be 3 dB and 2.1 dB, respectively. The input power level is insufficient to drive the divider below 303 GHz and around 310 GHz. Note $P_{\rm in}$ represents the nominal output power from the diode multiplier module, not the divider *sensitivity*.

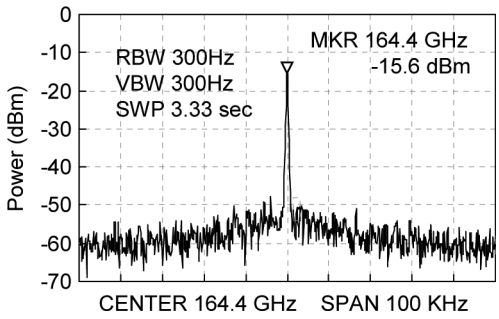

Fig. 5. Measured spectrum of the divider output with $f_{\rm in} = 328.8$ GHz.

P_{out} from -27 dBm to -12.3 dBm. The divider is not functional below 303 GHz and at the vicinity of 310 GHz, due to insufficient input power ($P_{\rm in} < -10$ dBm). Simulated divider output power is also shown in Fig. 4, where the measured $P_{\rm in}$ curve was used. Note reference planes are at waveguide interfaces, so probe losses are not de-embedded. Input (WR-3) and output (WR-5) probe losses are expected to be 3 dB (from manufacturer's data) and 2.1 dB (from a thru-line measurement), respectively. Fig. 5 shows a typical spectrum of the divider output with $f_{\rm in} = 328.8$ GHz. The signal peak passes the built-in "Signal Identification" check of the spectrum analyzer, across the entire divider bandwidth, confirming that the observed peak is at $f_{\rm in}/2$, not at $f_{\rm in}/2 \pm m f_{LO}$ (f_{LO}: local oscillator frequency of the harmonic mixer). The divider P_{out} was measured as a function of bias I_{EE} and I_{EF} (Fig. 6). The divider reaches its full output power for $I_{EE} \geq 8$mA and $I_{EF} \geq 12$ mA, and remains operating under a wide range of bias currents. No self-oscillation or spurious tones were observed during measurement. Table I compares recently reported dynamic frequency dividers operating at or above 100 GHz.

V. Conclusion

We have presented an InP-HBT dynamic frequency divider operating from 304.8 GHz to 331.2 GHz at $P_{dc} = 85.5$ mW,

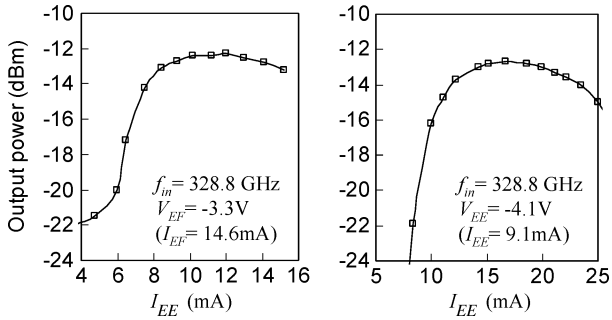

Fig. 6. Divider output power as a function of bias: sweeping mixer-core (I_{EE}, left) and emitter-follower current (I_{EF}, right).

designed toward a fully-integrated THz radio and mixed-signal systems. Lack of available RF sources prevents divider testing below $f_{\rm in} = 303$ GHz. To the best of authors' knowledge, the presented divider is almost twice as fast as the previous state-of-the-arts, at similar or reduced dc power consumption.

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