A 220-225.9 GHz InP HBT Single-Chip PLL

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***Abstract*—We present a 220 GHz fundamental PLL, based on a 220 GHz VCO, 2:1 dynamic frequency divider, fifth-order sub-harmonic phase detector, active loop filter, and output amplifier, fabricated in an InP HBT technology. The measured PLL locking range was 220.0 to 225.9 GHz, with -83 dBc/Hz of phase noise at a 100 KHz offset, with 465.3 mW of dc power consumption. The PLL occupies 1.1 mm^2 including pads.**

***Index Terms* — Phase-locked loops, hetero-junction bipolar transistors, dynamic frequency dividers, voltage controlled oscillators.**

I. Introduction

Sub-millimeter-wave and terahertz (THz) frequency bands covering 300 GHz to 3 THz have applications in security/medical imaging systems, radar, chemical/bio sensors, and high-rate data communications. Phase-locked loop (PLL) circuits provide a coherent local oscillator (LO) signals for frequency up/down-conversion, and are a critical building block for future high-performance THz systems.

Millimeter-wave PLLs have been demonstrated up to 164 GHz [1-5] in advanced SiGe or CMOS technologies. Recently, a 300 GHz PLL has been developed by the authors using InP HBT process [6], with 0.36 GHz of locking range and -23 dBm of output power. This paper presents a 220 GHz PLL design with an improved locking range and higher output power.

II. InP HBT Technology

InP double hetorojunction bipolar transistors (DHBTs) offer high transistor bandwidth with high voltage handling due to the use of a wide bandgap InP collector. In this work, circuits were fabricated on 4-inch semi-insulating InP substrates with device layers grown by molecular beam epitaxy. The epitaxy utilizes a 30 nm carbon-doped base layer and a 150 nm N-InP collector region. The emitter contact is patterned using electron-beam lithography and formed using an Au-based electroplating process. In this work, the nominal emitter junction width was 0.25 µm. A thin (< 100 nm) emitter semiconductor stack minimizes undercut during the self-aligned emitter mesa etch. Dielectric sidewall spacers are formed to passivate the base-emitter junction and permit the formation of a self-aligned base contact. After base-contact deposition, the remaining HBT process flow follows that of a standard mesa-HBT process. The transistors are passivated

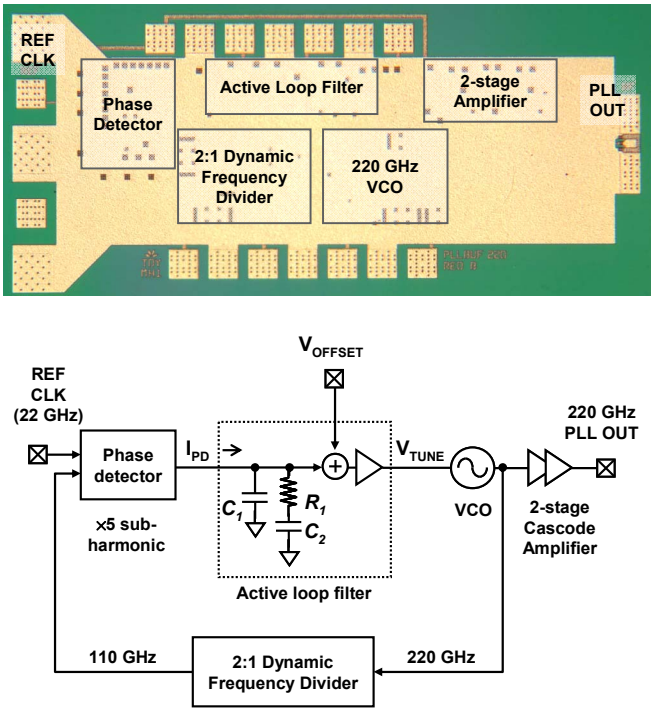

Fig. 1. 220 GHz InP HBT PLL: chip photograph (top) and block diagram (bottom). Chip size: 1,570×700 µm^2.

with a spin-on-dielectric (Benzocyclobutene, BCB), and a planarization etch is used to expose the emitter post. Device vias are opened to the remaining HBT contacts and first-level interconnects are formed using electroplated gold.

The HBT IC process includes thin-film resistors (50 Ohm/sq), MIM capacitors, and 4-levels of interconnect (M1-M4). A 1 µm thick BCB layer is used between metal layers. S-parameter measurements of transistors were performed from 1-110 GHz and RF figures-of-merit were extracted from these measurements. A 4×0.25 µm^2 HBT demonstrated an extrapolated current gain cutoff frequency (f_T) of > 350 GHz and an extrapolated maximum frequency of oscillation (f_{max}) of > 650 GHz, at I_C = 10 mA and V_{CE} = 1.8 V. Transistors have demonstrated common-emitter breakdown voltages (BV_{CEO}) of > 4V. Large-signal Agilent HBT models have been extracted. Compared to standard silicon BJT model (i.e. Gummel-Poon or

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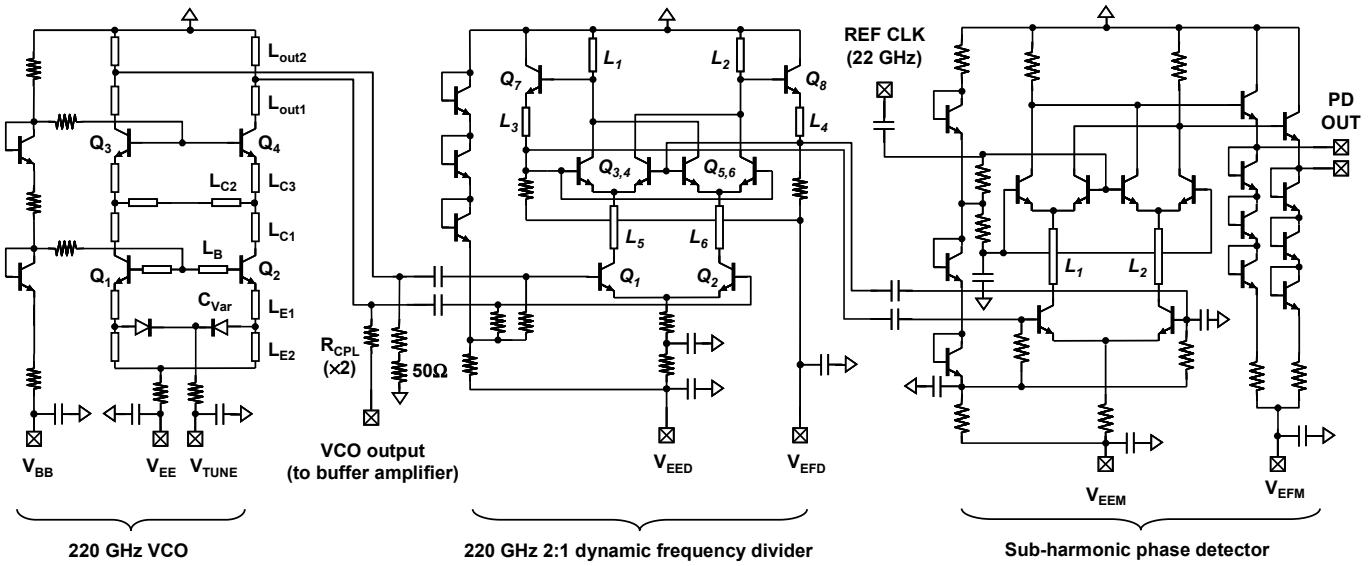

Fig. 2. Simplified schematic of the VCO, frequency divider, and phase detector.

VBIC), the Agilent model is better suited to capture some characteristics that are unique to III-V DHBTs such as collector current blocking and collector velocity modulation.

III. PLL Design

The authors' previous PLL design [6] demonstrated the first fundamental PLL operation at 300 GHz, but its low output power (-23 dBm) and narrow locking range (0.36 GHz) may limit its practical use. For the design of the 220 GHz PLL presented in this paper, several design changes and improvements were made. First, a 2-stage cascode amplifier is used to boost the PLL output power to -1 dBm, while allowing the dynamic frequency divider still receiving full oscillator power with > 3 dB input sensitivity margin. Second, the gain of the active loop filter is increased by 12 dB, generating a 4× larger swing at the VCO tuning port, thus increasing locking range. Third, the unused reference clock input port of the (differential) phase detector is terminated with a properly sized MIM capacitor (previous 300 GHz design used an improperly sized capacitor), which enhances phase detector gain with a single-ended reference clock input.

A chip photograph of the PLL IC is shown in Fig. 1. All the sub-circuits of the PLL IC are implemented using inverted microstrip lines to utilize a continuous ground plane on a top metal layer. Description of individual building blocks follow.

A. Voltage-Controlled Oscillator (VCO)

In this work, a series-tuned differential VCO is used [6,7], as shown in Fig. 2. Q_1-Q_2 form the oscillator core, and a common-base amplifier (Q_3-Q_4) provides power gain and isolation from load perturbation, while re-using the same bias current. C_{VAR} is a single finger base-collector (B-C) junction at reverse bias with expected Q~15 at 220 GHz. The differential topology makes oscillator operation insensitive to common-mode impedances, e.g. bias lines and grounding via inductance, thus tolerant to modeling uncertainties and errors. The VCO provides 0 dBm of single-ended power across > 8 GHz of tuning range, while consuming 95 mW. The VCO output is tapped by a simple 18 dB resistive coupler (R_{CPL}), and the output amplifier restores the PLL output power level to -1 dBm.

B. Dynamic Frequency Divider

Due to the bandwidth limitation of static frequency dividers, dynamic frequency dividers have been used for millimeter-wave PLLs up to 100 GHz, e.g. regenerative ("Miller") frequency dividers [1][2] or injection-locked frequency dividers [3][5]. In this work, a regenerative 2:1 dynamic frequency divider is employed [6][8], as shown in Fig. 2. The use of inductive loading (L_1-L_2) enables higher frequency operation than is possible with traditional resistive or transimpedance-stage loading, with less voltage headroom. According to simulation, the divider operating bandwidth is > 40 GHz centered at 220 GHz, with -25 to -15 dBm of output power, while consuming 91 mW.

C. Phase Detector

In order to perform phase comparison at a reasonably low frequency, a 5th-order sub-harmonic phase detector is used in this work [6], in favor of its simpler construction and lower power consumption compared to a chain of static frequency dividers. Fig. 2 shows schematic of the sub-harmonic phase detector based on a double-balanced mixer, where the 22 GHz reference clock and 110 GHz divider output are applied to the upper and lower differential pairs, respectively. Transmission lines L_1 and L_2 improve impedance matching between the upper and lower differential pairs at 110 GHz, thus enhancing phase detector gain. Simulation shows that the phase detector provides useful detection gain up to N = 5 sub-harmonic operation with -20 dBm of RF power at 110 GHz. Detector

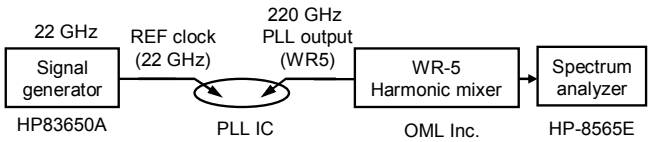

Fig. 3. PLL test setup.

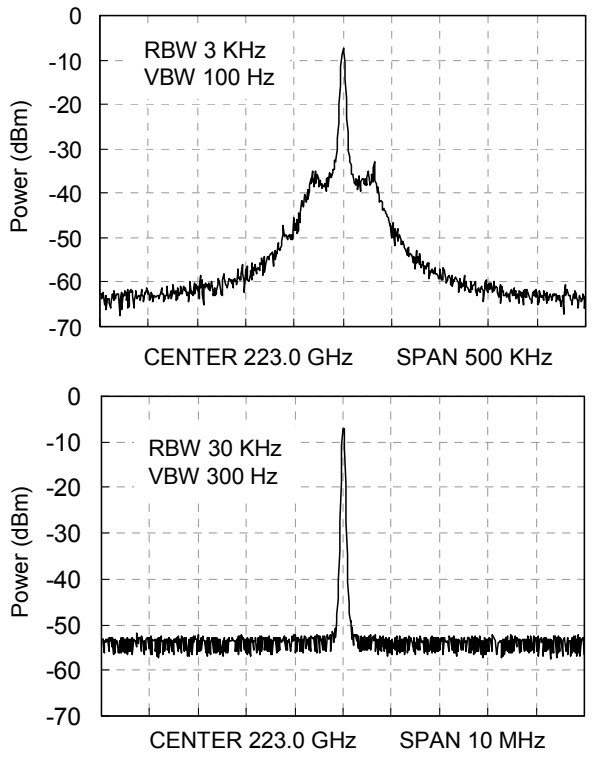

Fig. 4. Measured PLL output spectrum after down-conversion by a WR-5 sub-harmonic mixer, 500 KHz span (top) and 10 MHz span (bottom). Output power level is uncalibrated.

operation at $N > 5$ may suffer from increased sensitivity to detector offset voltages and may degrade PLL phase noise.

D. Active Loop Filter

A conventional lag-lead filter is used (Fig.1), which results in a 2nd-order PLL. The loop bandwidth is 150 MHz, determined from the intersection of the VCO phase noise and frequency-multiplied reference clock (22 GHz) phase noise skirts. This approach results in a low phase noise PLL, since the PLL output phase noise will follow the lower of the two. To ensure stability in the presence of process and temperature variations, the loop is designed with a sufficient phase margin (80 deg), accounting for extra phase shifts (~10 deg) from higher-order poles such as interconnect delays and the RC time-constant from varactor bias circuit.

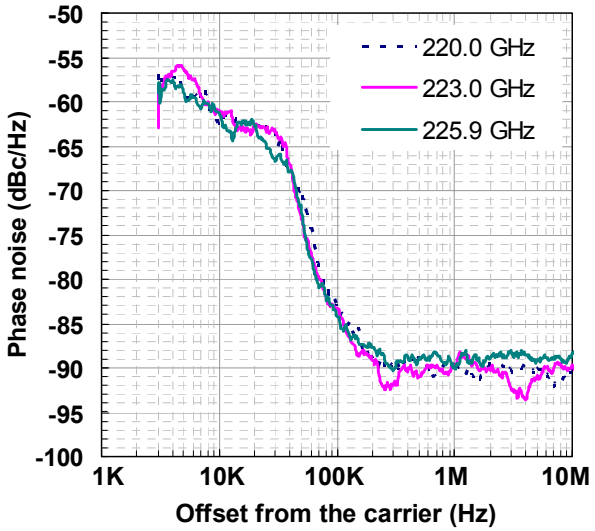

Fig. 5. Measured phase noise of the PLL output (4% of spectral averaging). Beyond 300 KHz, measurement is limited by the spectrum analyzer noise floor.

E. Output Amplifier

A 2-stage differential cascode amplifier is used as a PLL output amplifier to obtain -1 dBm of output power (including pad transition loss), while consuming 160 mW. The interface between the VCO and output amplifier is single-ended to simplify top-level layout, with the unused input port ac-terminated. For testing convenience, the PLL output is also single-ended, with the unused output port terminated with a 50-ohm on-chip load.

IV. Measurement Results

The fabricated PLL IC was characterized on-wafer using the test setup outlined in Fig. 3. The 220 GHz PLL output was down-converted by a WR-5 sub-harmonic mixer (OML Inc.), and was subsequently measured by a spectrum analyzer.

A typical PLL output spectrum is shown in Fig. 4. Note that the output power level in Fig. 4 is uncalibrated, mainly due to the saturation of the WR-5 harmonic mixer with a relative high input power. Accurate power measurements using a separate power meter are currently under way. Phase noise measurements were performed using the spectrum analyzer's built-in utility routine for offset frequencies from 3 KHz to 30 MHz. The measured phase noise was -61 dBc and -83 dBc, at the offset frequencies of 10 KHz and 100 KHz, respectively (Fig. 5). Beyond a 300 KHz offset, phase noise measurement is limited by the spectrum analyzer noise floor. The measured PLL locking range was from 220.0 to 225.9 GHz. The PLL consumes 465.3 mW of dc power. Measurement from a separate VCO breakout circuit shows that the VCO has > 8 GHz of tuning range centered around 220 GHz.

V. CONCLUSION

A 220 GHz single-chip PLL in InP HBT technology is presented, demonstrating a wider locking range (5.9 GHz) and higher output power (estimated to be -1 dBm) compared to the authors' previous design at 300 GHz [6]. All the PLL building blocks are integrated on-chip including bias circuits. Accurate measurements of the PLL output power are currently under way. Table. I compares recently published mm-wave PLL ICs.

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Table I. Comparison of recently reported millimeter-wave PLLs

	This work	[6]	[1]	[2]	[3]	[4]	[5]
Frequency [GHz]	**220.0–225.9**	300.76–301.12	162–164[A] 86–92 81–82	91.8–101[A] 45.9–50.5	95.1–96.5	79.4	73.4–73.72
Locking Range [GHz]	**5.9**	0.36	2 / 6 / 1	9.2 / 4.6	1.4	-	0.32
Technology	**InP HBT**	InP HBT	0.13μm BiCMOS	0.13μm CMOS	65nm CMOS	SiGe	90nm CMOS
Divide ratio [f_{VCO}/f_{REF}]	**10**	10	16,32, 64,128	512	256	64	32
Phase noise @100KHz [dBc/Hz]	**-83**	-78	-78.9 @163GHz -93.8 @90GHz	-63.5 (50KHz offset)	-75.2 to -75.86 (1MHz offset)	-81	-88
Supply voltage [V]	**-4.3, -5.0**	-4.3, -5.0	1.8, 2.5, 3.3	1.5, 0.8	1.2, 1.3	5.5	1.45
P_{OUT} [dBm]	**-1 (estimate)**	-23	-25 @163GHz 3 @90GHz	-10 @50GHz -31 to -22 @100GHz	-	-	-
P_{DC} [mW]	**465.3**	301.6	1,150 to 1,250	57	43.7	-	88[B]
Chip area [mm^2]	**1.57×0.7**	1.38×0.61	1.1×1.7	1.16× 0.75	1× 0.7	-	1×0.8

[A] Second-order harmonic [B] Excluding output buffers