InP HBT IC Technology for Terahertz Frequencies: Fundamental Oscillators Up to 0.57 THz

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***Abstract*—We report on the development of a 0.25-μm InP HBT IC technology for lower end of the THz frequency band (0.3–3 THz). Transistors demonstrate an extrapolated $f_{\max}$ of $>$800 GHz while maintaining a common-emitter breakdown voltage (BVCEO) $>$4 V. The transistors have been integrated in a full IC process that includes three-levels of interconnects, and backside processing. The technology has been utilized for key circuit building blocks (amplifiers, oscillators, frequency dividers, PLL, etc), all operating at $\geq$300 GHz.**

Next, we report a series of fundamental oscillators operating up to 0.57 THz fabricated in a 0.25-μm InP HBT technology. Oscillator designs are based on a differential series-tuned topology followed by a common-base buffer, in a fixed-frequency or varactor-tuned scheme. For $\geq$400 GHz designs, a subharmonic down-conversion mixer is integrated to facilitate spectrum measurement. At optimum bias, the measured output power was -6.2, -5.6, and -19.2 dBm, for 310.2-, 412.9-, and 573.1-GHz designs, respectively, with $P_{\rm DC} \leq$ 115 mW. Varactor-tuned designs demonstrated 10.6–12.3 GHz of tuning bandwidth up to 300 GHz.

***Index Terms*—InP HBT, millimeter-wave oscillators, MMIC oscillators, terahertz, TMICs, voltage-controlled oscillators.**

I. Introduction

INDIUM PHOSPHIDE (InP)-based high electron mobility transistors (HEMTs) and heterojuction bipolar transistors (HBTs) have attained the highest reported transistor bandwidths, with power gain cutoff frequencies (f_{max}) approaching or exceeding 1 THz [1]–[3]. Taking advantage of these record bandwidths, integrated circuits have recently been demonstrated in the submillimeter-wave and terahertz frequency bands (0.3–3 THz) [4]–[6], frequency regimes that were previously accessible only with two terminal devices such as Schottky diodes. Terahertz monolithic integrated circuits (TMICs) based on HEMT and HBT technologies will enable new and emerging applications in imaging, radar, spectroscopy, and communications.

Compared with InP HEMTs, double-heterojunction bipolar transistors with wide-bandgap InP collectors offer a higher breakdown voltage at a given current-gain cutoff frequency (f_t). InP HBTs have also demonstrated the highest reported bandwidths for digital circuit building-block static frequency divider circuits operating at $>$200 GHz [7], [8]. Further, at frequencies approaching a significant fraction of the transistor bandwidth, input shot noise no longer dominates the transistor noise characteristics, and InP HBTs operated at 10%–20% of their peak current density should have comparable noise figure to HEMTs of similar bandwidth. These characteristics make the HBT technology capable of realizing all necessary transmit and receive components (e.g., LNA, mixer, local-oscillator VCO/PLL, etc) in a single IC platform. Single-chip THz transmitters and receivers will eliminate lossy waveguide interconnects and transitions and permit the construction of receiver arrays with single-wavelength element spacing.

In addition to wide-bandwidth transistors, a TMIC technology requires a compact low-loss interconnect environment, wafer thinning and through-wafer vias for substrate mode control, and methods for efficiently coupling THz signals on to and off of the wafer. In this paper, we first describe the development of the various technical aspects of a 0.25-μm InP HBT TMIC technology [1].

A key element in THz radio systems is a compact, tunable signal source with sufficient output power level as a local oscillator (LO). Oscillator circuits can be specially designed for increased signal power at harmonics enabling RF power generation at close to or beyond the transistor f_{max} [9]–[15]. When the device f_{max} is sufficiently high, fundamental oscillators are generally preferred, since they are simpler and more power-efficient than harmonic-based oscillators, with no need of eliminating subharmonic outputs.

Fundamental oscillators up to 346 GHz have been demonstrated in an HEMT technology [16], [17], producing 0.27 mW at 330.56 GHz [18], and a fundamental InP HBT oscillator has been reported operating at 311 GHz [19]. These previously

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reported fundamental oscillators were single transistor circuits where the transistor was reactively tuned to be unstable. In CMOS technology, a 300-GHz fundamental oscillator has been recently reported [20].

In the latter part of this paper, we report on a series of fundamental oscillator designs with an integrated output buffer and bias circuitry operating up to 0.57 THz, extending our previous oscillator results [5]. For ≥400-GHz oscillator designs, integrated down-conversion mixers facilitate output spectrum measurement.

Sections II and III describe the 0.25-μm InP HBT process technology and its wiring environment including backside processing, respectively. In Section IV, design approaches and basic tradeoffs are discussed for the oscillator design. Measurement results from two HBT process runs are presented in Section V.

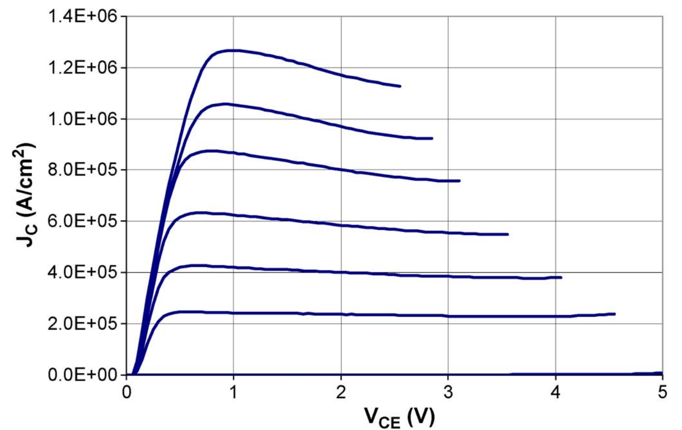


Fig. 1. Measured common-emitter IV characteristics of a 0.25×4 μm^2 HBT.

II. InP HBT Technology

General scaling laws for increasing the bandwidth of InP HBTs have been developed and outlined in [21]. Structurally, to increase the HBT bandwidth, one must vertically scale the transistor epitaxy and laterally scale the transistor junction dimensions. Operating current densities are increased as the square of the increase in transistor bandwidth, and the emitter junction dimensions must be decreased by the same ratio to maintain an acceptable junction temperature rise. Scaling of junction dimensions requires commensurate improvements in the emitter and base ohmic contact resistivities. A key technological challenge in obtaining InP HBTs with THz bandwidths is obtaining sufficiently low n-type and p-type ohmic contact resistivities in self-aligned process flows. These process flows must also maintain high yield as the transistor dimensions are scaled.

In this work, two generations of 0.25-μm HBT technologies have been used for IC designs: *THzIC1* and *THzIC2*. Improvement in the epitaxy and transistor layout of the *THzIC2* process resulted in a decrease of both the extrnisic emitter resistance and extrinsic base-collector capacitance by a factor of ~2 compared with the *THzIC1* technology. As a result, higher frequency transistor performance and thus higher oscillator operation frequencies were obtained.

A. HBT Technology

The HBTs are fabricated on 4-in InP substrates and epitaxial layers are grown by molecular beam epitaxy. The 0.25-μm technology described here utilizes a 30-nm carbon-doped base layer with 50 meV of compositional grading to reduce base transit time. The total N-collector thickness is 150 nm, and the base-collector junction design has been optimized to support high current density operation (> 10 mA/μm^2) [22].

Electron-beam lithography is used to define a 0.25-μm emitter contact. The contact is formed using an Au-based electroplating process [23]. After plating, a combination dry/wet etch process is used to form the emitter mesa. A thin emitter semiconductor stack (<80 nm) minimizes lateral undercut in wet etch steps. Dielectric sidewall spacers are then formed on the emitter contact using a conformal dielectric deposition followed by an anisotropic dry etch. The sidewalls passivate the base–emitter junction and facilitate the formation of a self-aligned base contact. I-line photolithography is used for all process steps after the emitter contact and the remaining process flow follows that of a standard triple-mesa HBT, with particular attention paid to minimizing the transistor parasitic capacitances. Further details of the technology can be found in [24].

B. HBT Characteristics

Fabricated HBTs demonstrate a dc beta (β) of approximately 25 and a common emitter breakdown voltage of >4.0 V ($J_E = 10$ μA/μm^2). The transistors support high current and power densities. This is illustrated in the common-emitter IV characteristics (Fig. 1) that show the transistor operating at current densities of >10 mA/μm^2, and power densities of >20 mW/μm^2.

Fig. 2 shows the measured RF power gains of a 0.25×4 μm^2 HBT in the *THzIC2* process biased for peak RF performance. S-parameter measurements were performed on-wafer to 50 GHz. An LRRM calibration was performed using a commercial calibration substrate, and pad parasitics were deembedded from the measurements using open and short test structures. The maximum current gain cutoff frequencies (f_t) and maximum power gain cutoff frequencies ($f_{\max}$) are extracted from least-squares fits to single-pole transfer functions of the measured H_{21} and unilateral power gain (U), respectively. The extrapolated f_t and $f_{\max}$ of the transistor are 392 and 859 GHz, respectively, at a bias condition of $V_{\text{CE}} = 1.8$ V and $I_C = 13$ mA.

Accurate transistor measurements at THz frequencies (>300 GHz) are difficult due to the small transistor parasitics and challenges in obtaining accurate on-wafer calibrations due to spurious modes generated in an on-wafer wiring environment. Transistor models are therefore extracted from low frequency measurements (typically to 50 GHz).

The Agilent III-V HBT model [25] is used for large-signal modeling of our InP HBTs. The model is capable of capturing many of the unique properties of III-V bipolar transistors that cannot be modeled with standard silicon BJT models. These properties include: collector transit time modulation with applied bias, collector–base capacitance cancellation, and base–collector current blocking at high collector currents. The model includes all relevant transistor parasitic elements and

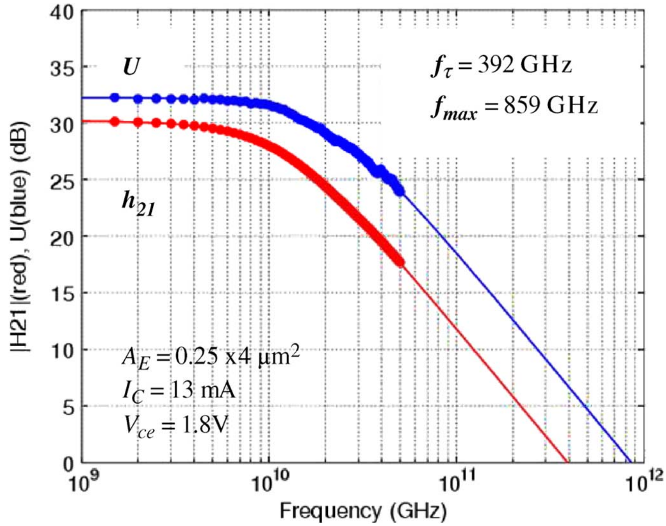


Fig. 2. Measured short circuit current gain (H_{21}) and unilateral power gain (U) of a 0.25 μm InP HBT.

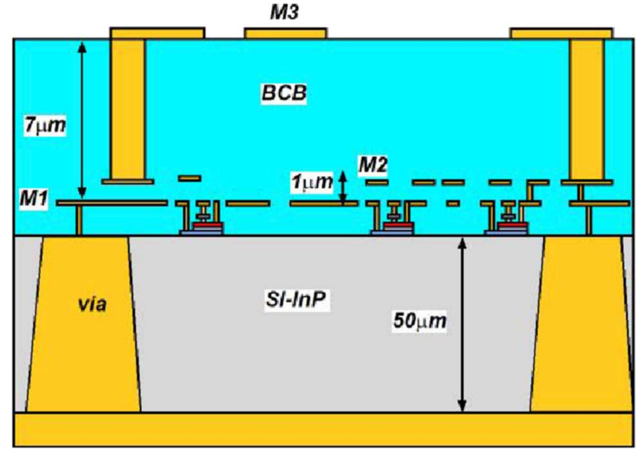


Fig. 3. Schematic cross section of InP HBT IC thin-film wiring environment

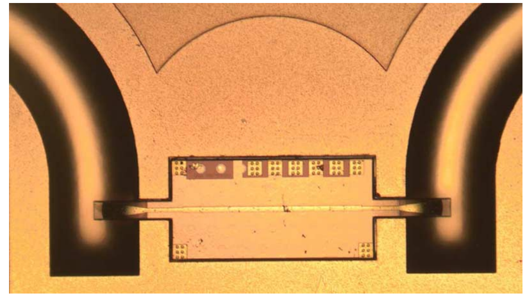


Fig. 4. A 220–325 GHz thru-line test chip in a silicon waveguide block. Integrated waveguide probes are formed after backside-etch singulation process. Chip dimensions are $1000 \times 500\ \mu m^2$.

should scale well to frequencies approaching the transistor cutoff frequencies; an assertion that is supported by the good agreement that we have observed between measurements and simulation for >300-GHz IC designs

III. Interconnects and Backside Processing

Integrated THz receiver and transmitters will require a mixture of circuits including both traditional distributed microwave (e.g., PA or LNA) and analog-type ICs (e.g., Gilbert-cell mixers or frequency dividers). A thin-film three-level IC wiring environment has been developed to support both circuit types. The wiring utilizes a benzocyclobutene (BCB) interlayer dielectric with a low dielectric constant ($\epsilon_r = 2.7$) and electroplated Au-based metallization. The technology also includes MIM capacitors and thin-film resistors.

Lumped analog blocks require low-delay low-parasitic wiring, and interconnects for these circuits must support narrow lines and fine pitch. This wiring can be achieved in the lower two metallization levels (M1 and M2) which are separated by a 1-μm BCB layer. The interlayer BCB thickness can be precisely controlled using a uniform reactive ion etch process. Distributed millimeter-wave and THz circuits require high-Q and low-loss transmission lines. To achieve this, the upper level metallization (M3) is separated from M1 by a thicker 7-μm BCB layer. This permits the realization of low-loss microstrip lines using either standard (M3 signal, M1 ground) or inverted (M1 signal, M3 ground) configurations. A cross section of the HBT wiring environment is shown in Fig. 3.

The use of thin-film wiring on the topside of the InP substrate permits the substrate thickness to be kept relatively thick (50 μm) to support handling ruggedness. Dry-etched substrate vias are added to IC designs with sufficient density to suppress modes that could be excited from parasitic RF leakage into the substrate. Substrate mode control is particularly important when packaging IC chips in waveguide blocks.

To facilitate waveguide packaging, we have developed a backside etch singulation process that is used to form nonrectangular IC die. This process permits the formation of narrow InP extensions that can be extended into rectangular waveguide channels. The extensions minimize breaks in the waveguide sidewall and permit a larger overall IC die size. Additionally, the backside etch process can be used to remove the InP substrate directly beneath waveguide probes (waveguide-to-chip transitions), improving probe performance. Waveguide probes designs have been separately characterized with through-line test structures in waveguide blocks shown in Fig. 4. Probe insertion losses of <1 dB per transition have been measured in the 220–325-GHz band.

IV. TMIC Design: 300–570-GHz Oscillators

A variety of transceiver building blocks have been demonstrated using the developed 0.25-μm InP HBT process: a single-stage cascode LNA with 8.4-dB gain at 288 GHz and 11.2-dB noise figure at 300 GHz [6]; a six-stage differential drive amplifier with 17.3-dB gain at 290 GHz [26]; differential oscillators up to 346 GHz with −9 dBm of output power and >10 GHz of tuning ranges [5]; a 305–330-GHz 2:1 dynamic frequency divider [27]; a single-chip 300 GHz PLL with 0.36-GHz locking range [28], and 220-GHz PLL IC with 5.9-GHz locking range [29]. In this paper, the design and testing of oscillators operating up to 0.57 THz will be presented.

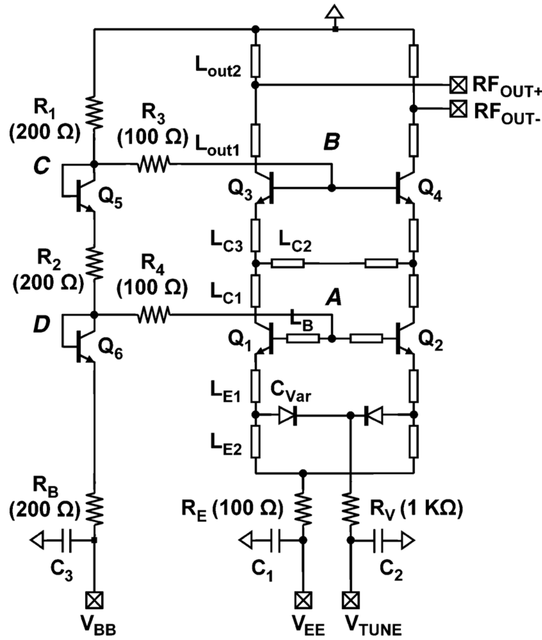


Fig. 5. Simplified schematic of voltage-controlled oscillators (VCO). All HBTs are $3 \times 0.25\ \mu m^2$ with a single finger. Actual oscillator output is single-ended, with one RF_{OUT} node internally terminated to 50 Ω. Fixed-frequency oscillators share the same topology, but with no varactors.

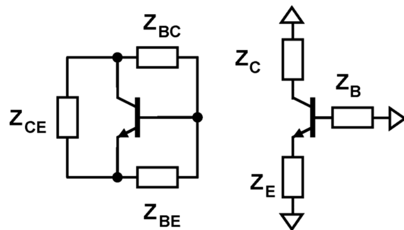


Fig. 6. Generic oscillator topology: parallel-tuned with Π-feedback (left) and series-tuned with T-feedback (right).

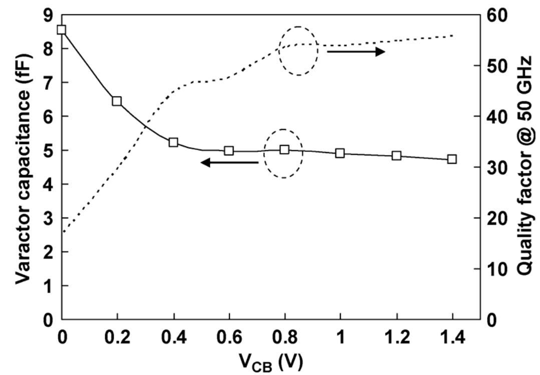


Fig. 7. Measured varactor characteristics at 50 GHz. Assuming a series RC equivalent model, varactor Q-factor would be 7–8 at 300 GHz (i.e., 1/6 of 50 GHz Q-factor) for $V_{CB} > 0.4$ V.

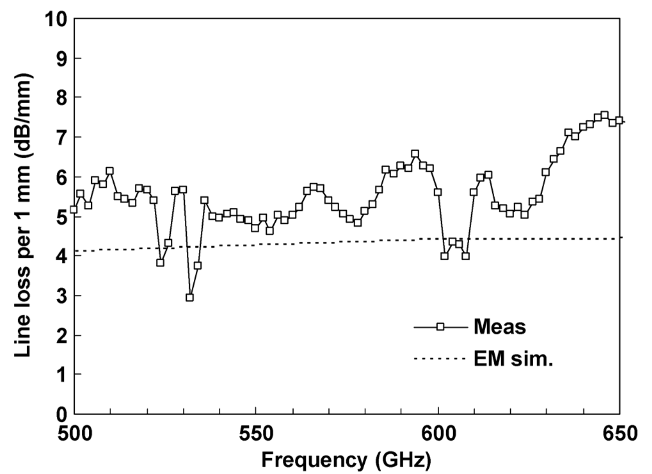


Fig. 8. Loss of 50 Ω inverted-microstrip line: measured (squares) and EM simulation (dot line).

A. Differential Oscillator With an Integrated Output Buffer

Oscillator design in this work is based on a differential series-tuned topology shown in Fig. 5. Compared with a parallel-tuned topology (Fig. 6), which has been popular for lower-frequency oscillators using lumped elements (e.g., Colpitts oscillators), a series-tuned topology provides more layout flexibility in transmission-line-based design, thus more scalable to different design frequencies. In addition, a series topology has less line discontinuities (thus more tolerant to modeling errors) and is more suitable for a differential configuration than a parallel topology.

The differential configuration offers significant advantages over single-ended implementations for very high-frequency oscillator designs. The differential operation creates a virtual ground along the plane of symmetry, making the oscillator operation insensitive to common-mode impedance such as the base/emitter bias circuitry, varactor bias lines, and collector grounding vias (which are $\sim$10 μm long). In particular, a virtual ground provides *lossless* ac–ground, thus eliminating circuit losses from the use of *lossy* ac–ground. This property of differential topology is especially beneficial for very high-frequency designs where typical ac–ground implementations (e.g., radial stubs or MIM capacitors) suffer from relatively high ohmic and radiation losses. A virtual ground is also broadband with no internal inductance. Typical single-ended ac-grounds have finite bandwidth due to internal inductance, and its inaccurate modeling can lead to detuning in circuit operating frequencies. At a system level, differential oscillator outputs enable fully differential transceiver architectures, thus improving common-mode noise rejection and LO leakage cancellation. Finally, the differential output power is 3 dB higher compared with single-ended designs under the same HBT bias. All of these benefits are obtained at the expense of increased dc power consumption and chip area. Care must be taken to eliminate the possibility of common-mode oscillations.

In the circuit schematic in Fig. 5, Q_1–Q_2 form a differential oscillator core. Q_3-Q_4 are configured as a common-base (CB) amplifier, providing power gain and reverse isolation from load perturbation, while re-using the same bias current as Q_1–Q_2. The oscillation frequency is determined by the impedance seen from the Q_1–Q_2 base, emitter, and collector nodes. Tuning bandwidth can be controlled by balancing L_{E1} and L_{E2}, for a given C_{VAR} and emitter impedance; longer L_{E2} will increase the tuning range (i.e., tighter varactor coupling), but the oscillation power can suffer if C_{VAR} does not have a sufficiently high Q-factor. Considering uncertainties in HBT and varactor models, varactor was rather loosely coupled: L_{E2}

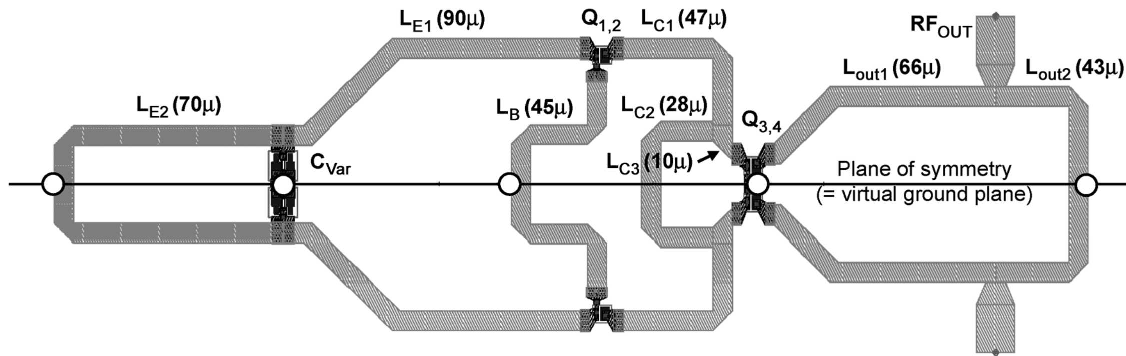


Fig. 9. Layout of 300-GHz differential VCO core with mirror symmetry. All lines are 70 Ω ($W = 5$ μm), except for the 50-Ω RF output lines ($W = 10$ μm). Bias connections are made at common-mode nodes, shown as circles. The size of oscillator core (with output buffer) is approximately 300 × 100 μm^2 and 150 × 50 μm^2, for 300- and 570-GHz design, respectively.

was increased to the point where output power starts to drop by a small amount (e.g., by 0.5 dB). $C_{\rm VAR}$ is a single-finger base–collector (B-C) junction at reverse bias, carefully sized to minimize series resistance arising from base metal/contact and subcollector regions. A varactor Q-factor at 300 GHz is expected to be 7–8, extrapolated from lower frequency characterization in Fig. 7. Capacitance ratio between 0–1 V of reverse bias is ~1.6. The amount of core power coupling to the CB buffer can be adjusted by "step-down" inductance L_{C2}. The additional series line L_{C3} increases flexibility in layout, since Q_3 and Q_4 must be as close to each other as possible. $L_{\rm out1}$ and $L_{\rm out2}$ provide impedance match to 50-Ω load at the CB buffer output. Base voltages of Q_1–Q_4 are defined by diode-connected HBTs (Q_5–Q_6) and R_1–R_2. All HBTs are 3 × 0.25 μm^2 with a single finger, nominally biased at the emitter current density of $J_E = 5 - 10$ mA/μm^2. Load pull simulations suggest that oscillation frequencies typically change by ±1 GHz at −15 dB of load impedance mismatches.

Differential circuits may be subject to common-mode instability, if not carefully designed. For example, in Fig. 5, there exists an explicit common-mode feedback loop consisting of the nodes A, B, C and D. Simulation showed the input impedance to the oscillator core at nodes A and B approaches a short circuit at 10–50 GHz, suggesting potential instability. Series resistors R_3–R_4 were therefore added for stabilization (parallel resistors could be used for open-circuit type instability).

All transmission lines in Fig. 5 are inverted-microstrip lines, where M2 and M3 constitute the signal line and ground plane, respectively. A large continuous ground plane is thus guaranteed, with M1 and M2 available for low-inductance local interconnects. With other wiring options such as coplanar waveguides or normal microstrip lines, the ground plane can no longer be solid and continuous, and resulting circuit design will be sensitive to electromagnetic (EM) modeling accuracies. EM simulation predicts 3–4 dB/mm of loss for a 50-Ω ($W = 10$ μm) inverted microstrip line from 300 to 500 GHz, with corresponding Q-factors from 18 to 23. Fig. 8 compares measured and simulated loss of a 50-Ω line, where measurement shows ~20% higher losses than simulation. Except for the output 50-Ω lines ($W = 10$ μm), relatively narrow lines ($W = 5$ μm) are used for oscillator circuits to obtain a higher line aspect ratio. This approach minimizes the effects of line discontinuities (e.g., bends, T-junctions, or crosses) at the cost of slightly higher line loss (~15% higher than a 50-Ω line). Layout of the differential oscillator core circuits are shown in Fig. 9. A VCO chip photograph is shown in Fig. 10.

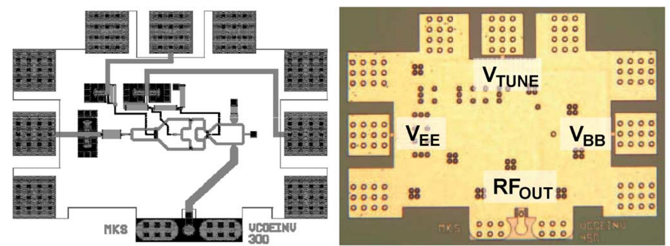


Fig. 10. VCO layout and chip photograph (740 × 550 μm^2). The entire circuit except pad areas is covered by a M3 ground plane.

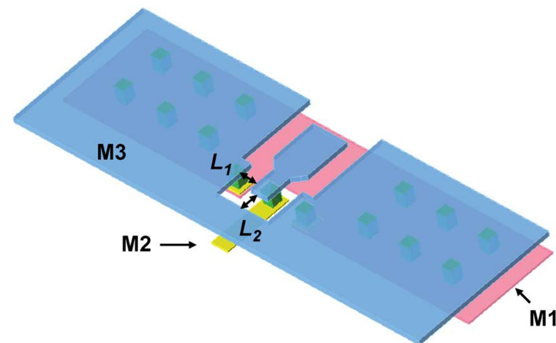


Fig. 11. Transition from inverted microstrip to a GSG pad. L_1 and L_2 were adjusted for a low insertion loss from 300 to 550 GHz.

On-wafer testing of the designed oscillators requires a transition from inverted-microstrip line to a coplanar GSG pad. Fig. 11 illustrates such a transition structure used in this work. Distance from the M3 ground plane to the signal pad (L_1 and L_2 in Fig. 11) was adjusted for broadband low-loss transition: simulated insertion loss was 0.5 and 1.4 dB at 300 and 550 GHz, respectively, with <12 dB of return loss. Measured transition loss at 500–550 GHz was to within 0.5 dB from simulation.

B. Oscillator Designs With an Integrated Down-Conversion Mixer

In this work, a series of integrated oscillator-mixer chain were also designed and fabricated to facilitate measurement

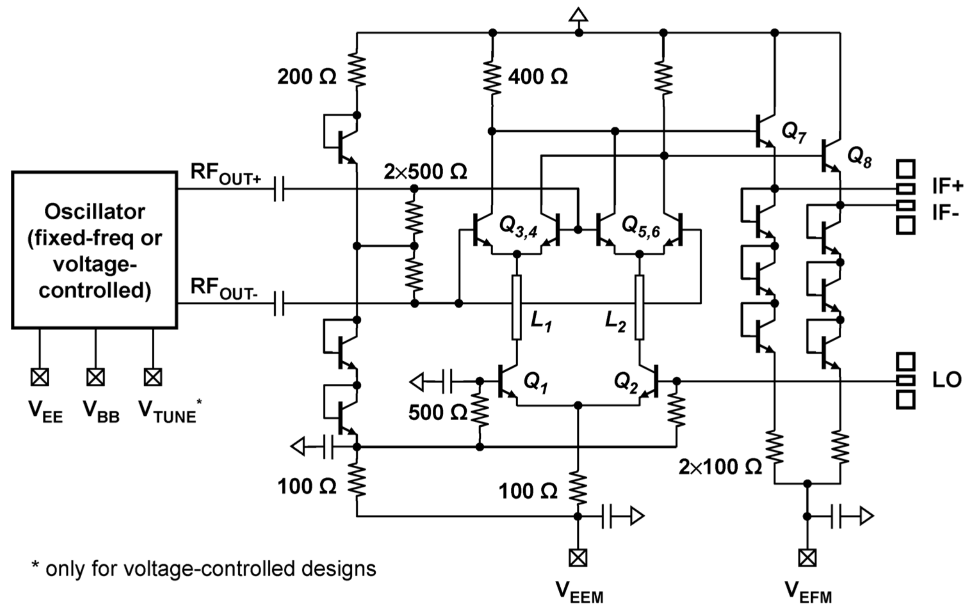


Fig. 12. Simplified schematic of the integrated oscillator-mixer chain. All HBTs are $3 \times 0.25\ \mu m^2$, except for emitter follower devices (Q7 and Q8: $4 \times 0.25\ \mu m^2$). The double-balanced mixer consumes approximately 70 mW of dc power.

of oscillation frequencies. This enables bypassing probe loss and/or waveguide transition losses, which tend to be significantly high beyond 320 GHz. Simplified schematic of an oscillator-mixer chain is shown in Fig. 12, where oscillator core circuits are followed by a double-balanced mixer. L_1 and L_2 provide impedance matching between lower and upper differential pairs, thus improving conversion gain and LO sensitivity. For testing convenience, the external LO is applied in a single-ended fashion, and the unused LO port is ac-grounded by a MIM capacitor. Emitter followers at the mixer output extend IF bandwidth.

Oscillation frequency $f_{\rm OSC}$ can be obtained from the external LO frequency $f_{\rm LO}$ and measured IF frequency $f_{\rm IF}$ as follows.

$$f_{\rm OSC} = N f_{\rm LO} \pm f_{\rm IF}. \quad (1)$$

The harmonic number N can be determined by monitoring $f_{\rm IF}$ while applying a frequency shift at LO

$$N = \text{Find a nearest integer} \left[\left| \frac{\Delta f_{\rm IF} + \epsilon}{\Delta f_{\rm LO}} \right| \right] \quad (2)$$

where $\Delta f_{\rm LO}$ and $\Delta f_{\rm IF}$ are LO frequency shift and resulting change in IF frequency, respectively. In practice, determination of the IF frequency is subject to a measurement error ϵ due to oscillation frequency drift, modulation due to external power supply noise, among others. Once N is obtained, the sign of the ratio $\Delta f_{\rm LO}/\Delta f_{\rm IF}$ uniquely determines $f_{\rm OSC}$ from (1): $f_{\rm OSC} = N f_{\rm LO} - f_{\rm IF}$ if $\Delta f_{\rm LO}/\Delta f_{\rm IF} > 0$, $f_{\rm OSC} = N f_{\rm LO} + f_{\rm IF}$ otherwise. Selection of LO frequency shift $\Delta f_{\rm LO}$ is critical for accurate oscillation frequency measurement: it must be large compared with ϵ, yet it should be small enough to avoid ambiguity in identifying N. The latter consideration typically limits $\Delta f_{\rm LO}$ to $(1/2) f_{\rm LO}$. As will be discussed later, it was experimentally found that the choice of $f_{\rm LO} \simeq 20$ GHz and $\Delta f_{\rm LO} = 0.2$ GHz enables reasonably accurate frequency measurement of 400–570-GHz oscillators with $N = 21$–31. Conversion loss

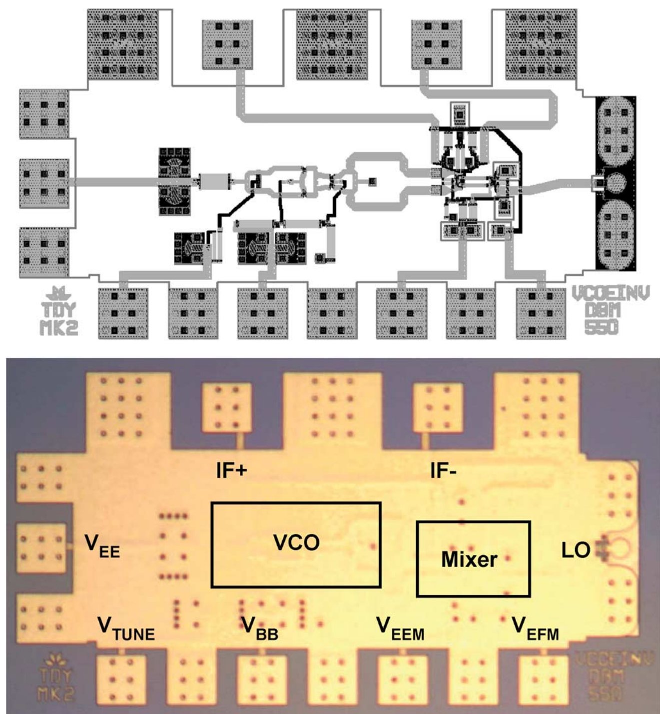


Fig. 13. Layout (top) and chip photograph (bottom) of the integrated VCO–mixer chain ($880 \times 470\ \mu m^2$).

of the designed mixer under these harmonic numbers was −35 to −55 dB at −3 dBm of external LO power, according to simulation. Determination of LO frequencies needs considerations of signal generator availability: the down-conversion loss can be reduced by operating the mixer at a lower N, but at the cost of using higher LO frequencies.

The designed mixer has >25 GHz of 3 dB IF bandwidth, which is wide enough to perform IF spectrum measurement with $f_{LO} = 20$ GHz. The mixer RF input is reasonably well

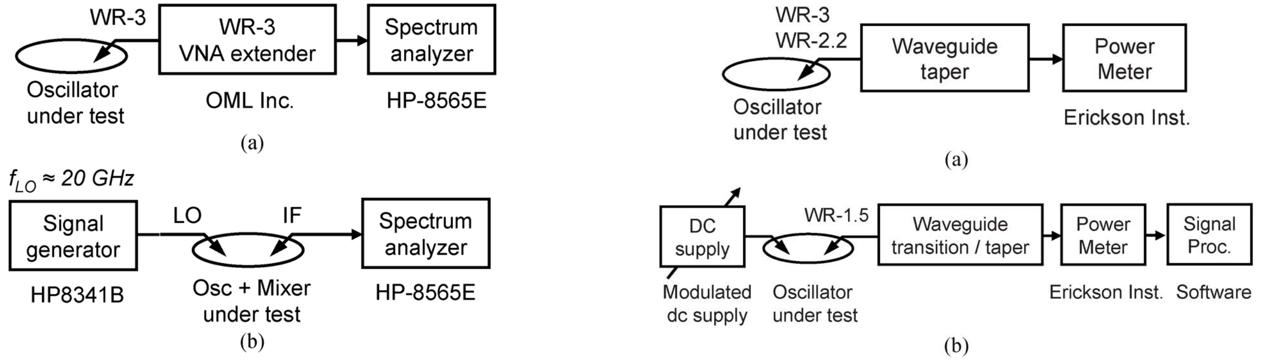
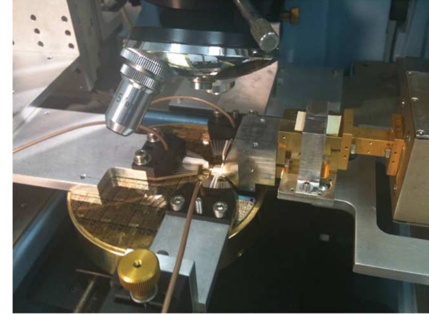


Fig. 14. Setup for oscillator frequency measurement: (a) Oscillators up to 346 GHz and (b) 400–570 GHz oscillator–mixer chains.



(c)

Fig. 15. Setup for oscillator power measurement. (a) WR-3 (220-325 GHz)/ WR-2.2 (325–500 GHz) band designs. (b) WR-1.5 band (500–750 GHz) oscillator. (c) Photograph of the WR-1.5 band (500–750 GHz) setup.

matched (<15 dB of return loss), and therefore detuning in oscillation frequency compared with a 50-Ω load is typically less than 1 GHz in simulation. Overall layout and chip photograph of an integrated oscillator–mixer chain is shown in Fig. 13.

V. Measurement Results

Measured oscillator results from two recent HBT process runs are presented. A series of fixed-frequency oscillators (FFOs) and VCOs were designed up to 570 GHz and fabricated in *THzIC1* and *THzIC2*. Oscillator designs with an integrated mixer were only implemented in the *THzIC2* technology.

A. Setup

The fabricated oscillators were characterized on-wafer using the test setup illustrated in Figs. 14 and 15. For spectrum measurement, the oscillator output was down-converted by either a WR-3 (220–325 GHz) VNA extender [OML Inc in Fig. 14(a)] or integrated double-balanced mixer [Fig. 14(b)], depending on the design frequency. IF output of the external or integrated mixer connects to a spectrum analyzer. Oscillation frequency can be determined by monitoring the IF frequency shift resulting from a change in LO frequency, as discussed in the previous section. Oscillator output power was measured by using a wideband power meter (Erickson Instrument), as shown in Fig. 15. Waveguide probes at three different bands were used depending on the design frequencies: WR-3 (220–325 GHz, from GGB Inc.), WR-2.2 (325–500 GHz, from GGB Inc.), and WR-1.5 (500–750 GHz [30]).

B. Oscillation Frequency

Typical IF spectra from the 220–325-GHz VNA extender are shown in Fig. 16. Figs. 17 and 18 show IF spectra of 413- and 573-GHz oscillator–mixer chains at two different LO frequencies with $\Delta f_{\mathrm{LO}} = 0.2$ GHz, illustrating the determination of oscillation frequency. From (2), the harmonic number in Fig. 17 is $N = (7.100\ \mathrm{GHz} - 2.893\ \mathrm{GHz})/(20.0\ \mathrm{GHz} - 19.8\ \mathrm{GHz}) = 21.035 \simeq 21$. Since $\Delta f_{\mathrm{LO}}/\Delta f_{\mathrm{IF}} > 0$, it follows that $f_{\mathrm{osc}} = N f_{\mathrm{LO}} - f_{\mathrm{IF}} = 412.9$ GHz. For Fig. 18, similar calculation yields $f_{\mathrm{osc}} = 573.11$ GHz with $N = 29.035 \simeq 29$. Note in Figs. 17 and 18 that the spectral line width is small compared with $\Delta f_{\mathrm{LO}} = 0.2$ GHz, allowing for accurate determination of oscillation frequencies. The drift of oscillation frequencies for a 10-min duration was typically less than 10 MHz, i.e., less than 5% of Δf_{LO}.

Measured frequencies of fixed-frequency oscillators are summarized in Table I. For *THzIC1* designs, there is ∼10% discrepancy in frequency between the initial design and measurement. Initial HBT models used in the design cycle were based on projected transistor performance determined from the transistor geometry and epitaxy design. The HBT model was revised to match measured transistor data, and resimulations now predict the oscillation frequencies to within 3% of measurement.

Measured VCO tuning ranges were approximately 10 GHz for up to 296-GHz designs [Fig. 19(a)], which is within ±10% of simulation. Tuning ranges of higher frequency VCO designs are, however, substantially smaller [Fig. 19(b)] due to conservative tuning network design (i.e., loose varactor coupling).

A total of 22 fixed-frequency oscillators centered at 287 GHz were measured across a full 4-in wafer. The measured spread in oscillation frequency was ±1 GHz for 77% of the measured samples. The maximum deviation in oscillation frequency was 6 GHz.

C. Phase Noise

HBT devices, due to their lower $1/f$ noise compared with HEMTs, have the potential for low phase-noise oscillators. Phase noise of fixed-frequency oscillators up to 346 GHz was measured by looking at their IF spectrum. Fig. 20 shows that measured phase noise at 10-MHz offset ranges from −103 to −90 dBc/Hz, depending on the oscillation frequency. Note that the measured phase noise slope is approximately 20 dBc/dec for offset frequencies between 1 and 10 MHz. Fluctuations in oscillation frequency prevent phase noise measurement below

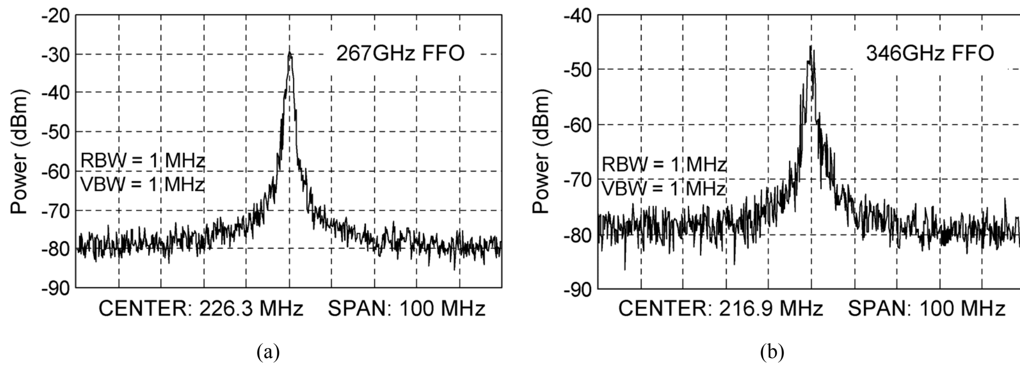


Fig. 16. Measured IF spectrum of (a) 267-GHz and (b) 346-GHz fixed-frequency oscillators, down-converted by a WR-3 (220–325 GHz) VNA extender.

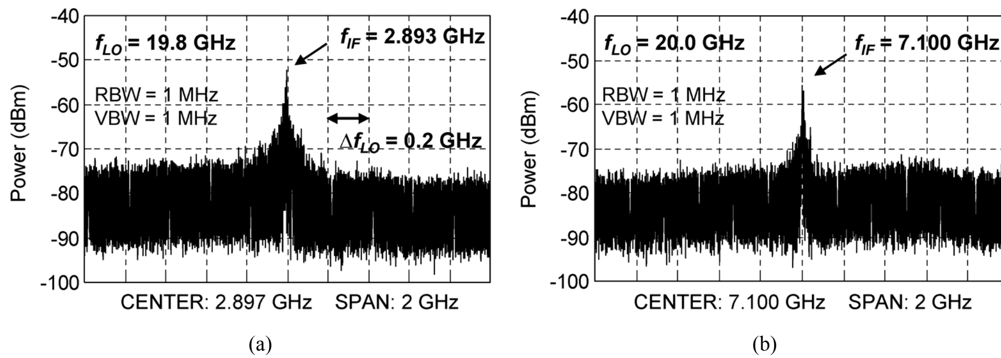


Fig. 17. Measured IF spectrum of 413-GHz fixed-frequency integrated oscillator-mixer chain with $f_{\rm LO}$ = (a) 19.8 GHz and (b) 20 GHz.

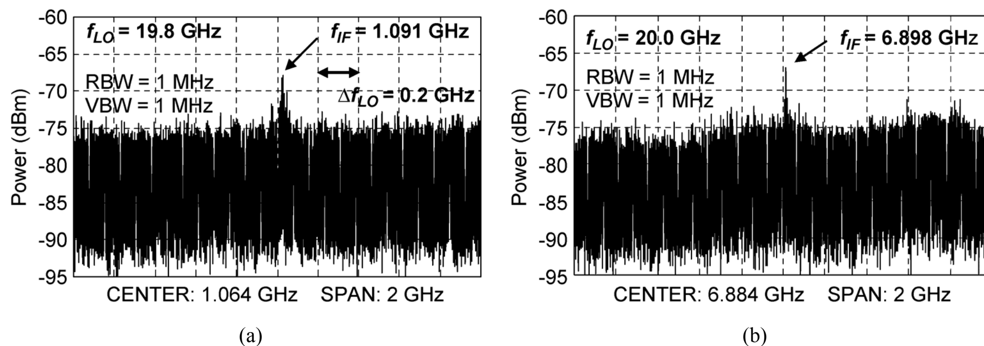


Fig. 18. Measured IF spectrum of 573-GHz fixed-frequency integrated oscillator-mixer chain with $f_{\rm LO}$ = (a) 19.8 GHz and (b) 20 GHz.

1-MHz offset. Measurement beyond 100-MHz offset is limited by the IF noise floor, especially for $\geq$300-GHz designs. Fig. 21 summarizes measured phase noise results. Total dc power consumption was 50.3 mW, with $V_{\rm EE} = -4.6$ V (8 mA) and $V_{\rm BB} = -4.5$ V (3 mA).

D. Output Power

Output power of fixed-frequency oscillators up to 346 GHz was measured using the setup in Fig. 15(a). Maximum output power was obtained at J_E = 7-10 mA/μm^2, with total dc power ranging from 76 to 115 mW. Under an optimum bias, the measured output power was 312 (-5.1 dBm), 205 (-6.9 dBm), 120 (-9.2 dBm), and 80 μW (-11.0 dBm), for 267.4-, 286.8-, 310.2-, and 346.2-GHz design, respectively, before applying WR-3 probe loss correction. Loss of a WR-3 probe is expected to be approximately 3 dB up to 325 GHz (from manufacturer's data) and 4 dB at around 346 GHz (from a thru-line measurement).

Oscillation power of 400–500-GHz designs were measured using a similar setup [Fig. 15(a)] with a WR-2.2 (325–500 GHz) probe. After deembedding WR-2.2 probe loss (5.5–7.5 dB [31]), the measured power was -5.6 and -8.9 dBm, at oscillation frequencies of 412.9 and 487.7 GHz, respectively.

Output power of the 570-GHz design was substantially lower than lower frequency designs, making accurate power measurement challenging. At the lower end of power full-scale (e.g., 200 μW or 2 mW maximum), measurement time-constant of the power meter was of the order of 1–10 s. Long settling time can make power meter calibration invalid, since measurement drifts (e.g., due to changes in thermal condition or ambient radiation) can be relatively large compared to the actual input

TABLE I
SUMMARY OF FIXED-FREQUENCY OSCILLATOR RESULTS

Process Technology	Oscillation Frequency			Single-ended output power[1] (dBm)			Phase noise @ 10 MHz offset
	Design	Measured	Simulation w/ revised HBT model	Simulation w/ revised HBT model[2]	Measured (uncorrected)	Measured (corrected[3])	
THzIC1	292.4 GHz	267.4 GHz	261.5 GHz	-3.6 dBm	-5.1 dBm	-2.1 dBm	-102.4 dBc/Hz
THzIC1	315.4 GHz	286.8 GHz	280.6 GHz	-4.7 dBm	-6.9 dBm	-3.9 dBm	-99.8 dBc/Hz
THzIC1	336.5 GHz	310.2 GHz	303.7 GHz	-6.4 dBm	-9.2 dBm	-6.2 dBm	-95.6 dBc/Hz
THzIC1	387.8 GHz	346.2 GHz	346.0 GHz	-7.7 dBm	-11.0 dBm	-7.0 dBm	-88.8 dBc/Hz
THzIC2	397.0 GHz	412.9 GHz	394.5 GHz	-3.5 dBm	-11.1 dBm	-5.6 dBm	-
THzIC2	508.0 GHz	487.7 GHz	505.9 GHz	-5.2 dBm	-16.4 dBm	-8.9 dBm	-
THzIC2	587.9 GHz	573.1 GHz	586.3 GHz	-9.0 dBm	-36.2 dBm	-19.2 dBm	-

[1] V_{EE} and V_{BB} tuned for a maximum measured power ($P_{\mathrm{DC}} = 76$–115 mW, depending on design).
[2] Inverted-microstrip-to-GSG-pad transition loss included.
[3] Probe and/or waveguide transition loss is deembedded.

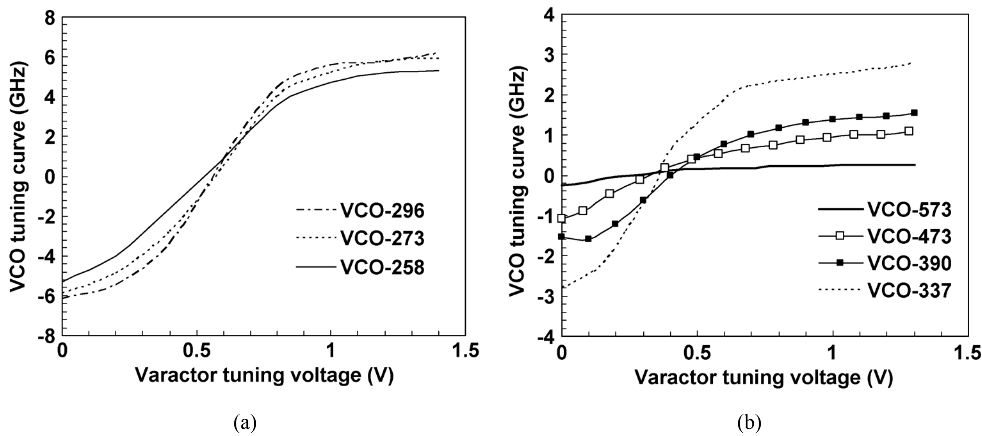


Fig. 19. Measured tuning curves of VCOs. (a) Lower band VCOs centered at 258, 273, and 296 GHz have wider tuning ranges than (b) upper frequency VCOs centered at 337, 390, 473, and 573 GHz as a result of tighter varactor coupling. Tuning voltages represent actual reverse bias across *B*–*C* varactors.

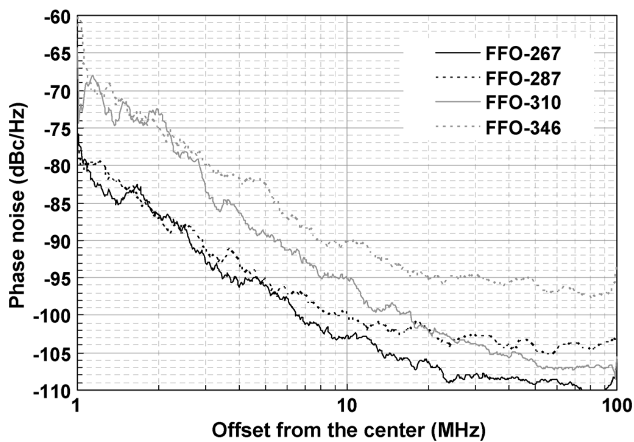


Fig. 20. Typical measured phase noise of four fixed-frequency oscillators centered at 267, 287, 310, and 346 GHz. Phase noise measurement utility of spectrum analyzer (HP8565E) was used with 4% spectral averaging.

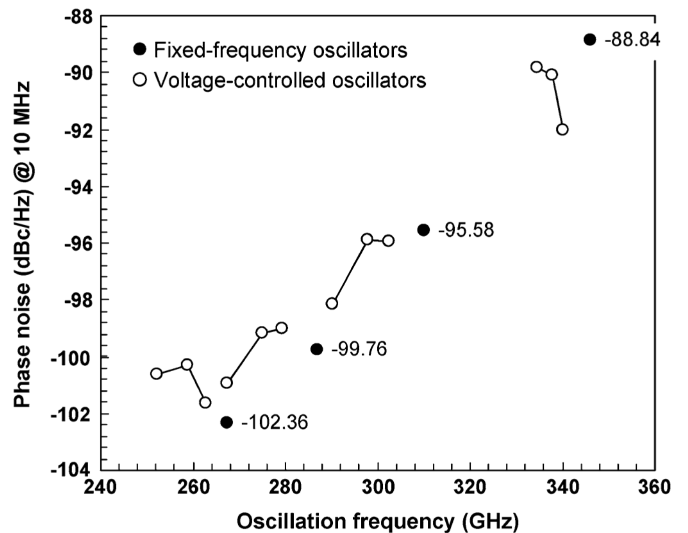
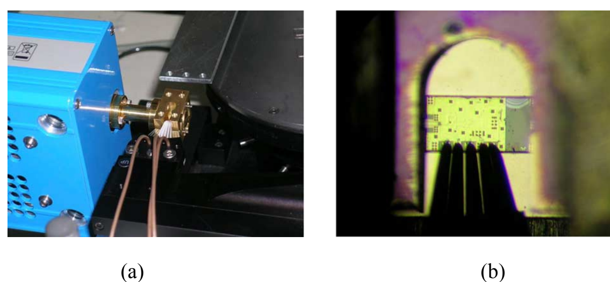


Fig. 21. Measured phase noise (10-MHz offset) of FFOs and VCOs up to 346 GHz. Each point represents an average of five measurements by using Marker-Noise function of the spectrum analyzer at 100-MHz span.

power. For more accurate power measurement, a modulated test setup was devised [Fig. 15(b) and (c)]: oscillator power supplies are periodically switched on and off, while the power meter read-out is digitized and subsequently demodulated by separately averaging on- and off-period measurements. If the modulation period is chosen sufficiently short, measurement drifts will be averaged out. A cycle time of 6 s was experimentally found to give a reasonable accuracy. After averaging 100 such



(a) (b)

Fig. 22. Testing of a 300-GHz oscillator in (a) a waveguide package and (b) its close-up view, where a dc probe is used for biasing.

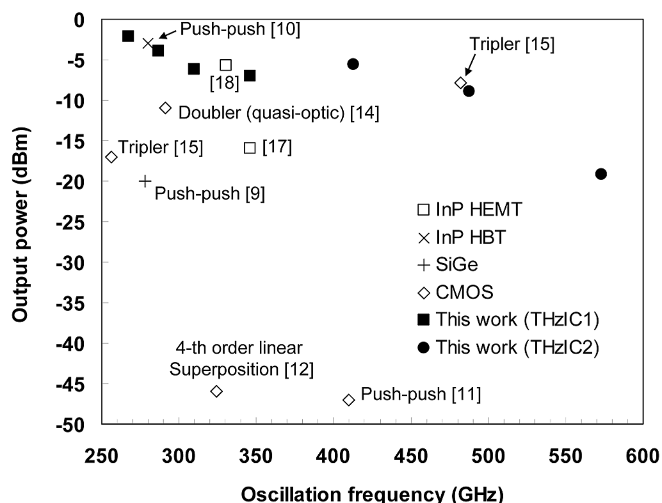


Fig. 23. Recently reported mm-wave oscillators beyond 250 GHz.

cycles, the output power of the 570-GHz oscillator was measured to be 12 μW (-19.2 dBm), after correcting for WR-1.5 (500–750 GHz) probe and transition losses (total 17 dB). Measurement error was estimated to be ± 1.7 μW, calculated from the standard deviations of on- and off-periods.

VCOs exhibit slightly less measured output power than fixed-frequency designs: typically ~ 1 and ~ 3 dB less power, for <320-GHz designs and 570-GHz design, respectively.

Note that all power measurement includes the loss of inverted-microstrip-to-pad transition in Fig. 11. A 300-GHz oscillator in a waveguide package was characterized by direct waveguide connection (Fig. 22), and similar measurement results were obtained as on-wafer testing. See Table I for a full summary of FFO results. Fig. 23 compares recently reported mm-wave oscillators.

VI. Conclusion

We have presented a high-performance 0.25-μm InP HBT IC technology suitable for >300-GHz applications. The initial demonstration of key circuit building blocks presents a promising path for developing fully integrated THz transmitter and receiver circuits [5], [6], [26]–[29]. Additionally, a 128-nm HBT technology is in development for operation at even higher frequencies.

Design and characterization of fundamental oscillators operating up to 0.57 THz have been presented. To the best of the authors' knowledge, this work represents the highest frequency fundamental oscillators using three-terminal devices. The measured output power was comparable to HEMT oscillators up to 346 GHz. Varactor-tuned designs exhibit >10 GHz of tuning bandwidth.

Acknowledgment

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References

[1] M. Urteaga, M. Seo, J. Hacker, Z. Griffith, A. Young, R. Pierson, P. Rowell, A. Skalare, and M. Rodwell, "InP HBT integrated circuit technology for terahertz frequencies," in *Proc. IEEE Compound Semicond. Integr. Circuit Symp.*, 2010, pp. 1–4.

[2] R. Lai, X. Mei, W. Deal, W. Yoshida, Y. Kim, P. Liu, J. Lee, J. Uyeda, V. Radisic, M. Lange, T. Gaier, L. Samoska, and A. Fung, "Sub 50 nm InP HEMT device with f_{max} greater than 1 THz," in *Proc. IEEE Int. Electron Devices Meeting*, 2007, pp. 609–611.

[3] E. Lobisser, Z. Griffith, V. Jain, B. Thibeault, M. Rodwell, D. Loubychev, A. Snyder, Y. Wu, J. Fastenau, and A. Liu, "200-nm InGaAs/InP type I DHBT employing a dual-sidewall emitter process demonstrating $f_{max} \gg 800$ GHz and $f_T = 360$ GHz," in *Proc. IEEE Int. Conf. Indium Phosphide Related Materials*, May 2009, pp. 16–19.

[4] W. Deal, X. Mei, V. Radisic, K. Leong, S. Sarkozy, B. Gorospe, J. Lee, P. Liu, W. Yoshida, J. Zhou, M. Lange, J. Uyeda, and R. Lai, "Demonstration of a 0.48 THz amplifier module using InP HEMT transistors," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 5, pp. 289–291, May 2010.

[5] M. Seo, M. Urteaga, A. Young, V. Jain, Z. Griffith, J. Hacker, P. Rowell, R. Pierson, and M. Rodwell, " >300 GHz fixed-frequency and voltage-controlled fundamental oscillators in an InP HBT process," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2010, pp. 272–275.

[6] J. Hacker, M. Seo, A. Young, Z. Griffith, M. Urteaga, T. Reed, and M. Rodwell, "THz MMICs based on InP HBT technology," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2010, pp. 1126–1129.

[7] M. D'Amore, C. Monier, S. Lin, B. Oyama, D. Scott, E. Kaneshiro, A. Gutierrez-Aitken, and A. Oki, "A 0.25 μm InP DHBT 200 GHz+ static frequency divider," in *Proc. IEEE Compound Semicond. Integr. Circuit Symp.*, 2009, pp. 1–4.

[8] Z. Griffith, M. Urteaga, R. Pierson, P. Rowell, M. Rodwell, and B. Brar, "A 204.8 GHz static divide-by-8 frequency divider in 250 nm InP HBT," in *Proc. IEEE Compound Semicond. Integr. Circuit Symp.*, 2010, pp. 1–4.

[9] R. Wanner, R. Lachner, G. Olbrich, and P. Russer, "A SiGe monolithically integrated 278 GHz push-push oscillator," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2007, pp. 333–336.

[10] Y. Baeyens, N. Weimann, V. Houtsma, J. Weiner, Y. Yang, J. Frackoviak, P. Roux, A. Tate, and Y. Chen, "Highly efficient harmonically tuned InP D-HBT push-push oscillators operating up to 287 GHz," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2007, pp. 341–344.

[11] E. Seok, C. Cao, D. Shim, D. Arenas, D. Tanner, and C.-M. Hung, "A 410 GHz CMOS push-push oscillator with an on-chip patch antenna," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 472–629.

[12] D. Huang, T. LaRocca, L. Samoska, A. Fung, and M.-C. Chang, "324 GHz CMOS frequency generator using linear superposition technique," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 476–629.

[13] Q. Gu, Z. Xu, H.-Y. Jian, X. Xu, M. Chang, W. Liu, and H. Fetterman, "Generating terahertz signals in 65 nm CMOS with negative-resistance resonator boosting and selective harmonic suppression," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2010, pp. 109–110.

[14] K. Sengupta and A. Hajimiri, "Distributed active radiation for THz signal generation," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 288–289.

[15] O. Momeni and E. Afshari, "High power terahertz and millimeter-wave oscillator design: A systematic approach," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 583–597, Mar. 2011.

[16] S. Rosenbaum, B. Kormanyos, L. Jelloian, M. Matloubian, A. Brown, L. Larson, L. Nguyen, M. Thompson, L. Katehi, and G. Rebeiz, "155- and 213-GHz AlInAs/GaInAs/InP HEMT MMIC oscillators," *IEEE Trans. Microw. Theory Tech.*, vol. 43, no. 4, pp. 927–932, Apr. 1995.

[17] V. Radisic, X. Mei, W. Deal, W. Yoshida, P. Liu, J. Uyeda, M. Barsky, L. Samoska, A. Fung, T. Gaier, and R. Lai, "Demonstration of sub-millimeter wave fundamental oscillators using 35-nm InP HEMT technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 3, pp. 223–225, Mar. 2007.

[18] V. Radisic, L. Samoska, W. Deal, X. Mei, W. Yoshida, P. Liu, J. Uyeda, A. Fung, T. Gaier, and R. Lai, "A 330-GHz MMIC oscillator module," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2008, pp. 395–398.

[19] V. Radisic, D. Sawdai, D. Scott, W. Deal, L. Dang, D. Li, J. Chen, A. Fung, L. Samoska, T. Gaier, and R. Lai, "Demonstration of a 311-GHz fundamental oscillator using InP HBT technology," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 11, pp. 2329–2335, Nov. 2007.

[20] B. Razavi, "A 300-GHz fundamental oscillator in 65-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 894–903, Apr. 2011.

[21] M. Rodwell, M. Le, and B. Brar, "InP bipolar ICs: Scaling roadmaps, frequency limits, manufacturable technologies," *Proc. IEEE*, vol. 96, no. 2, pp. 271–286, Feb. 2008.

[22] Z. Griffith, E. Lind, M. Rodwell, X.-M. Fang, D. Loubychev, Y. Wu, J. Fastenau, and A. Liu, "Sub-300 nm InGaAs/InP Type-I DHBTs with a 150 nm collector, 30 nm base demonstrating 755 GHz f_{max} and 416 GHz f_T," in *Proc. IEEE Int. Conf. Indium Phosphide Related Materials*, May 2007, pp. 403–406.

[23] M. Urteaga, P. Rowell, R. Pierson, B. Brar, M. Dahlstrom, Z. Griffith, M. Rodwell, S. Lee, N. Nguyen, and C. Nguyen-Global, "Deep submicron InP DHBT technology with electroplated emitter and base contacts," in *Proc. IEEE Device Res. Conf.*, 2004, vol. (xiv+247), p. 2.

[24] M. Urteaga, M. Seo, J. Hacker, Z. Griffith, A. Young, R. Pierson, P. Rowell, A. Skalare, V. Jain, E. Lobisser, and M. Rodwell, "InP HBTs for THz frequency integrated circuits," in *Proc. IEEE Int. Conf. Indium Phosphide Related Materials*, May 2011, pp. 1–4.

[25] M. Iwamoto, D. Root, J. Scott, A. Cognata, P. Asbeck, B. Hughes, and D. D'Avanzo, "Large-signal HBT model with improved collector transit time formulation for GaAs and InP technologies," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2003, vol. 2, pp. 635–638.

[26] H. Park, J. Rieh, M. Kim, and J. Hacker, "300 GHz six-stage differential-mode amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2010, pp. 49–52.

[27] M. Seo, M. Urteaga, A. Young, and M. Rodwell, "A 305–330+ GHz 2:1 dynamic frequency divider using InP HBTs," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 8, pp. 468–470, 2010.

[28] M. Seo, M. Urteaga, M. Rodwell, and M. Choe, "A 300 GHz PLL IC in an InP HBT process," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2011, pp. 1–4.

[29] M. Seo, A. Young, M. Urteaga, Z. Griffith, M. Choe, M. Field, and M. Rodwell, "A 220-225.9 GHz InP HBT single-chip PLL," presented at the IEEE Compound Semicond. Integr. Circuit Symp., Oct. 2011.

[30] L. Chen, C. Zhang, T. J. Reck, C. Groppil, A. Arsenovic, A. Lichtenberger, R. M. Weikle, and N. S. Barker, "Terahertz micromachined on-wafer probes: Repeatability and robustness," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2011, pp. 1–4.

[31] *Private Communication With Jet Propulsion Lab, CA.* Oct. 2009.

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Richard Pierson, photograph and biography not available at the time of publication.

Petra Rowell, photograph and biography not available at the time of publication.

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