

A Widely-tunable Integrated Coherent Optical Receiver Using a Phase-Locked Loop

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Abstract—A novel widely-tunable coherent receiver incorporating an optical phase-locked loop (OPLL) on two adjacent chips—a photonic IC and an electronic IC—is described. The design of both is novel, but the focus will be on the photonic IC in this paper. Results indicate a high degree of functionality.

Keywords—coherent; receiver; phase-locked loop

Digital coherent optical receivers have received a lot of interest lately because of their greater tolerance to noise, their compatibility with different modulation formats (such as multi-level phase shift keying), and their intrinsic ability to demultiplex wavelength-division multiplexed (WDM) channels without the use of optical filters.[1-3]

For the implementation of an optical coherent receiver, a free-running local oscillator (LO) is generally used. However, the high-speed digital signal processing is required to perform phase and frequency offset estimation and its correction. However, the high-speed digital signal processors used currently have high power consumption, latency, limited speed and cost considerations.

One solution to this problem is to implement an optical phase-lock loop (OPLL) [4,5], where a local oscillator tracks the frequency and phase of the transmitter laser. Although studies of optical phase-locked loops can be traced back almost fifty years, the OPLL has been proven hard to implement. The main difficulty is that it requires a short loop delay and generally narrow linewidth lasers. For example, to achieve a 1 GHz loop bandwidth, a loop delay less than 100 ps is normally required, which is not feasible using fiber pigtailed components. However, photonic integration can provide short loop delays and alleviate the linewidth issue to some extent.

In this work, we demonstrate a receiver that is realized using a highly integrated optical phase-locked loop that closely integrates a photonic integrated circuit (PIC) with an electronic integrated circuit (EIC) together with a loop filter, as illustrated in Fig.1. The PIC integrates a widely-tunable laser, a 90 degree hybrid and four waveguide detectors. The EIC includes limiting amplifiers, an XOR gate, and a single-sideband mixer. The phase error of the LO laser is detected and negatively fed back into the LO laser, which keeps both lasers phase-locked to

the incoming carrier. Since the two mixed signal have the same phase, no frequency or phase correction is needed.

The PIC uses a widely tunable sampled-grating distributed Bragg reflector (SG-DBR) laser [6] as the LO laser. Two variations 90 degree hybrid designs are realized. One uses four MMI multi-mode interference (MMI) couplers, and the other uses a star coupler.

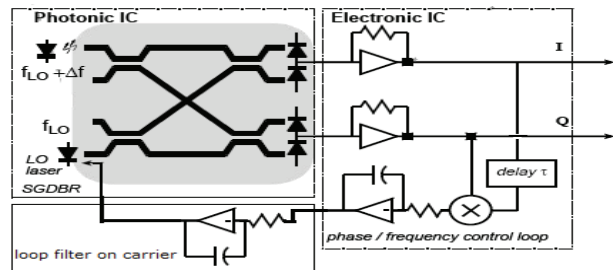


Fig. 1. The architecture of the coherent receiver showing three parts of this receiver: a photonic integrated circuit, an electrical integrated circuit and a loop filter.

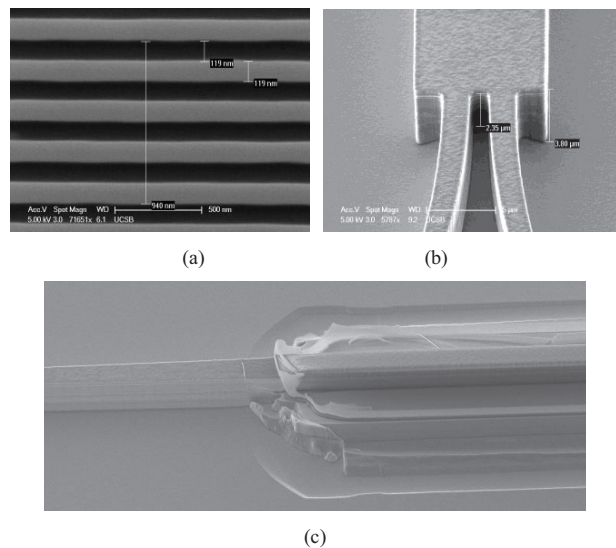


Fig. 2. SEM images of the fabricated PIC showing: (a) the gratings definition for SG-DBR lasers, (b) The vertical and smooth waveguide etch, (c) the waveguide transition from surface ridge to deeply etched waveguide.

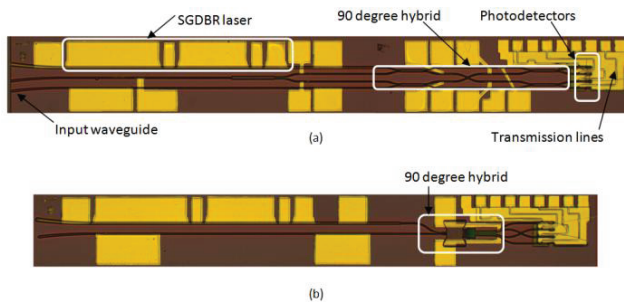


Fig. 3. Microscope images of the PIC showing (a) the PIC using MMI couplers as a 90 degree hybrid, (b) the PIC using star coupler as a 90 degree hybrid.

To monolithically integrate these optical components, we have chosen an InP/InGaAsP centered quantum well (CQW) platform. Quantum well intermixing (QWI) technology was used to define active and passive areas[7]. Sampled gratings, as shown in Fig. 2(a), are defined using electron beam lithography. This is followed by a p-cladding over-growth and waveguide definition using a $\text{Cl}_2/\text{H}_2/\text{Ar}$ based ICP-RIE etch. The results of the etching are shown in Fig. 2(b). Since both the surface ridge waveguide and deeply-etched waveguide are integrated on one PIC, a low loss transition is needed, as shown in Fig. 2(c). To achieve high-frequency on-chip photodetectors, microstrip transmission lines are fabricated on the PIC using bisbenzocyclobutene (BCB) as a dielectric layer. After the BCB definition step, the waveguide tops are opened for p-metal contacts using a ‘semi-self aligned’ process followed by the opening of direct vias for detectors. After deposition of P-metal, the wafer is thinned down, and back-side metallization is applied. Fig. 3 shows the microscope images of the final devices. Fig. 3(a) shows a PIC that is designed using MMI couplers as the 90 degree hybrid and Fig. 3(b) shows the PIC that is designed using a star coupler.

Fig. 4(a) shows the gain curve of a 200 μm long, 3 μm wide CQW SOA at 1550 nm. 68 mA (11.3 kA/cm^2) of current gives a peak gain of 7dB (35 dB/mm). The performance of the SG-DBR laser is shown in Fig. 4(b). The SG-DBR laser is characterized using a 200 μm long SOA acting as a photodetector under reverse bias, assuming unity quantum efficiency. The threshold current is 40 mA with a differential efficiency of 0.37 W/A. The maximum output power is around 18mW.

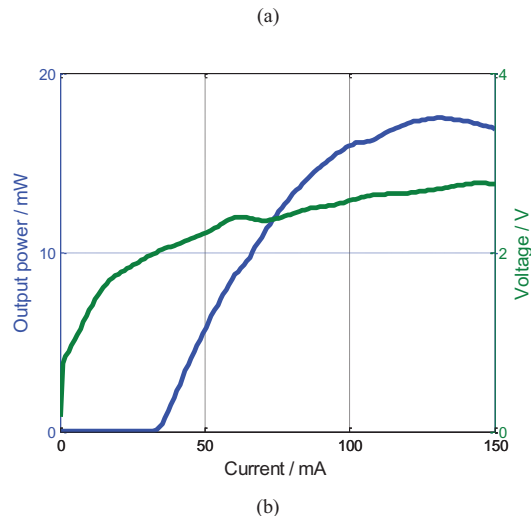
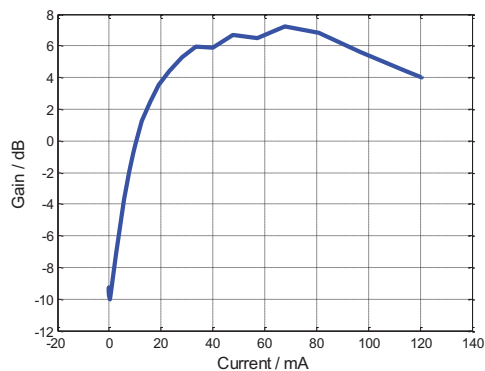


Fig. 4. Measurement result of the PIC. (a) The gain curve of the SOA at 1550nm. (b) The L-I-V curve of the SG-DBR laser

Data for the OPLL receiver will be presented at the meeting.

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