100-1000 GHz Bipolar ICs: Device and Circuit Design Principles

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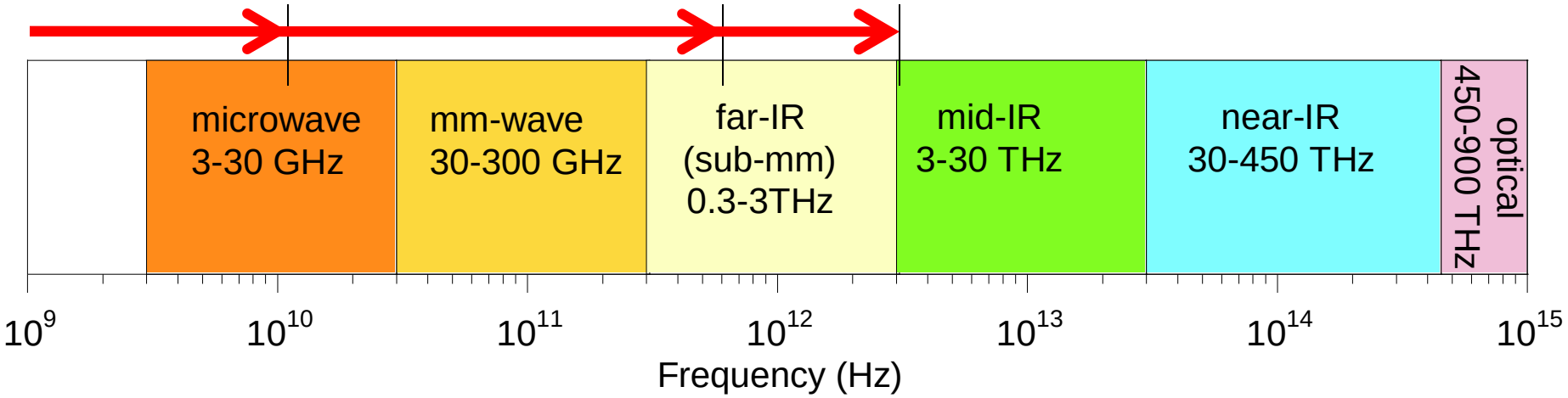
Motivation / Overview

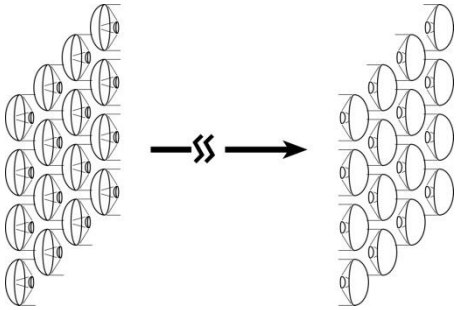
DC to Daylight. Far-Infrared Electronics

How high in frequency can we push electronics ?

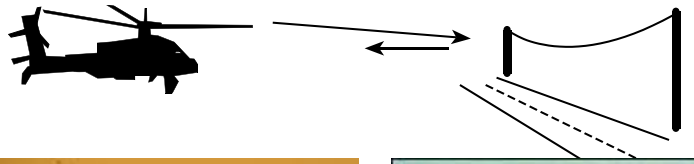


...and what would be do with it ?

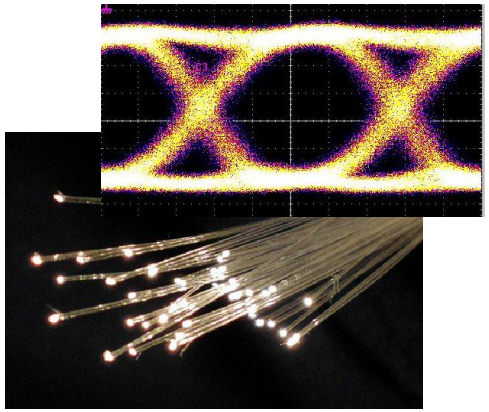
0.3-3 THz radio: vast capacity bandwidth, # channels



0.3- 3 THz imaging systems

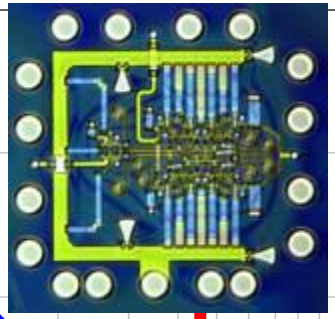


0.1-1 Tb/s optical fiber links

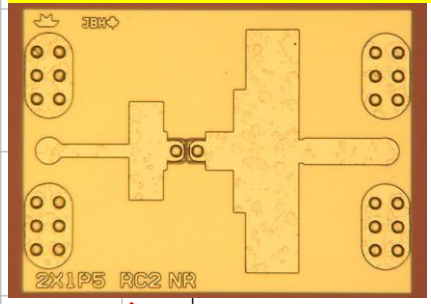


THz Transistors: Not Only For THz Circuits

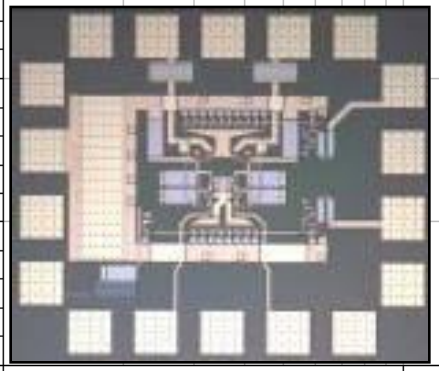
500 GHz digital logic → fiber optics



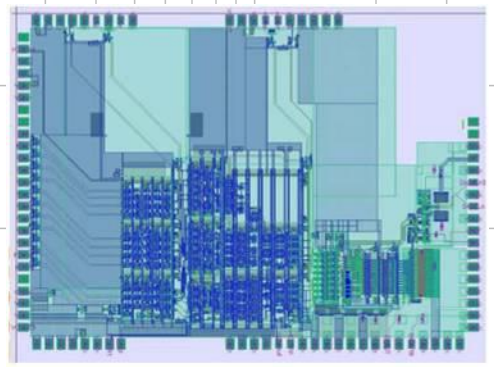
THz amplifiers→ THz radios → imaging, sensing, communications



precision analog design at microwave frequencies → high-performance receivers



Higher-Resolution Microwave ADCs, DACs, DDSs



Transistor Power Gain, dB

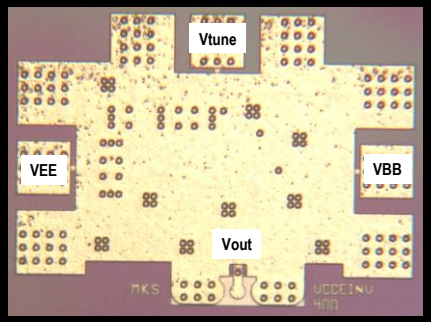
35
30
25
20
15
10
5
0

1E9
1E10
1E11
1E12
3E12

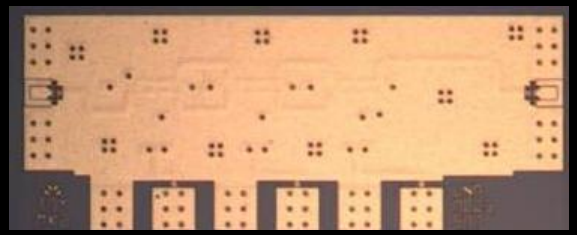
Frequency, Hz

ICs to 600 GHz : Teledyne and UCSB

570 GHz fundamental VCO
M. Seo, TSC
CSIC 2010

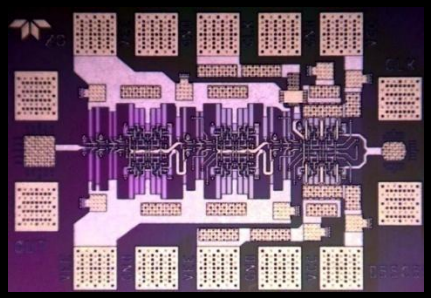


430 GHz low-noise amplifier
M. Seo, TSC
other ICs by J. Hacker



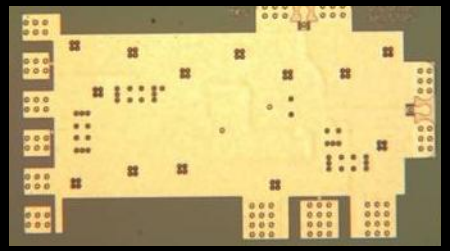
204 GHz static frequency divider (ECL master-slave latch)

Z. Griffith, TSC
CSIC 2010



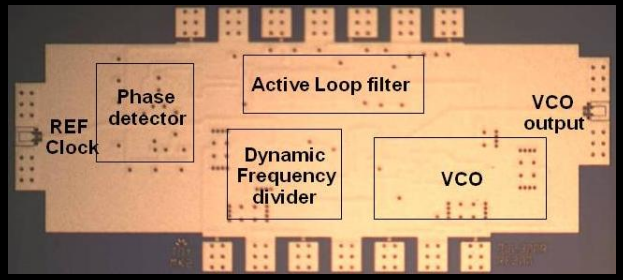
340 GHz dynamic frequency divider

M. Seo, TSC
IEEE MWCL 2010



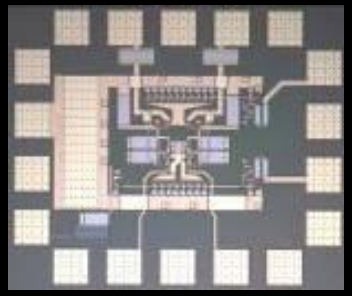
300 GHz fundamental PLL

M. Seo, TSC
IMS 2011



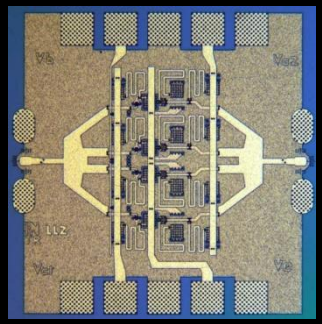
40 GHz op-amp with 54 dBm IP3 at 2 GHz

Z. Griffith, TSC
IMS 2011



220 GHz 48 mW power amplifier

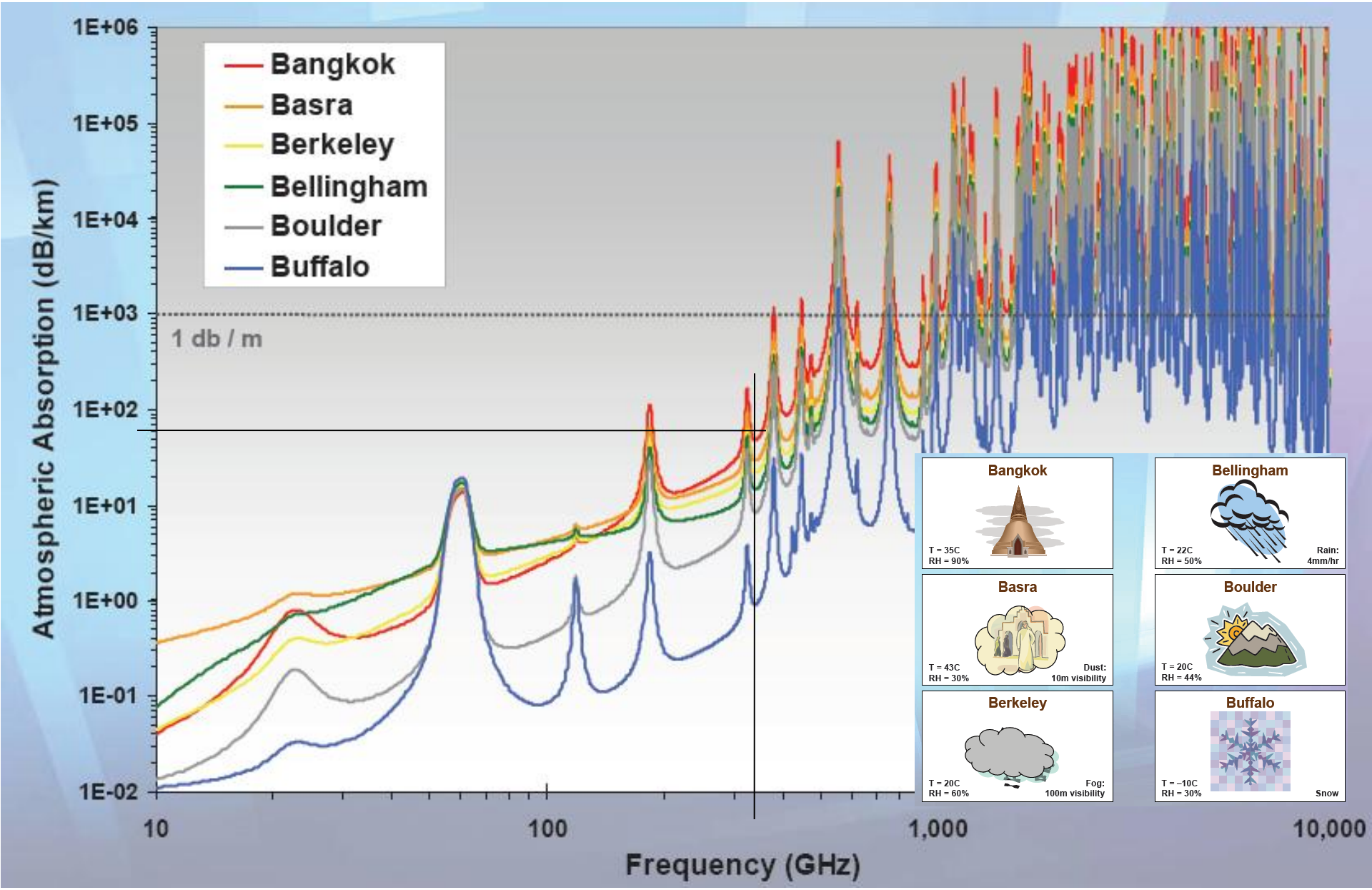
T. Reed, UCSB
CSIC 2011



Other ICs in design:
30-40 GS/s track/hold
optical PLLs
coherent optical receivers
340 GHz arrays

At High Frequencies The Atmosphere Is Opaque

Mark Rosker
IEEE IMS 2007

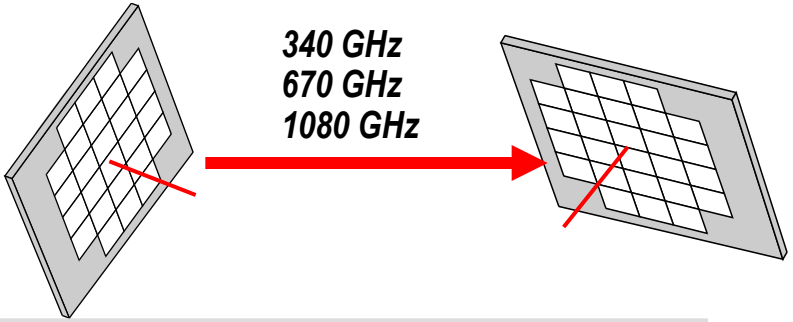


THz Bipolar Transistors: Where Next ?

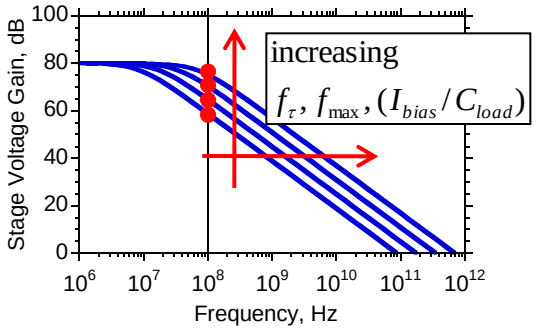
array transmitters: critical for sub-mm-wave radio / radar

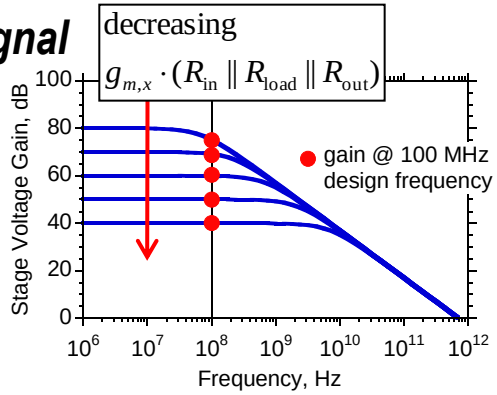
$$\frac{P_{received}}{P_{transmit}} = \frac{N_{receive} N_{transmit}}{16} \frac{\lambda^2}{R^2} e^{-\alpha R}$$

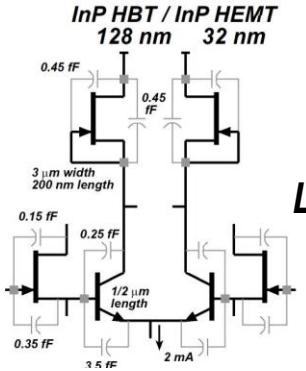
32 x 32 array → 60-90 dB increased SNR →vastly increased range



HBT / HEMT integration for mixed-signal



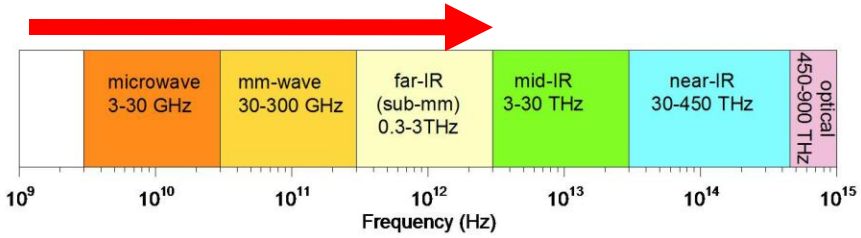




III-V NFET vs. Si PFET active loads: much lower C_{load}/I_{bias}

LSI @ 128 nm node: scaled interconnects high packing density → speed, power

32 nm / 3 THz node, beyond

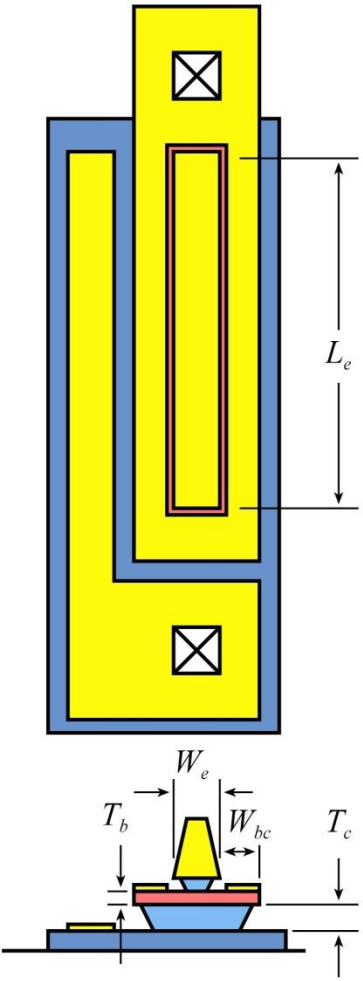


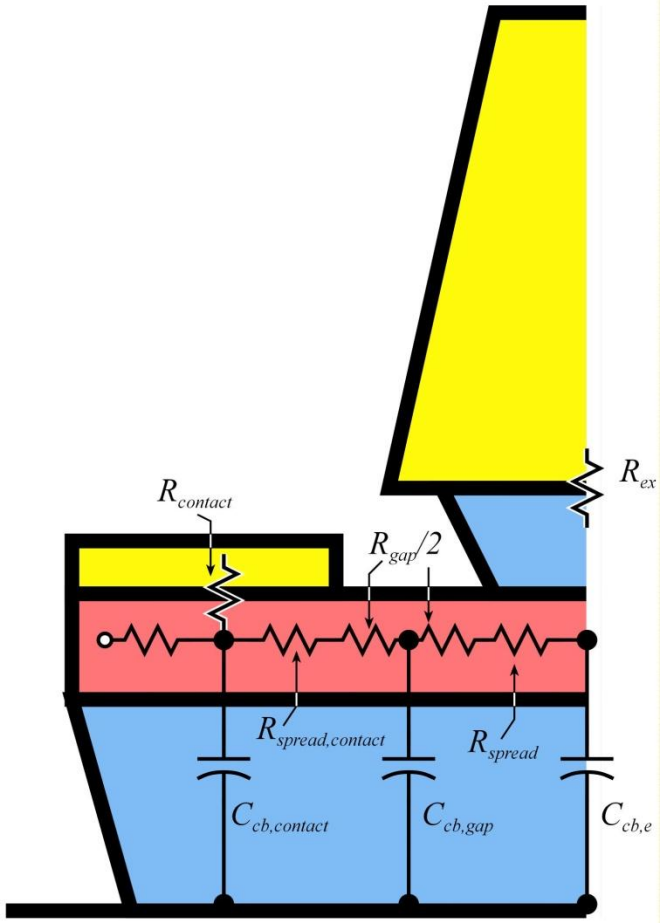
Transition to production

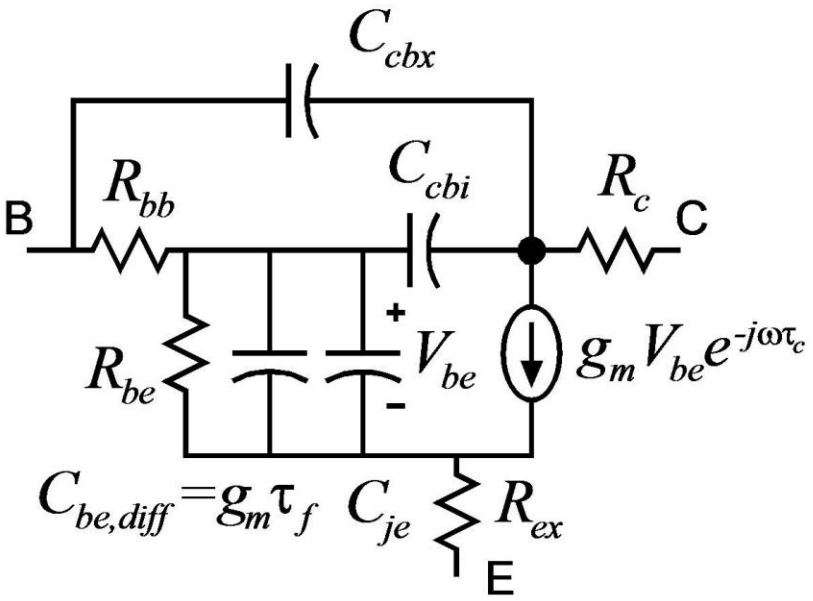
R&D→ pilot → foundry
design tools, reliability, scaled interconnects
CMOS control integration: 3-D, flip chip

Bipolar Transistors: Models, Scaling Laws, State of Art, Roadmaps

Bipolar Transistor: Structure & Models







$$R_{be} = \beta / g_m$$

$$g_m = qI_E / nkT$$

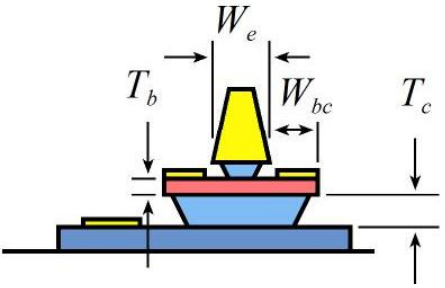
$$C_{be} = C_{je} + g_m(\tau_b + \tau_c)$$

$$\tau_b \approx T_b^2 / 2D_n + T_b / v_{thermal}$$

$$\tau_c \approx T_c / 2v_{"sat"}$$

$$\frac{1}{2\pi f_\tau} = \tau_{base} + \tau_{collector} + C_{je}\frac{nkT}{qI_E} + C_{bc}\left(\frac{nkT}{qI_E} + R_{ex} + R_{coll}\right)$$

Base-Collector Distributed RC Parasitics



(emitter length L_E)

$$R_{ex} = \rho_{contact,emitter} / A_{emitter}$$

$$R_{spread} = \rho_s W_e / 12 L_E$$

$$R_{gap} = \rho_s W_{gap} / 4 L_E$$

$$R_{spread,contact} = \rho_s W_{bc} / 6 L_E$$

$$R_{contact} = \rho_{contact,base} / A_{base\_contacts}$$

$$C_{cb,e} = \varepsilon A_{emitter} / T_c$$

$$C_{cb,gap} = \varepsilon A_{gap} / T_c$$

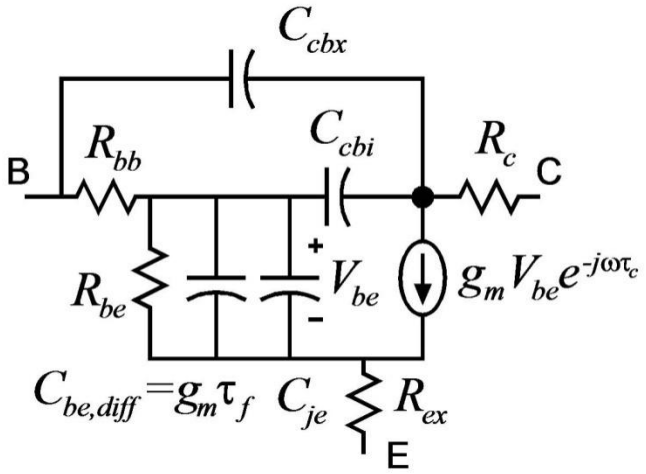
$$C_{cb,contact} = \varepsilon A_{base\_contacts} / T_c$$

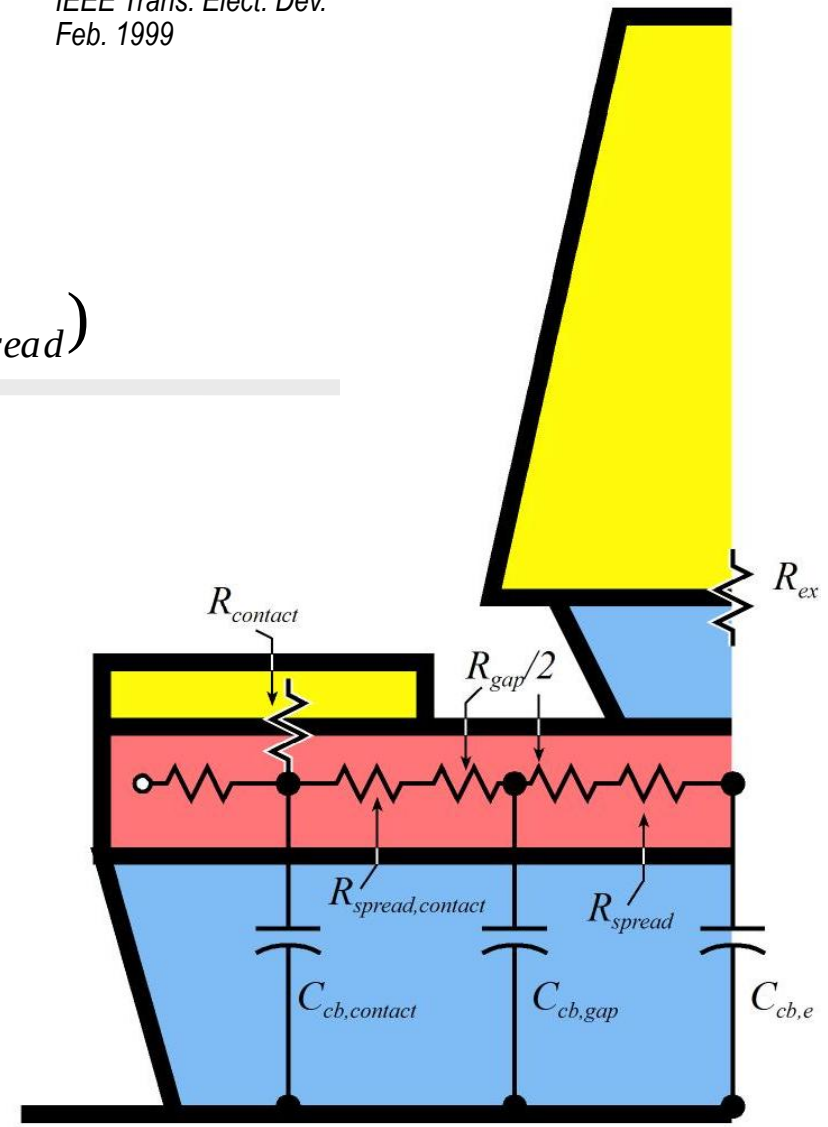
$R_{bb}C_{cb}$ Time Constant, F_{max}, Simple Hybrid-π model

$$f_{\max} \cong \sqrt{f_\tau / 8\pi R_{bb} C_{cbi}} \text{ where}$$

$$\tau_{cb} = R_{bb}C_{cbi} = C_{cb,contact}R_{contact}$$
$$+ C_{cb,gap}(R_{contact} + R_{spread,contact} + R_{gap}/2)$$
$$+ C_{cb,e}(R_{contact} + R_{spread,contact} + R_{gap} + R_{spread})$$

Vaidyanathan & Pulfrey
IEEE Trans. Elect. Dev.
Feb. 1999





R_{bb} = true total base resistance

$C_{cbi} + C_{cbx}$ = true total C_{cb}

$C_{cbi} : C_{cbx}$ ratio set to fit $f_{\max}$ from above

Key 2nd-Order Effects in III-V HBTs: Omitted for Brevity

Current - induced velocity overshoot : decreases τ_c

Nakajima, Japanese Journal of Applied Physics, Feb. 1997

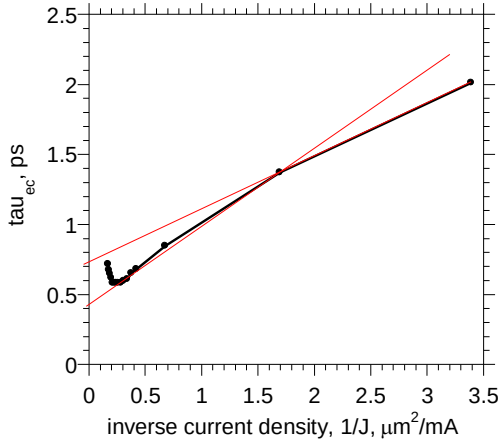
Voltage modulation of collector velocity : increases τ_c

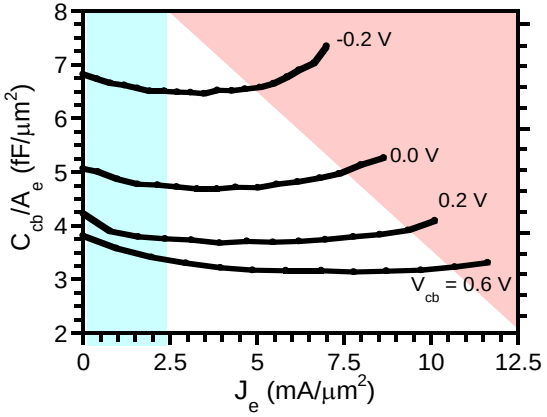
Partial C_{cb} cancellation by collector velocity modulation.

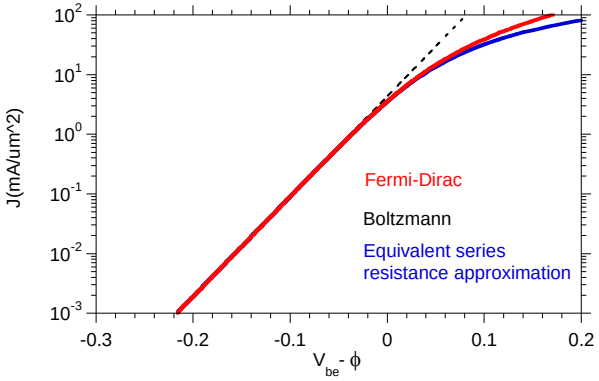
Betser and Ritter , IEEE Trans. Elect. Dev., April 1999
Urteaga & Rodwell, IEEE Trans. Elect. Dev., July 2003

Degenerate electron injection into base : increases R_{ex}

Rodwell, Le, Brar, Proc IEEE , February 2008
Jain & Rodwell, IEEE Electron. Dev. Lett., to be published (2011)



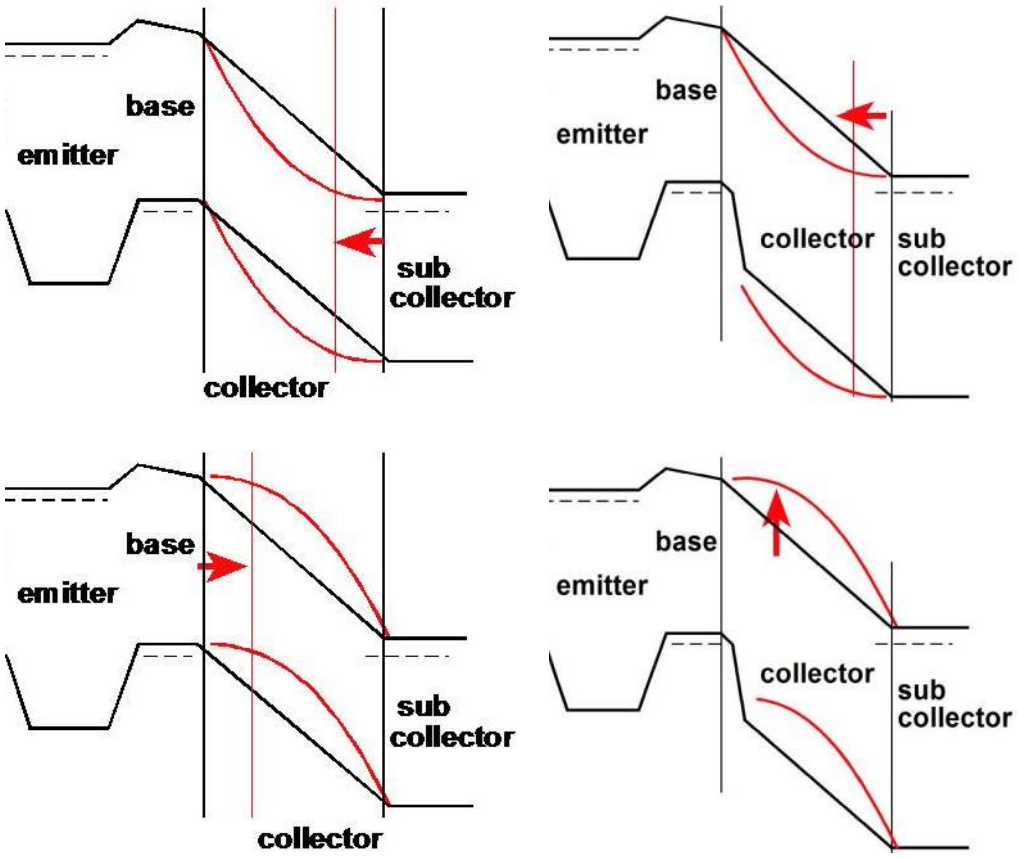




More detailed information regarding III-V bipolar transistor physics and design:
http://www.ece.ucsb.edu/Faculty/rodwell/publications_and_presentations/publications/2009_may_IPRM_short_course_rodwell.pdf

Space Charge, Kirk Effect, Minimum C_{cb} charging time

SiGe HBT ***InP DHBT***



Collector Depletion Layer Collapse

$$V_{cb,\min} + \phi > +(qN_d)(T_c^2 / 2\varepsilon)$$

Collector Field Collapse

$$V_{cb} + \phi > +(J / v_{sat} - qN_d)(T_c^2 / 2\varepsilon)$$

$$\Rightarrow \quad J_{\max} = 2\varepsilon v_{eff} (V_{cb} + V_{cb,\min} + 2\phi) / T_c^2$$

Note that $V_{be} \cong \phi$, hence $(V_{cb} + \phi) \cong V_{ce}$

$$C_{cb}\Delta V_{LOGIC} / I_C = (\varepsilon A_{\text{collector}} / T_c)(\Delta V_{LOGIC} / I_C) = \frac{\Delta V_{LOGIC}}{(V_{CE} + V_{CE,\min})} \left(\frac{A_{\text{collector}}}{A_{\text{emitter}}} \right) \left(\frac{T_C}{2v_{eff}} \right)$$

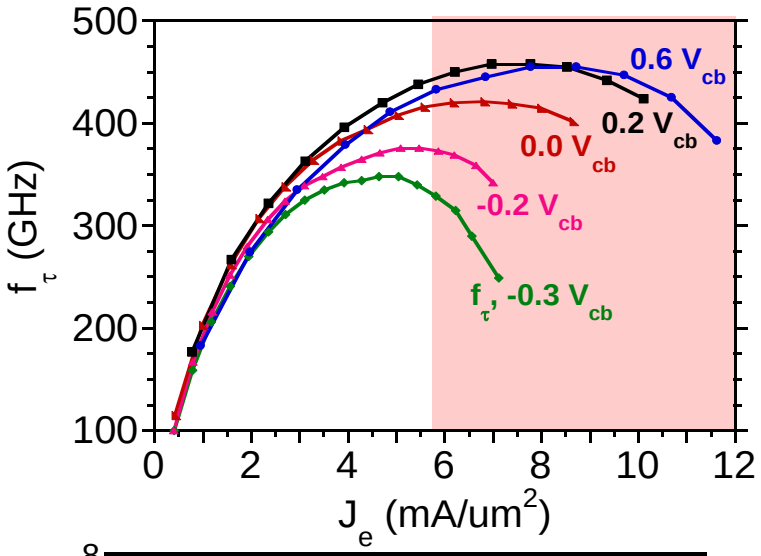
Collector capacitance charging time minimized by setting $J = J_{max}$

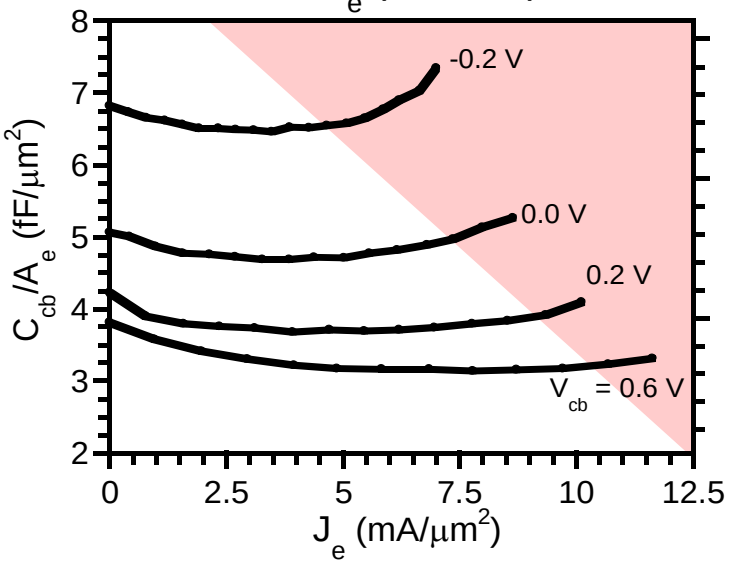
...if so, charging time scales linearly with collector thickness.

Space-Charge-Limited Current (Kirk effect) in BJTs

Decreased (f_τ , $f_{\max}$), increased C_{cb} at high J.

Kirk threshold increases with increased V_{ce}.



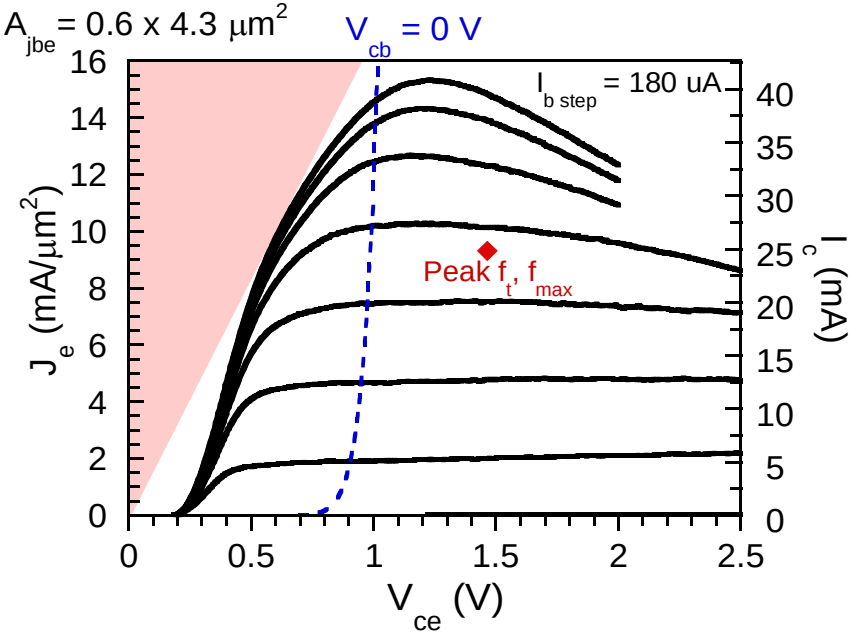


Increase in $V_{ce,sat}$ with increased J

$$\frac{dV_{ce}}{dI_c} = R_{\text{space-charge}} = \frac{T_c^2}{2\varepsilon v_{sat} A_{effective}}$$

where the effective collector current flux area is

$$A_{effective} \approx L_E\left(W_E + 2T_C\right)$$

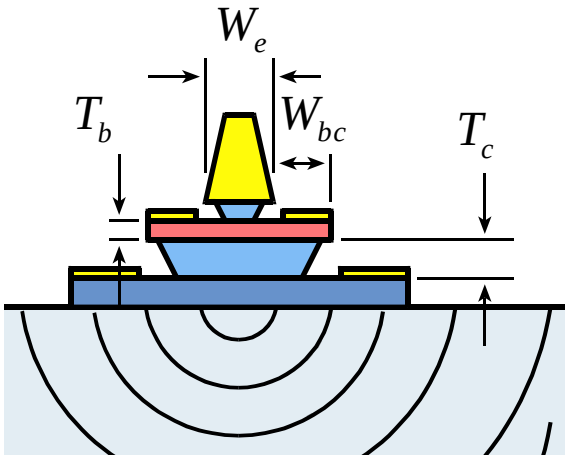


Bipolar Transistor Design

$$\tau_b \approx T_b^2 / 2D_n$$

$$\tau_c = T_c / 2v_{sat}$$

$$C_{cb} = \varepsilon A_c / T_c$$



(emitter length L_E)

$$I_{c,\max} \propto v_{sat} A_e \left(V_{\text{ce,operating}} + V_{\text{ce,punch-through}}\right) / T_c^2$$

$$\Delta T \propto \frac{P}{L_E}\left[1 + \ln\left(\frac{L_e}{W_e}\right)\right]$$

$$R_{ex} = \rho_{\text{contact}} / A_e$$

$$R_{bb} = \rho_{\text{sheet}}\left(\frac{W_e}{12L_e} + \frac{W_{bc}}{6L_e}\right) + \frac{\rho_{\text{contact}}}{A_{\text{contacts}}}$$

Bipolar Transistor Design: Scaling

$$\tau_b \approx T_b^2 / 2D_n$$

$$\tau_c = T_c / 2v_{sat}$$

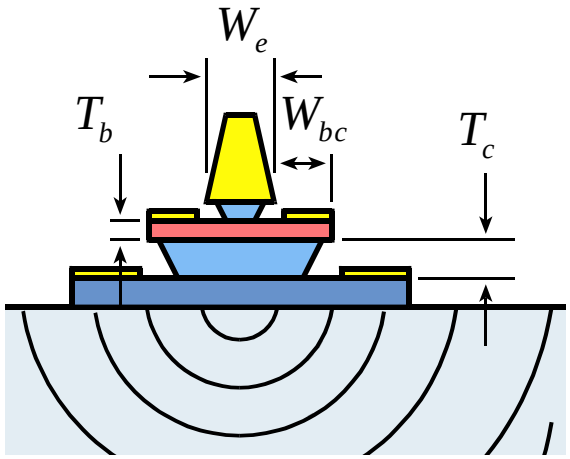
$$C_{cb} = \varepsilon A_c / T_c$$

$$I_{c,\max} \propto v_{sat} A_e (V_{\text{ce,operating}} + V_{\text{ce,punch-through}}) / T_c^2$$

$$\Delta T \propto \frac{P}{L_E}\left[1 + \ln\left(\frac{L_e}{W_e}\right)\right]$$

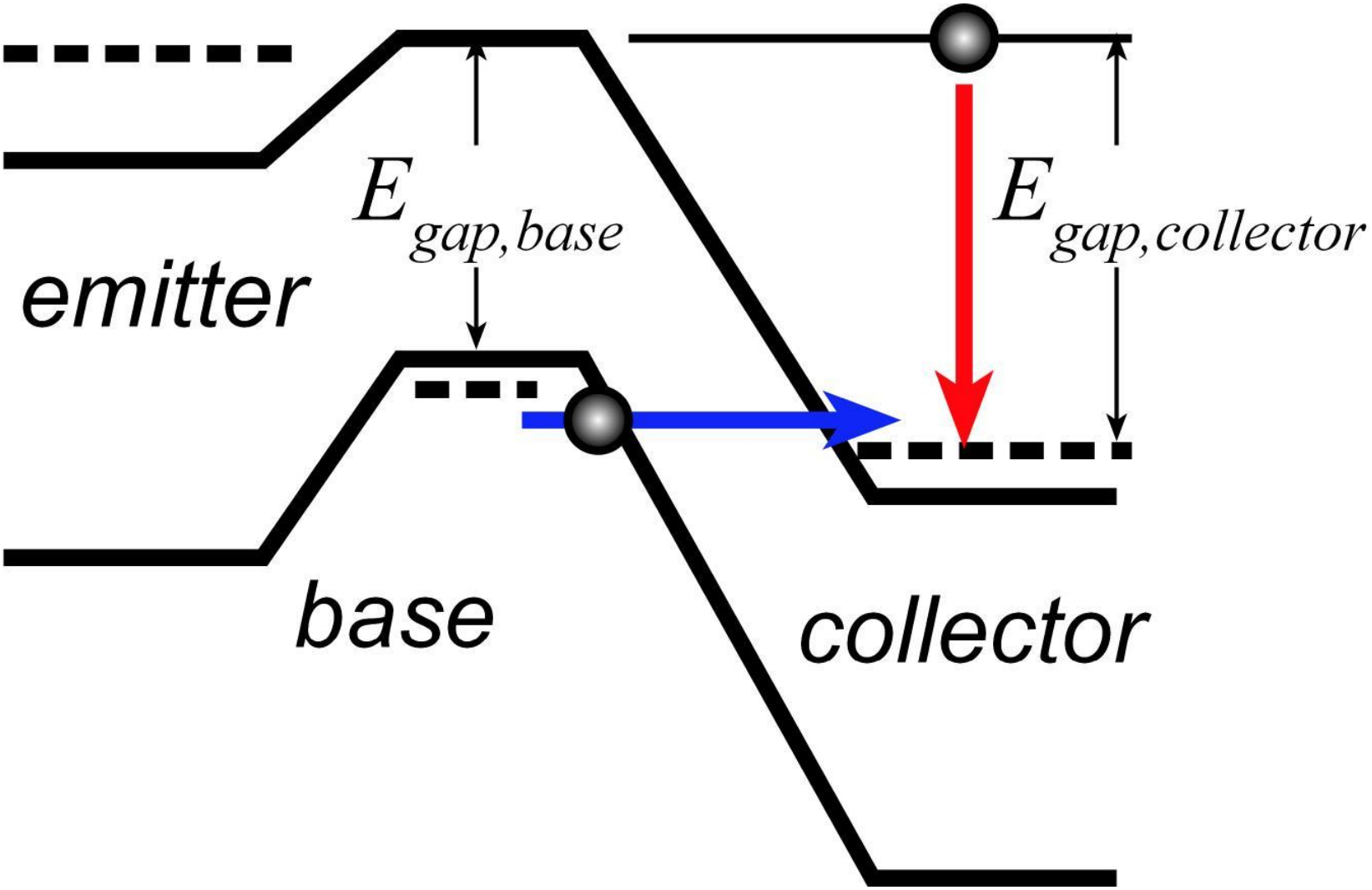
$$R_{ex} = \rho_{\text{contact}} / A_e$$

$$R_{bb} = \rho_{\text{sheet}}\left(\frac{W_e}{12L_e} + \frac{W_{bc}}{6L_e}\right) + \frac{\rho_{\text{contact}}}{A_{\text{contacts}}}$$



(emitter length L_E)

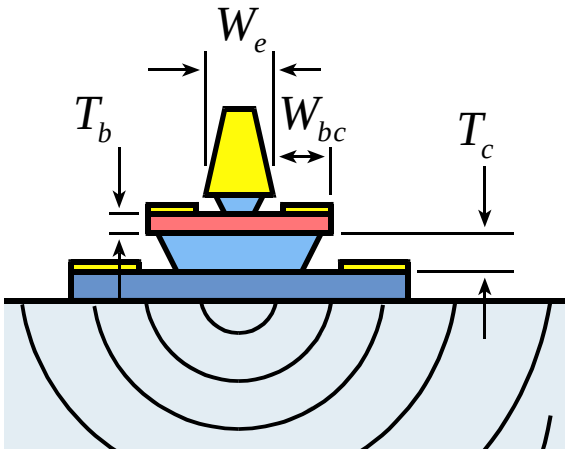
Breakdown is Never Less Than The Bandgap



Bipolar Transistors: Scaling Laws, Scaling Roadmap

scaling laws: to double bandwidth

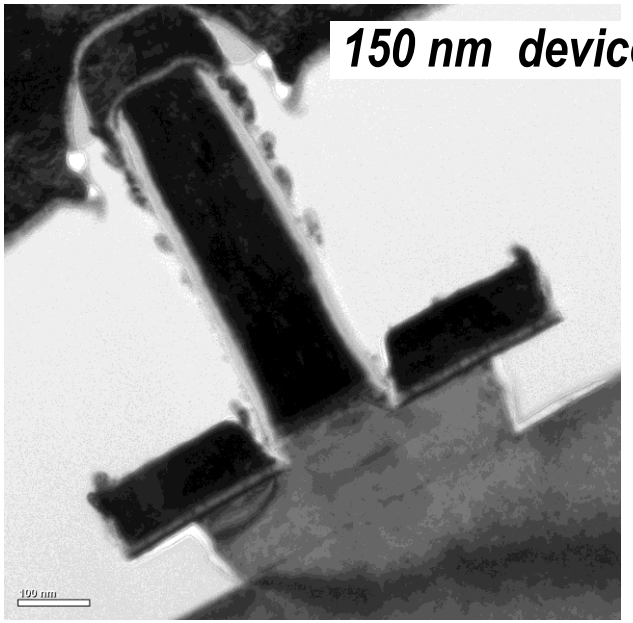
HBT parameter	change
emitter & collector junction widths	decrease 4:1
current density (mA/μm²)	increase 4:1
current density (mA/μm)	constant
collector depletion thickness	decrease 2:1
base thickness	decrease 1.4:1
emitter & base contact resistivities	decrease 4:1



(emitter length L_E)

InP HBT scaling roadmap

emitter	512	256	128	64	32 nm width
	16	8	4	2	1 Ω·μm² access ρ
base	300	175	120	60	30 nm contact width,
	20	10	5	2.5	1.25 Ω·μm² contact ρ
collector	150	106	75	53	37.5 nm thick,
	4.5	9	18	36	72 mA/μm² current density
	4.9	4	3.3	2.75	2-2.5 V, breakdown
f_τ	370	520	730	1000	1400 GHz
f_{max}	490	850	1300	2000	2800 GHz
power amplifiers	245	430	660	1000	1400 GHz
digital 2:1 divider	150	240	330	480	660 GHz



Recent InP HBT Results: Urteaga et al, DRC 2011

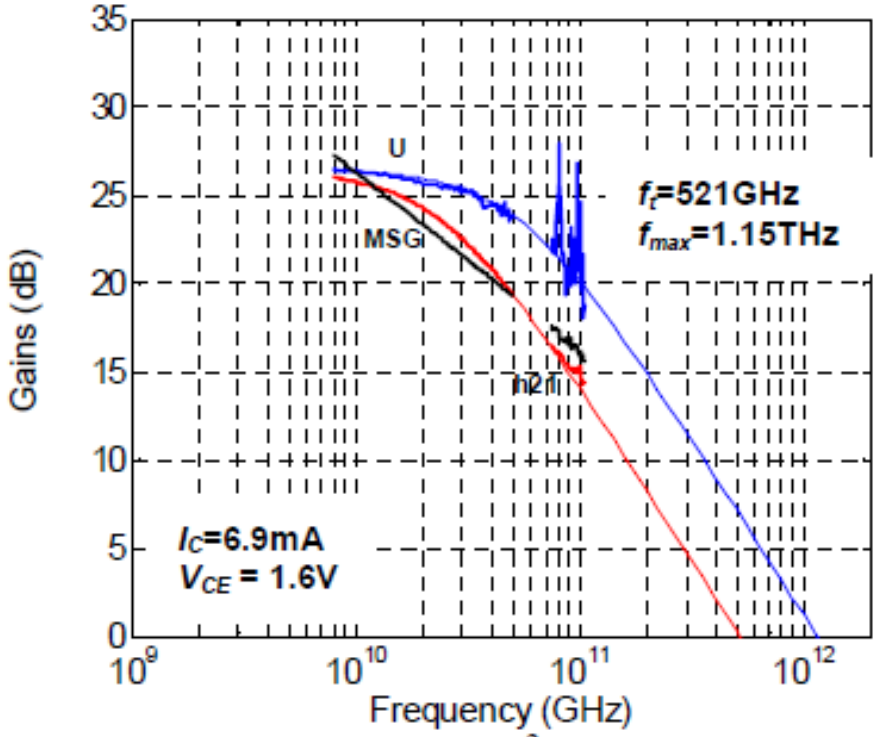


Fig. 3 RF gains of 0.13x2μm^2 HBT

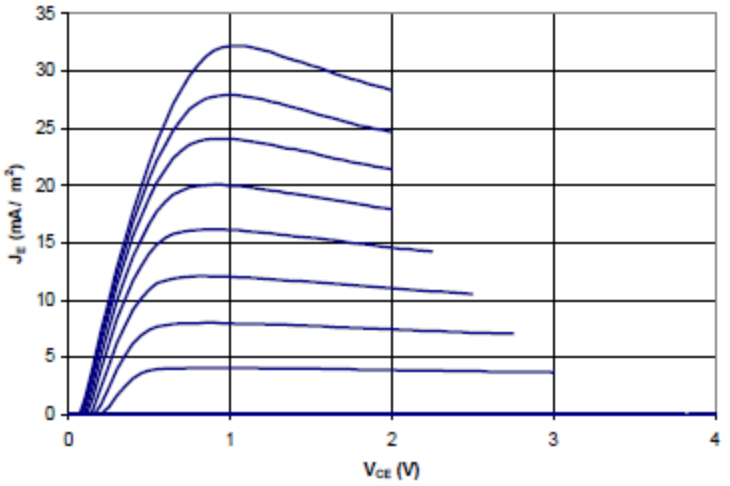


Fig. 2 Common-emitter IV characteristics of 130nm HBT normalized to emitter area

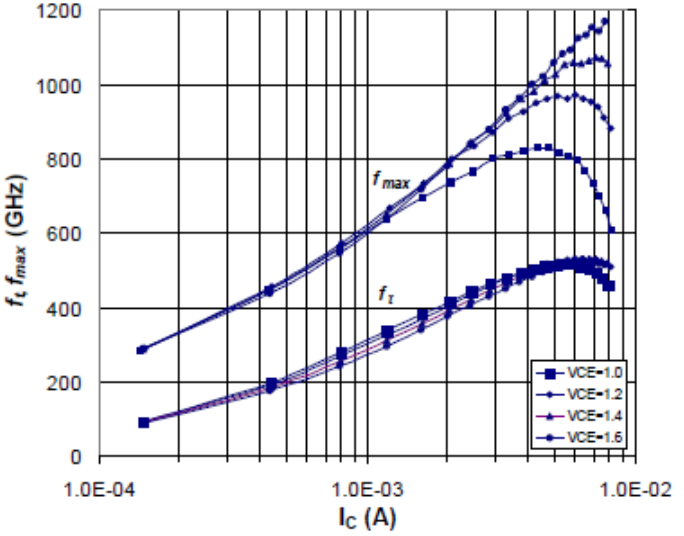


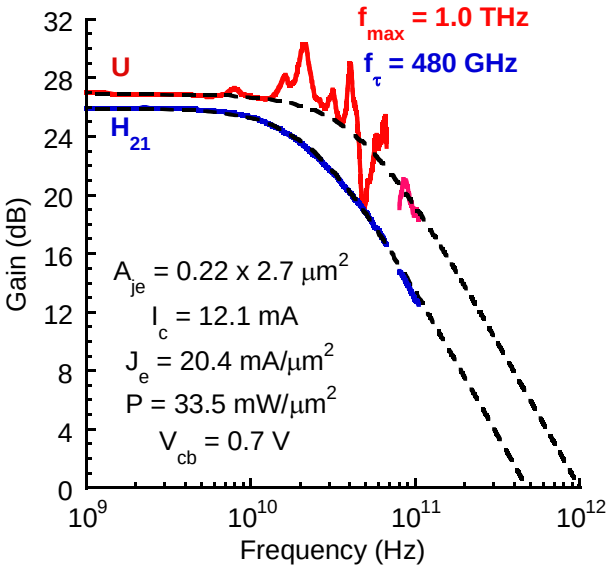
Fig. 4 f_t and f_{max} versus collector current at varying values of V_{CE} for 0.13x2μm^2 HBT

130nm InP DHBTs with f_t>0.52THz and f_{max} >1.1THz

M. Urteaga[1], R. Pierson[1], P. Rowell[1], V. Jain[2], E. Lobisser[2], M.J.W. Rodwell[2]
[1]Teledyne Scientific Company, Thousand Oaks, CA 93160. [2]Department of ECE, University of California, Santa Barbara, CA 93106. E-mail: murteaga@teledyne-si.com

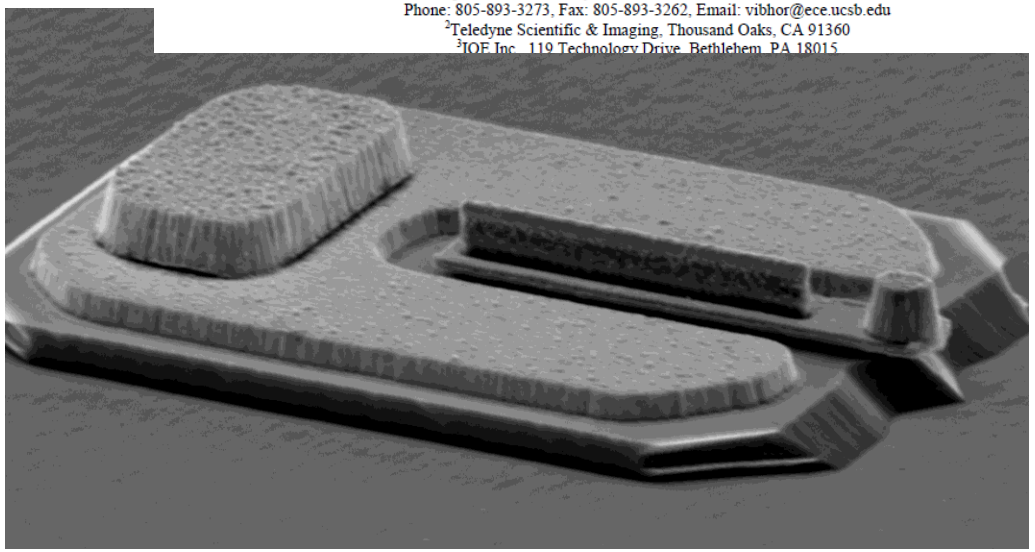
Recent InP HBT Results: Jain et al, DRC 2011

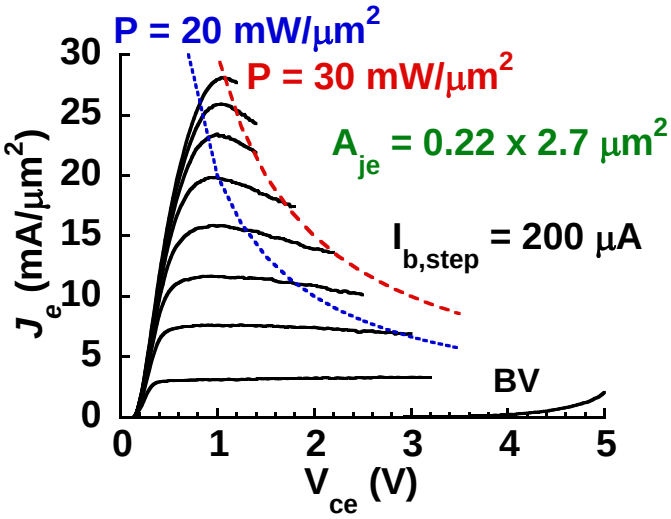
30nm emitter, *30nm* base, *100nm* collector

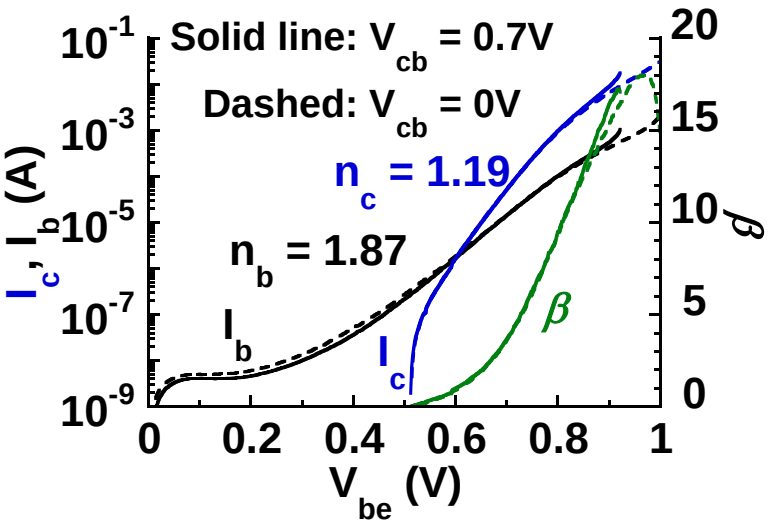


1.0 THz f_{max} InP DHBTs in a refractory emitter and self-aligned base process for reduced base access resistance

Vibhor Jain[1], Johann C. Rode[1], Han-Wei Chiang[1], Ashish Baraskar[1], Evan Lobisser[1], Brian J. Thibeault[1], Mark Rodwell[1], Miguel Urteaga[2], D. Loubychev[3], A. Snyder[3], Y. Wu[3], J. M. Fastenau[3], W.K. Liu[3]
[1]ECE Department, University of California, Santa Barbara, CA 93106-9560
Phone: 805-893-3273, Fax: 805-893-3262, Email: vibhor@ece.ucsb.edu
[2]Teledyne Scientific & Imaging, Thousand Oaks, CA 91360
[3]IQE Inc., 119 Technology Drive, Bethlehem, PA 18015







Can we make a 1 THz SiGe Bipolar Transistor ?

Simple physics clearly drives scaling

transit times, C_{cb}/I_c

→ thinner layers, higher current density

high power density → narrow junctions

small junctions→ low resistance contacts

Key challenge: Breakdown

15 nm collector → very low breakdown

Also required:

low resistivity Ohmic contacts to Si

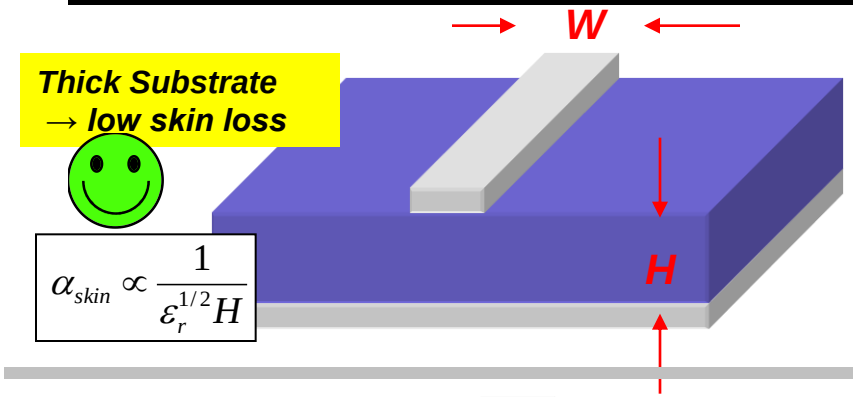
very high current densities: heat

	InP	SiGe	
emitter	64	18	nm width
	2	**0.6**	$\Omega\cdot\mu m^2$ access ρ
base	64	18	nm contact width,
	2.5	**0.7**	$\Omega\cdot\mu m^2$ contact ρ
collector	53	**15**	nm thick
	36	125	$mA/\mu m^2$
	2.75	**1.3?**	V, breakdown
f_τ	**1000**	**1000**	GHz
f_{max}	**2000**	**2000**	GHz
PAs	1000	1000	GHz
digital	480	480	GHz
(2:1 static divider metric)			

Assumes collector junction 3:1 wider than emitter.
Assumes SiGe contacts no wider than junctions

Interconnects

III-V MIMIC Interconnects -- Classic Substrate Microstrip

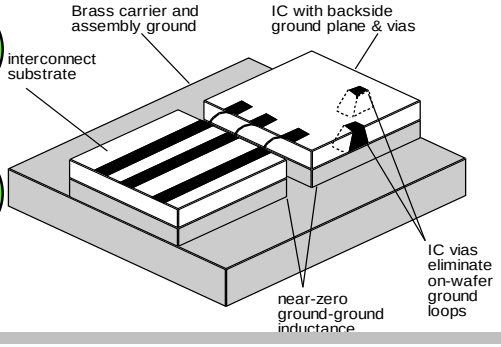


Thick Substrate → low skin loss

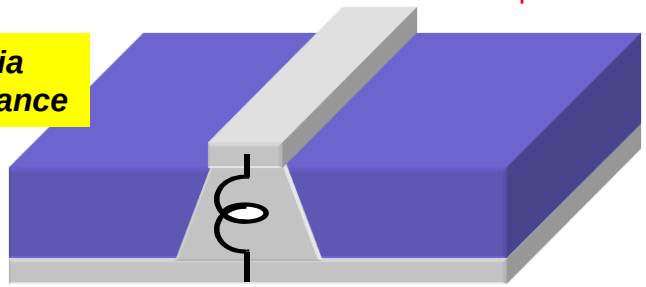
$$\alpha_{skin} \propto \frac{1}{\varepsilon_r^{1/2} H}$$

Zero ground inductance in package

No ground plane breaks in IC

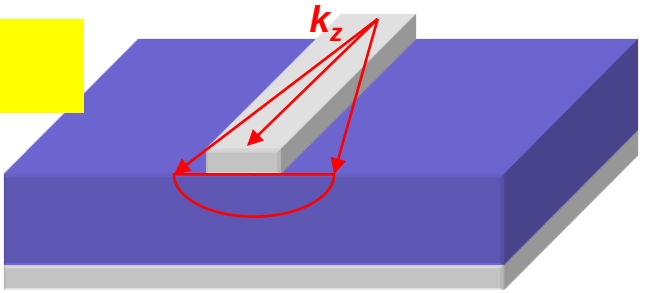


High via inductance



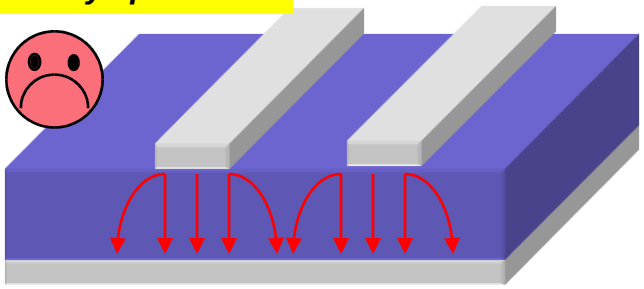
12 pH for 100 μm substrate -- 7.5 Ω @ 100 GHz

TM substrate mode coupling



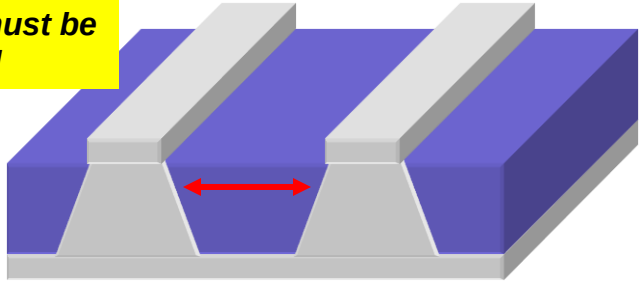
Strong coupling when substrate approaches ~λ_d / 4 thickness

lines must be widely spaced



Line spacings must be ~3(substrate thickness)*

ground vias must be widely spaced

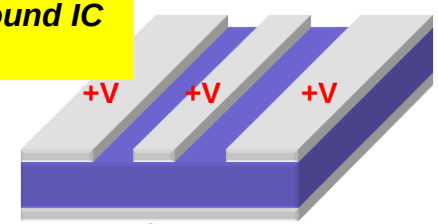


all factors require very thin substrates for >100 GHz ICs
→ lapping to ~50 μm substrate thickness typical for 100+ GHz

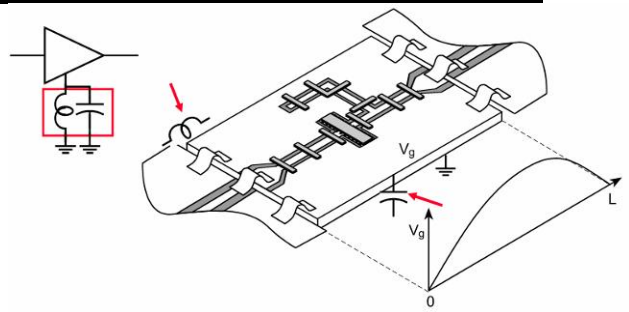
Coplanar Waveguide

No ground vias
No need (???) to thin substrate

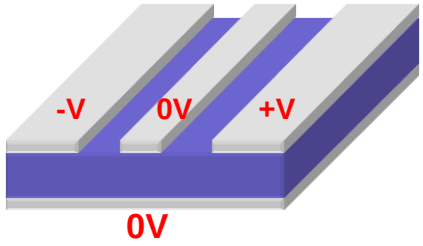
Hard to ground IC to package



Parasitic microstrip mode

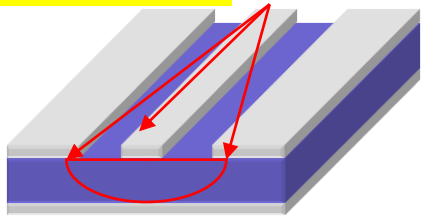


ground plane breaks → loss of ground integrity



Parasitic slot mode

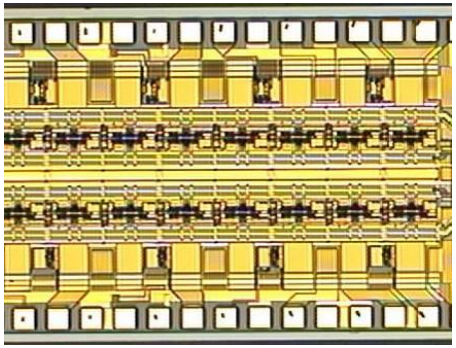
substrate mode coupling or substrate losses



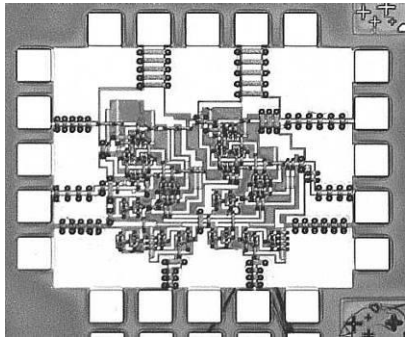
III-V: semi-insulating substrate→ substrate mode coupling

Silicon conducting substrate → substrate conductivity losses

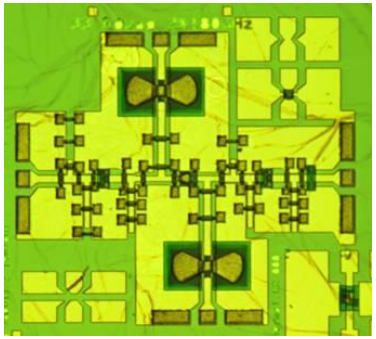
Repairing ground plane with ground straps is effective only in simple ICs
In more complex CPW ICs, ground plane rapidly vanishes
→ common-lead inductance → strong circuit-circuit coupling



40 Gb/s differential TWA modulator driver
note CPW lines, fragmented ground plane



35 GHz master-slave latch in CPW
note fragmented ground plane



175 GHz tuned amplifier in CPW
note fragmented ground plane

poor ground integrity

loss of impedance control

ground bounce

coupling, EMI, oscillation

III-V MIMIC Interconnects -- Thin-Film Microstrip

narrow line spacing → IC density

no substrate radiation, no substrate losses

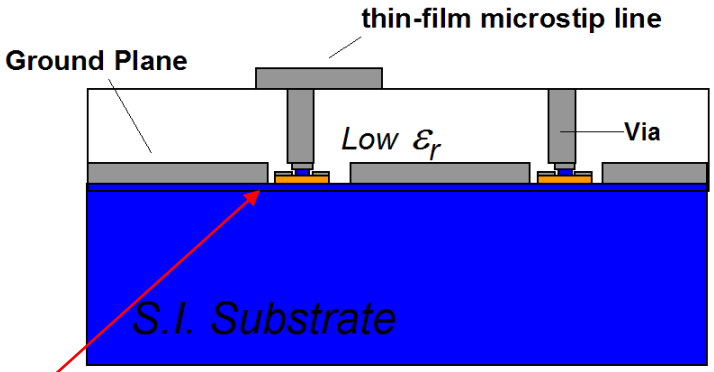
fewer breaks in ground plane than CPW

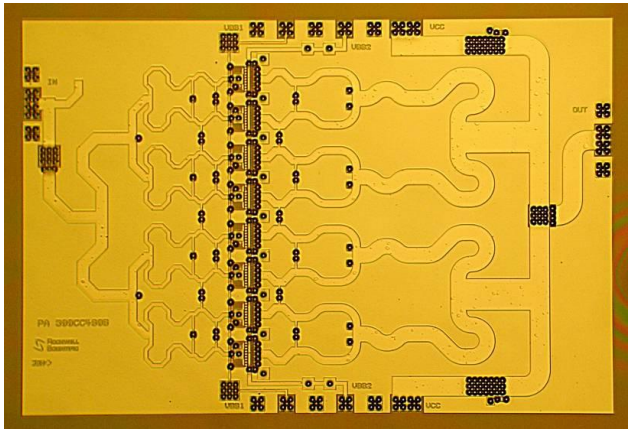
... but ground breaks at device placements

still have problem with package grounding

...need to flip-chip bond

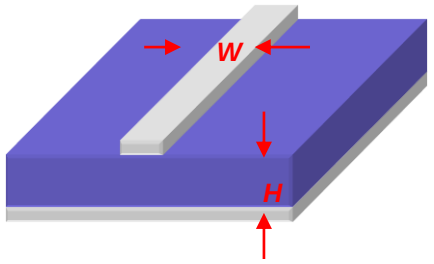
thin dielectrics → narrow lines
→ high line losses
→ low current capability
→ no high-Z_o lines





InP 34 GHz PA
(Jon Hacker , Teledyne)

$$Z_o \sim \frac{\eta_o}{\varepsilon_r^{1/2}}\left(\frac{H}{W+H}\right)$$



III-V MIMIC Interconnects -- Inverted Thin-Film Microstrip

narrow line spacing → IC density

Some substrate radiation / substrate losses

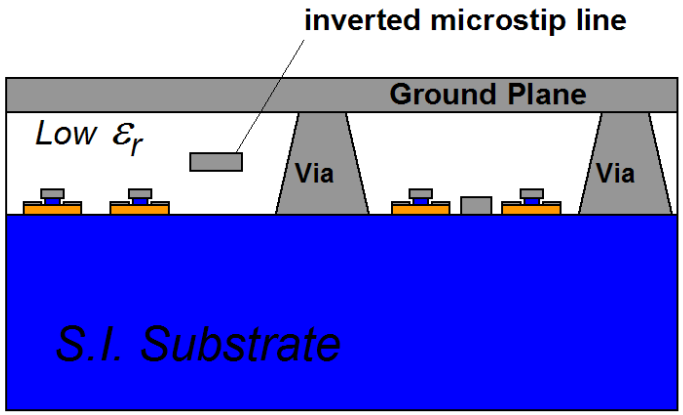
No breaks in ground plane

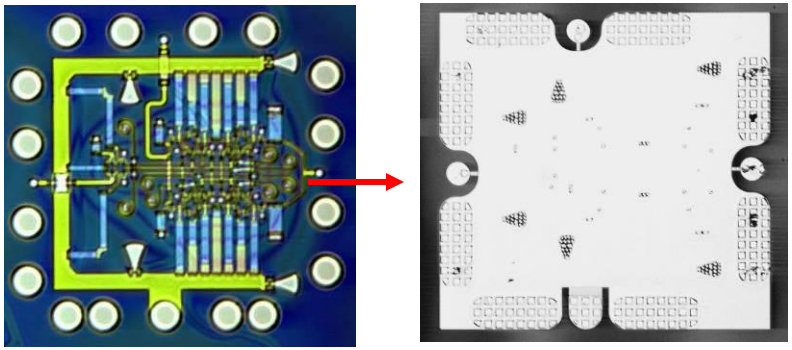
... no ground breaks at device placements

still have problem with package grounding

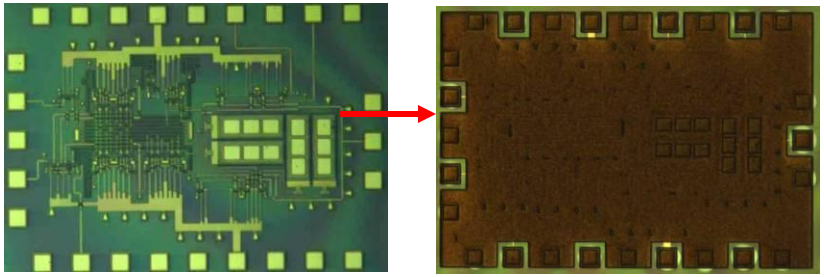
...need to flip-chip bond

thin dielectrics → narrow lines
→ high line losses
→ low current capability
→ no high-Z_o lines



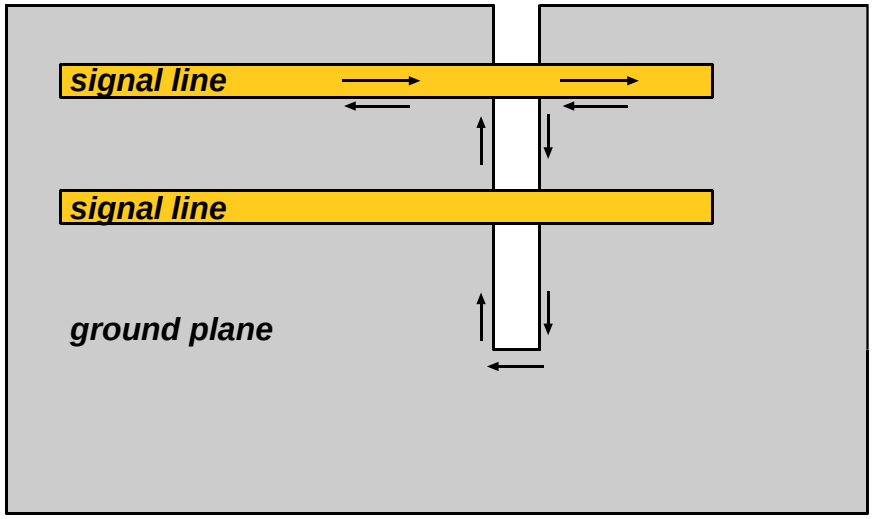


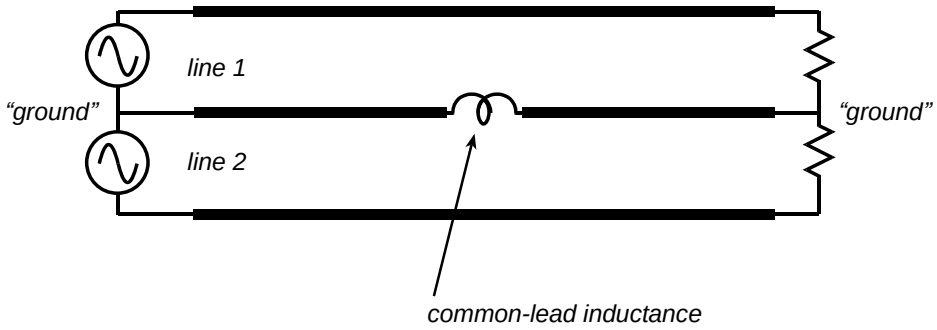
InP 150 GHz master-slave latch



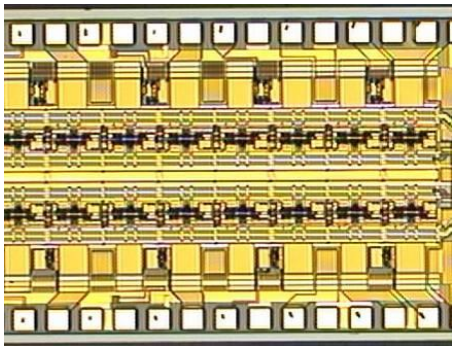
InP 8 GHz clock rate delta-sigma ADC

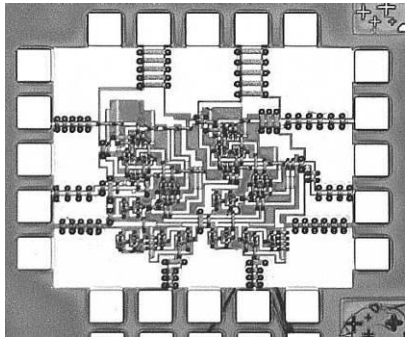
If It Has Breaks, It Is Not A Ground Plane !

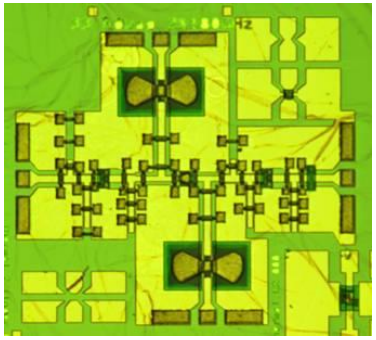




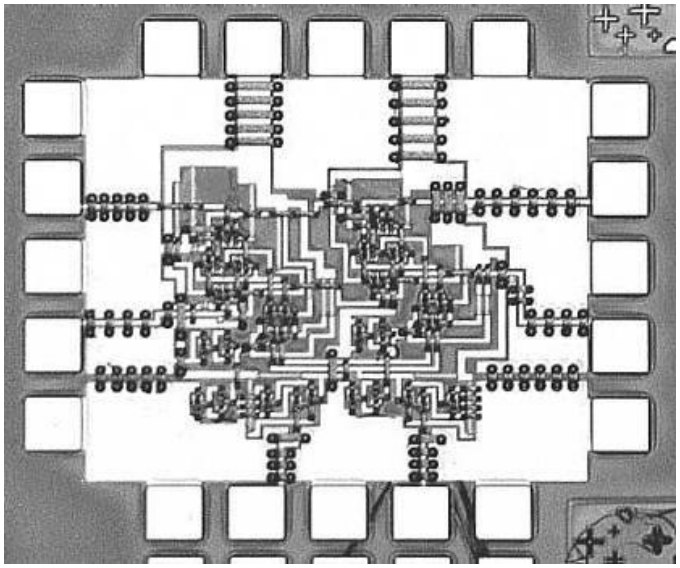
coupling / EMI due to poor ground system integrity is common in high-frequency systems
whether on PC boards
...or on ICs.



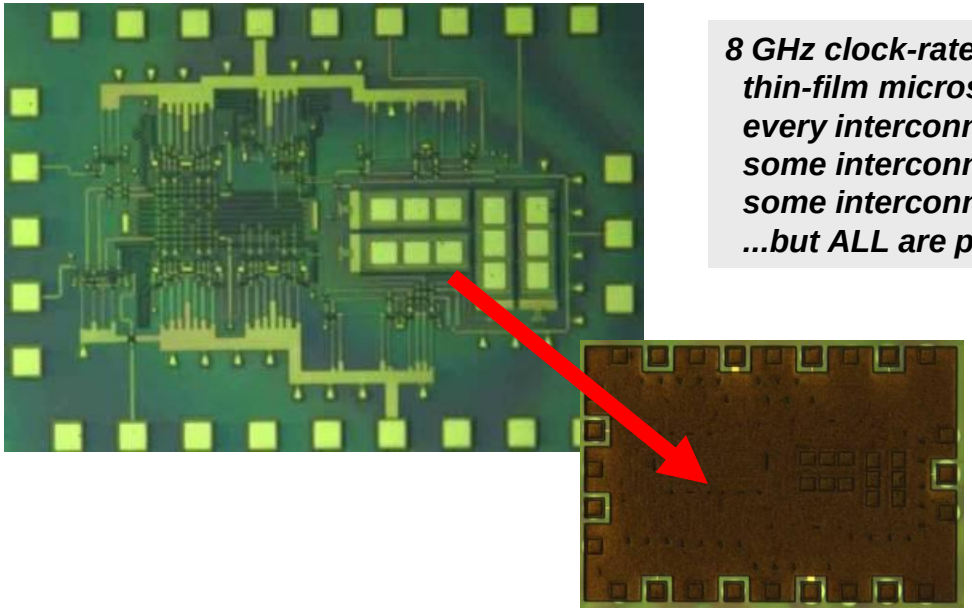




No clean ground return ? → interconnects can't be modeled !



35 GHz static divider
- *interconnects have no clear local ground return*
- *interconnect inductance is non-local*
- *interconnect inductance has no compact model*



8 GHz clock-rate delta-sigma ADC
- *thin-film microstrip wiring*
- *every interconnect can be modeled as microstrip*
- *some interconnects are terminated in their Zo*
- *some interconnects are not terminated*
- *...but ALL are precisely modeled*

InP 8 GHz clock rate delta-sigma ADC

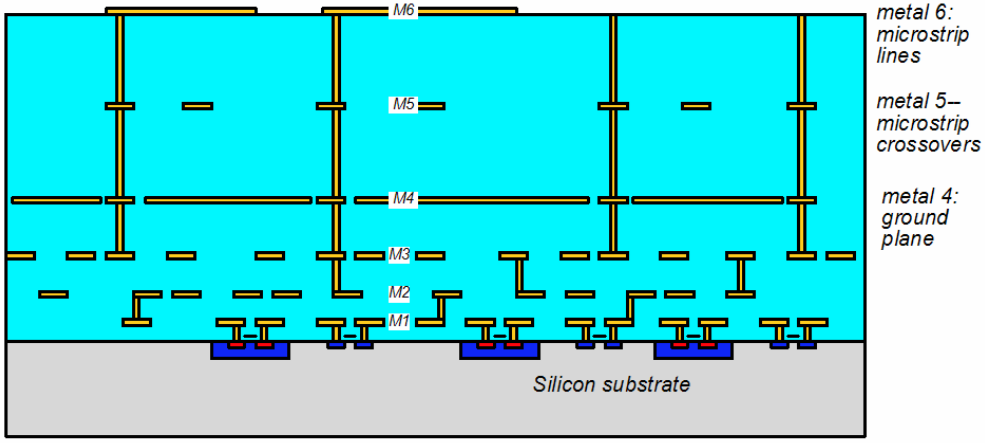
VLSI mm-wave interconnects with ground integrity

narrow line spacing → IC density

no substrate radiation, no substrate losses

negligible breaks in ground plane

negligible ground breaks @ device placements



Also:
Ground plane at *intermediate level* permits critical signal paths to cross supply lines, or other interconnects without coupling.
(critical signal line is placed above ground, other lines and supplies are placed below ground)

still have problem with package grounding

...need to flip-chip bond

thin dielectrics → narrow lines
→ high line losses
→ low current capability
→ no high-Z_o lines

Modeling Interconnects, Passives in Tuned (RF) IC's

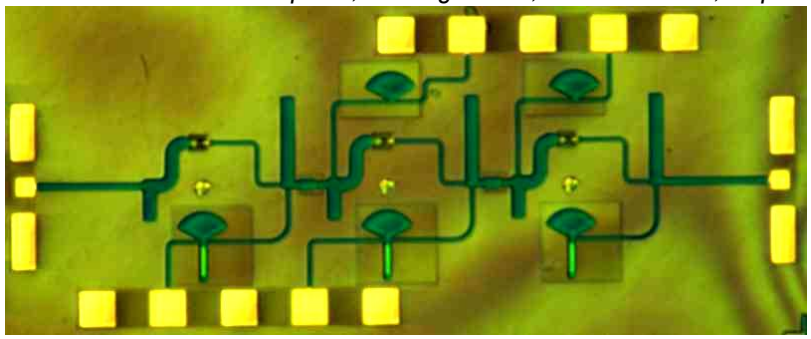
Interconnects* are *tuning elements

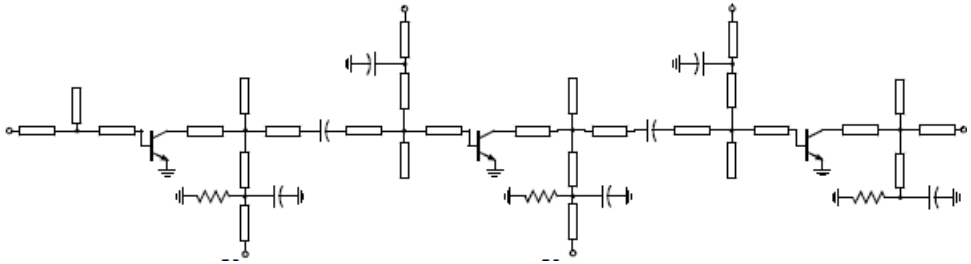
Narrow bandwidths→ precision is critical

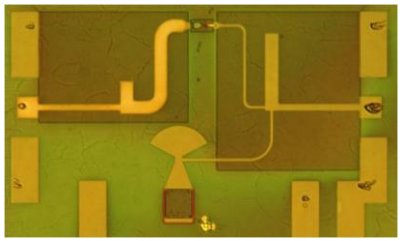
Initial IC simulation uses CAD-systems' library of passive element models.

Final design: 2.5-Dimensional electromagnetic simulation of:
lines, junctions, stubs, capacitors, resistors, pads.

150-200 GHz HBT amplifier, Urteaga et al, IEEE JSSCC , Sept. 2003

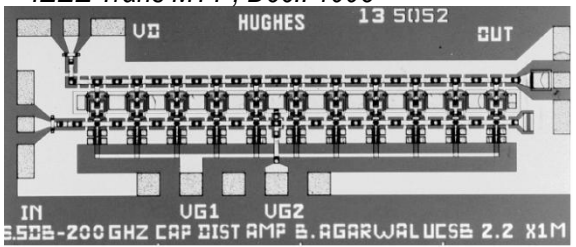






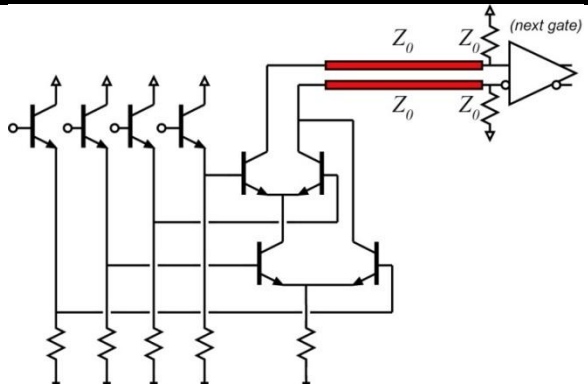
185GHz HBT amplifier, Urteaga et al, IEEE IMS, May. 2001

1-180GHz HBT amplifier, Agarwal et al, IEEE Trans MTT , Dec.. 1998

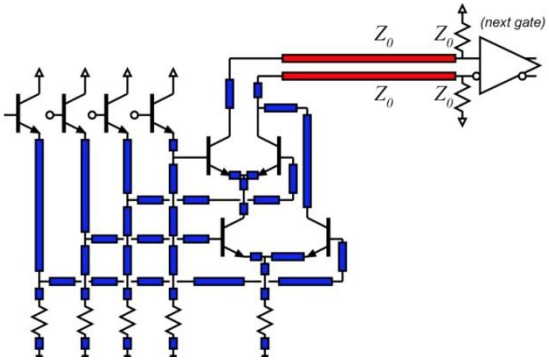


Modeling Interconnects: Digital & Mixed-Signal IC's

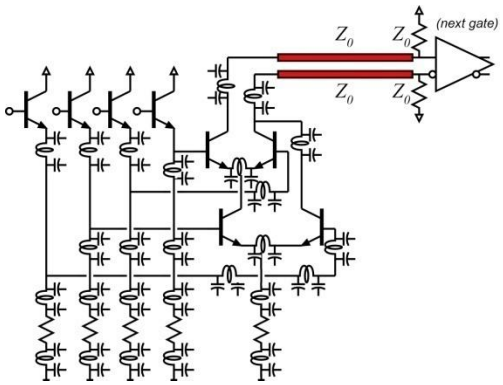
longer interconnects:
lines terminated in Zo → no reflections.



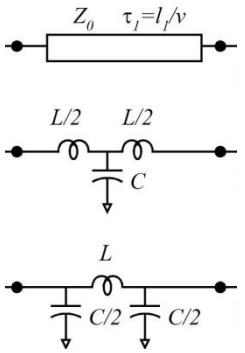
Shorter interconnects:
lines NOT terminated in Zo .
*But they are *still* transmission-lines.*
Ignore their effect at your peril !



If length << wavelength,
or line delay<<risetime,
short interconnects behave
as lumped L and C.

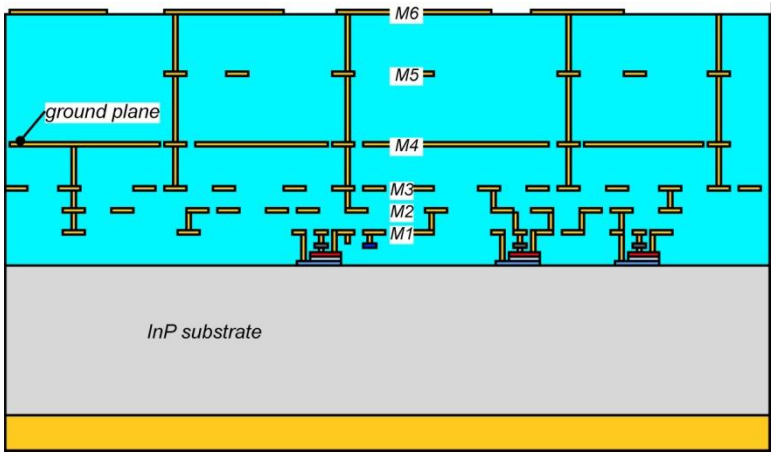


$$L = Z_0 \tau\,,$$
$$C = \tau / Z_0,$$
$$\tau = l / v$$



Design Flow: Digital & Mixed-Signal IC's

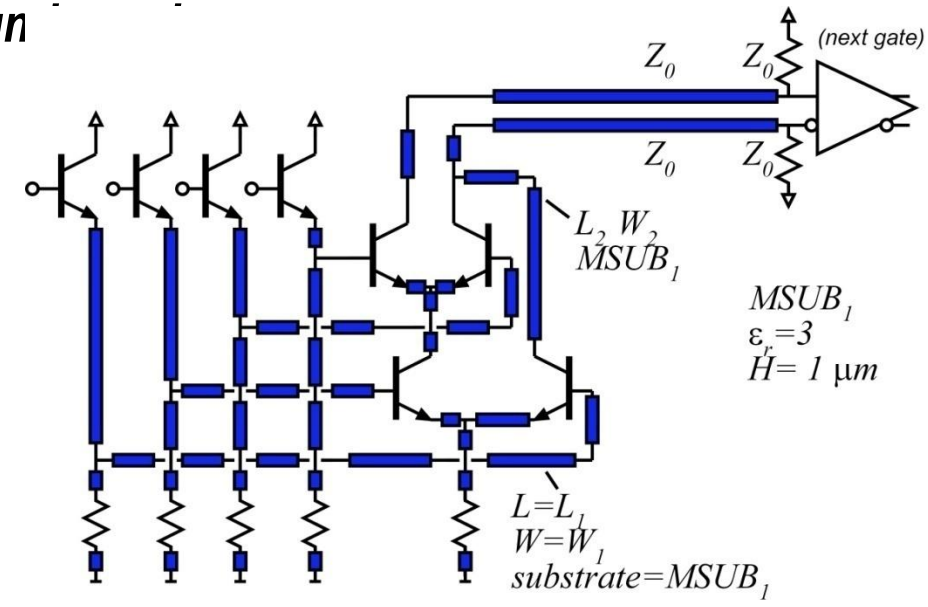
All interconnects: thin-film microstrip environment.
<u>Continuous</u> ground on one plane.



2.5-D simulations run on representative lines.
various widths, various planes
same reference (ground) plane.

Simulation data manually fit to CAD line model
effective substrate ε_r, effective line-groun

Width, length, substrate of each line entered on CAD schematic.
rapid data entry, rapid simulation.

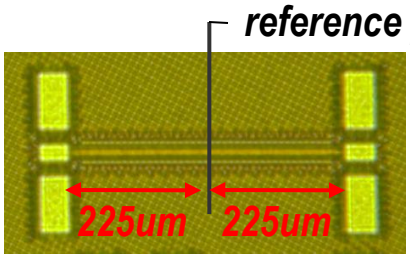


Resistors and capacitors:
2.5-D simulation→ RLC fit
RLC model used in simulation.

Network analyzer Calibration... on-wafer LRL

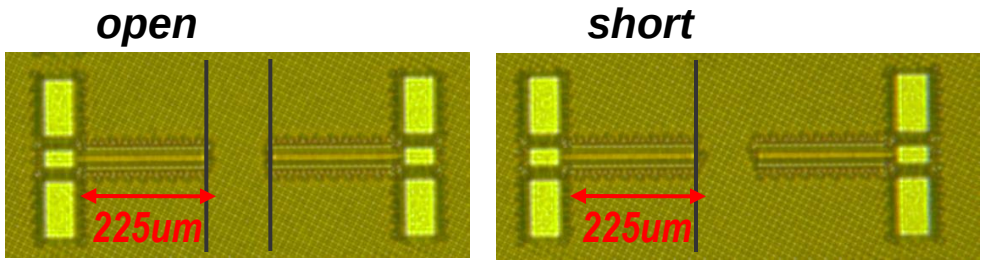
On-Wafer Through-Reflect-Line (TRL) Calibration

Through



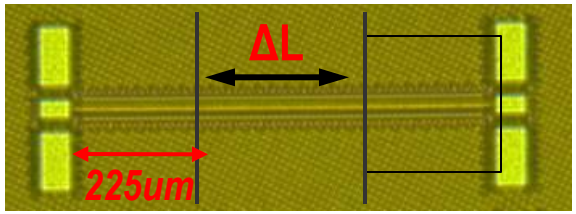
Through line should be long for large probe separation.
Minimizes probe-probe coupling.
Measurements normalized to the line characteristic impedance.

Reflect



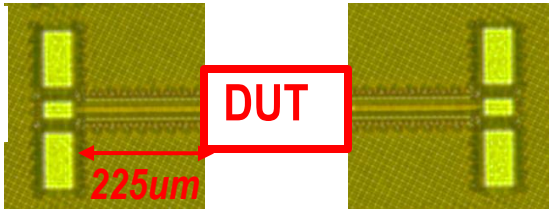
Either open or short needed.
Standards need not be accurate.
"Open" must have Γ closer to that of open than that of short.
Ports 1 & 2 must be symmetric.

Line



ΔL= 90 deg @center frequency.
$\lambda/8<\Delta L<3\lambda/8$

Device Under Test



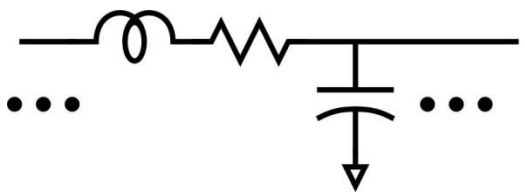
Please see also:
http://www.ece.ucsb.edu/Faculty/rodwell/publications_and_presentations/publications/204vg.ppt

On-Wafer TRL: Ongoing Issues

High-f_{max} transistors have very small ($C_{cb} \rightarrow Y_{12} \rightarrow S_{12}$)

Measurements show small background Y_{12}.
...even with extended reference planes.
Particular difficulty in extracting Mason's Unilateral gain.
→ Corrupts f_{max} measurement, model extraction.

Measurements normalized to line Z_0.
...line impedance is complex at lower frequencies.
→ must correct for complex Z_o in measurements.
excessive line resistance degrades precision.



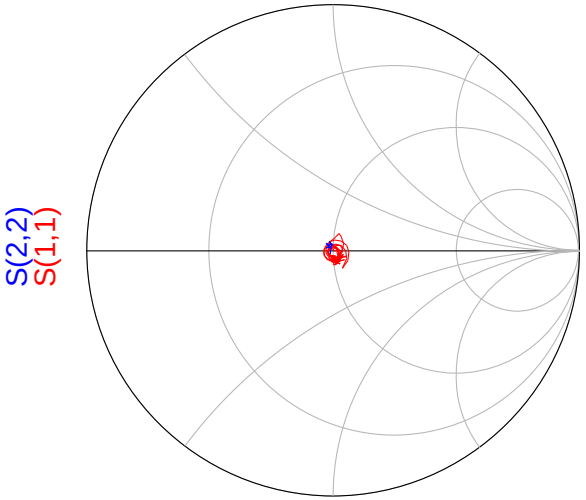
$$Z_O = \sqrt{\frac{R(j\omega) + j\omega L}{j\omega C}}$$

TRL precision greatly impaired if lines couple to substrate;
CPW line standards do not work well.

Verification of 140-220GHz TRL Calibration

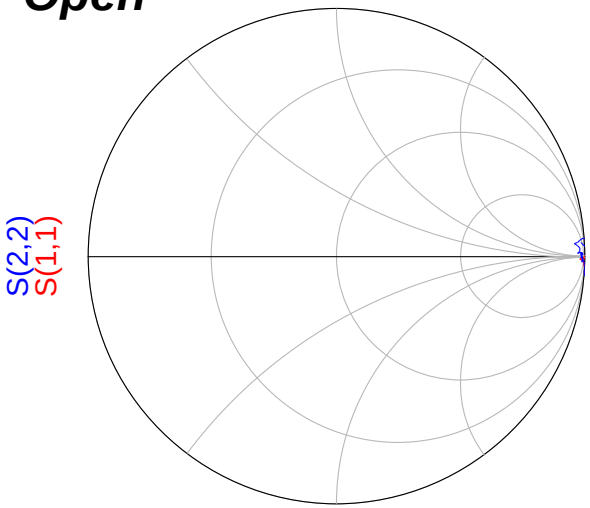
M. Seo

Through



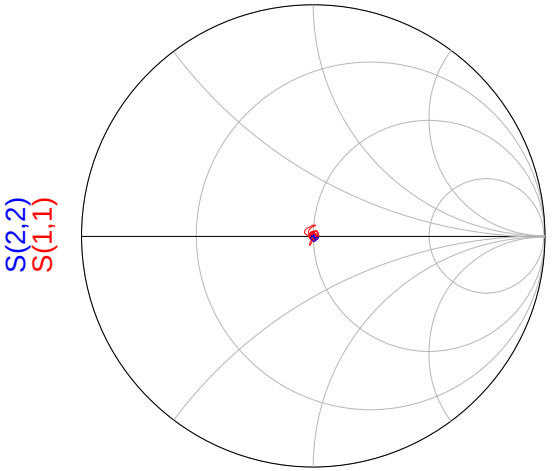
freq (140.0GHz to 200.0GHz)

Open

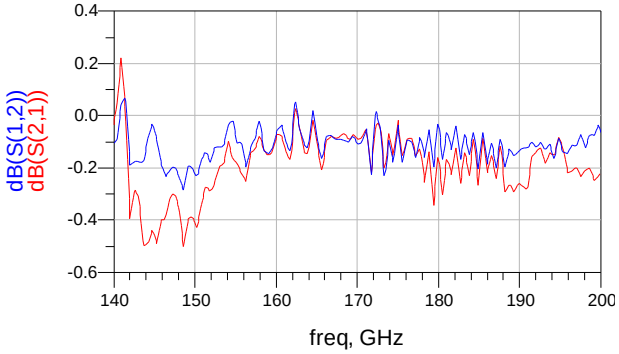


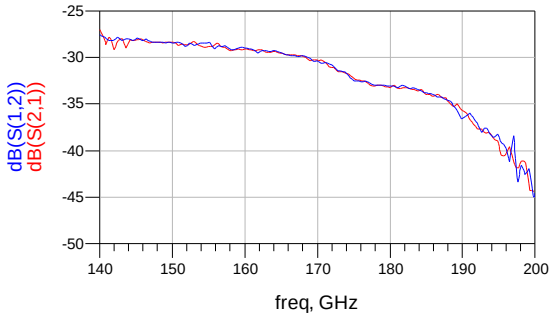
freq (140.0GHz to 200.0GHz)

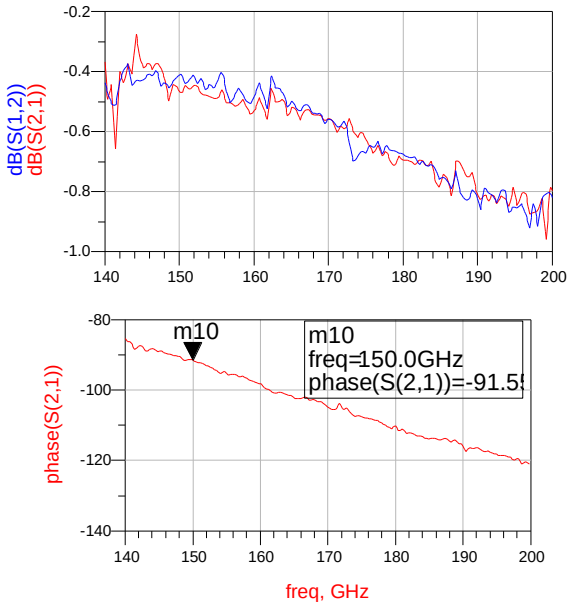
Line



freq (140.0GHz to 200.0GHz)

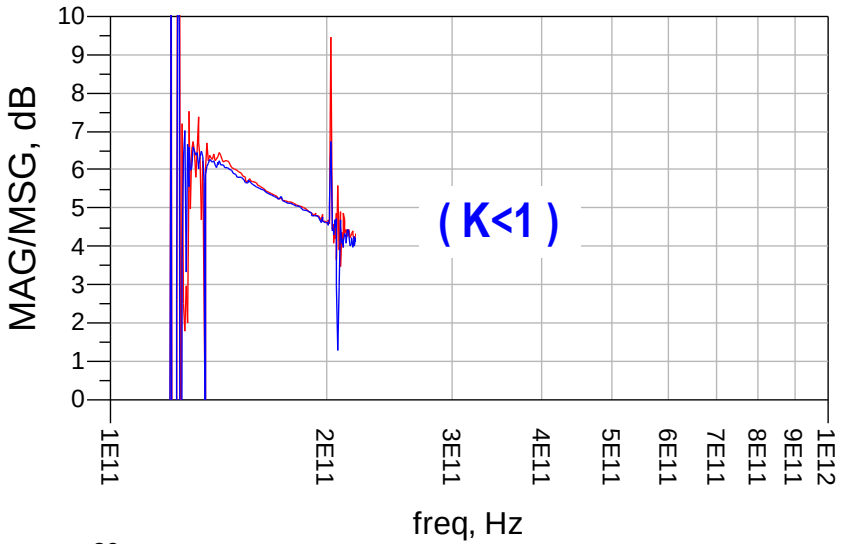


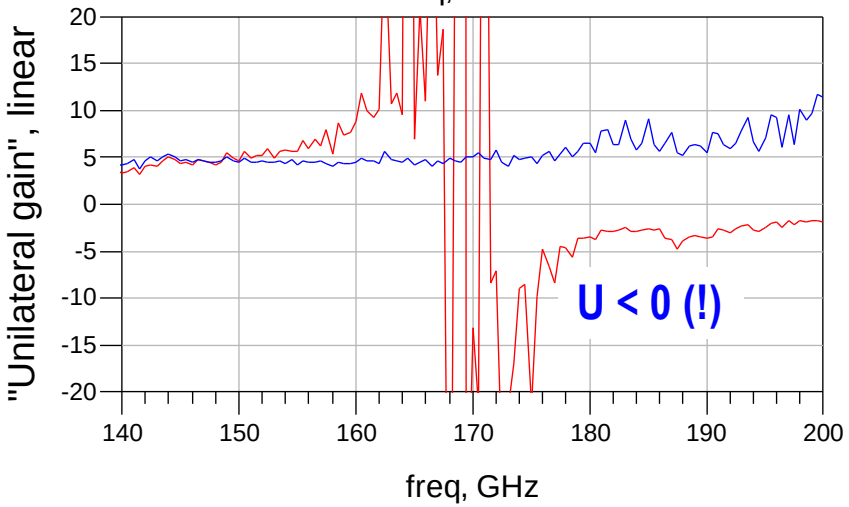




Difficulties with 140-220GHz TRL Calibration

Data on two layouts of 65 nm MOSFET



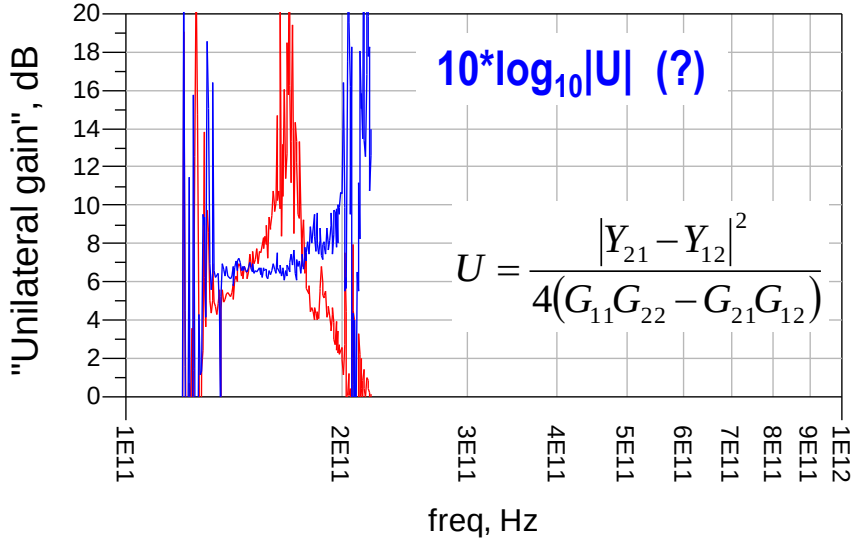


Measured Y-parameters correlate reasonably with expected device model.

Small errors in measured 2-port parameters result in large changes in Unilateral gain and Rollet's stability factor; neither measurement is credible.

Y_{12} appears to be the key problem.

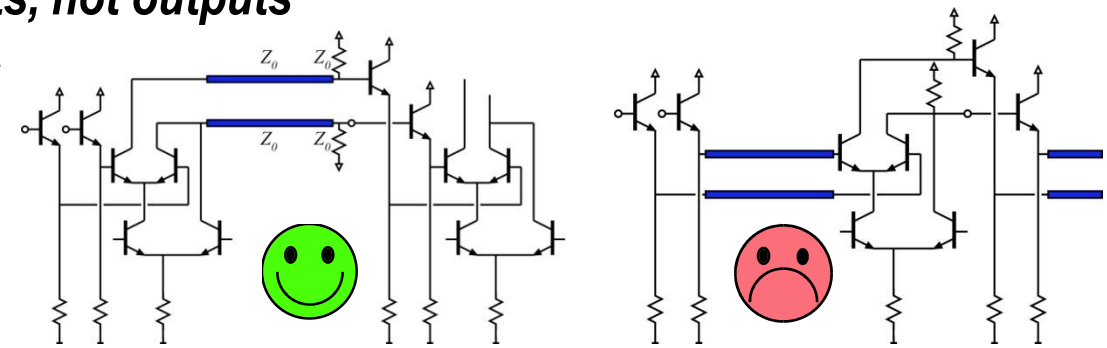
IC S_{ij} measurements are fine. Transistor f_{max} measurements are hard.



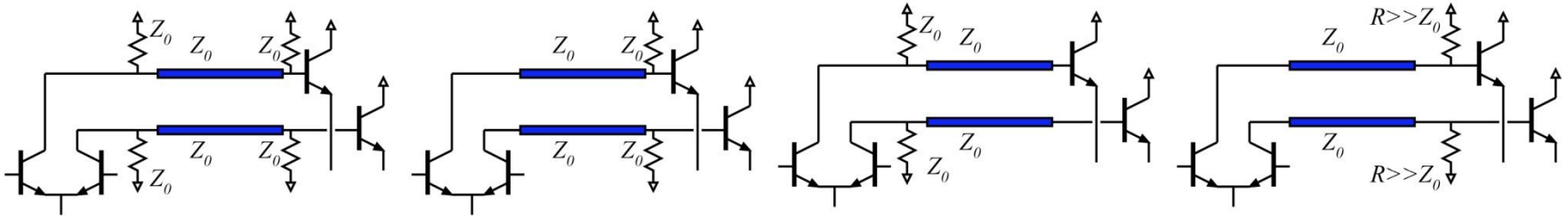
50+ GHz Mixed-Signal & ECL design: Principles & Examples

High Speed ECL Design

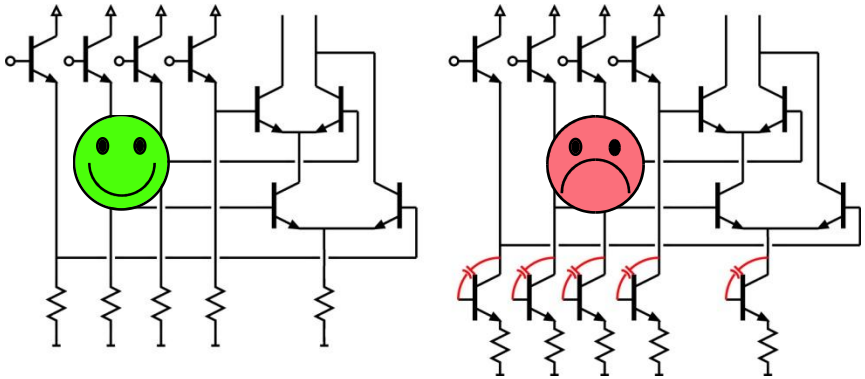
Followers associated with inputs, not outputs
Emitters never drive long wires.
(instability with capacitive load)



Double termination for least ringing, send or receive termination for moderate-length lines, high-Z loading saves power but kills speed.



Current mirror biasing is more compact.
Mirror capacitance→ ringing, instability.
Resistors provide follower damping.

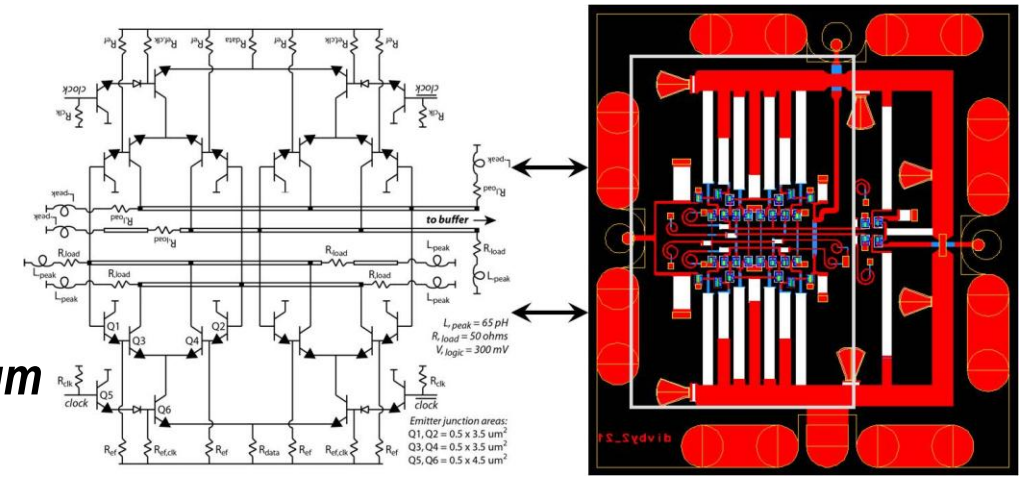


High Speed ECL Design

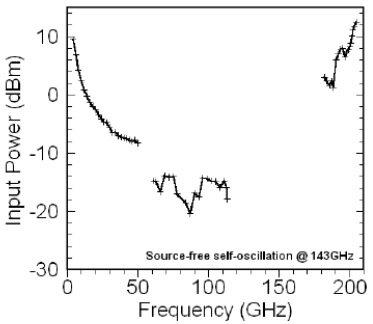
Layout: short signal paths at gate centers, bias sources surround core. Inverted thin film microstrip wiring.

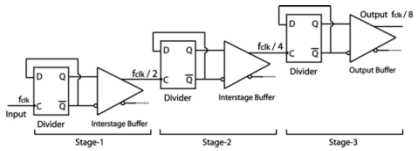
Key: transistors in on-state operate at Kirk limited-current. → minimizes C_{cb}/I_c delay.

Key: transistors designed for minimum ECL gate delay*, not peak (f_τ, f_{max}).
**hand expression, charge-control analysis*

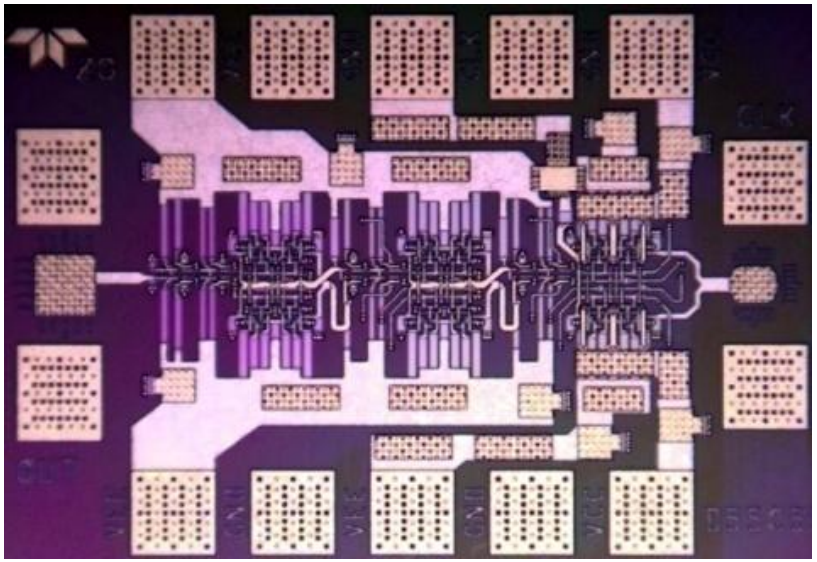


Example: 8:1 205 GHz static divider in 256 nm InP HBT.





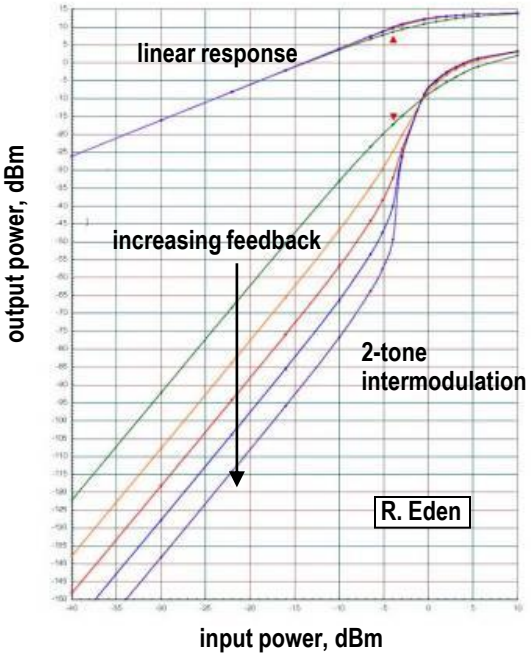
205 GHz divider, Griffith et al, IEEE CSIC, Oct. 2010

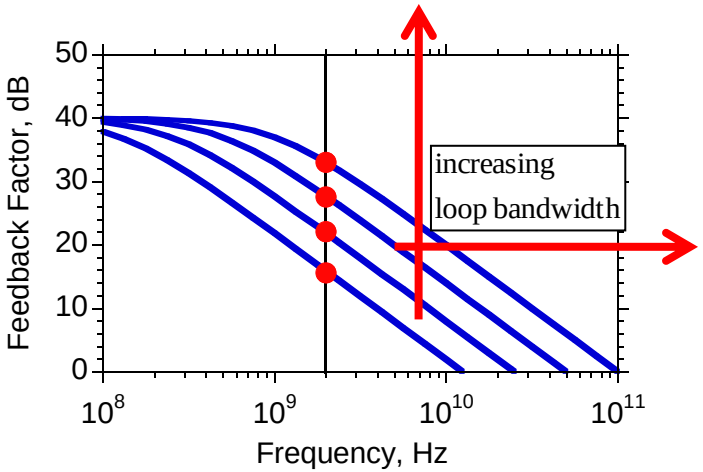


mm-wave Op-Amps for Linear Microwave Amplification

Griffith et al, IEEE IMS, June. 2011

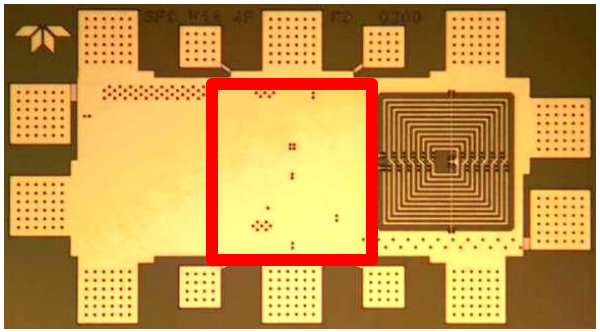
Reduce distortion with strong negative feedback

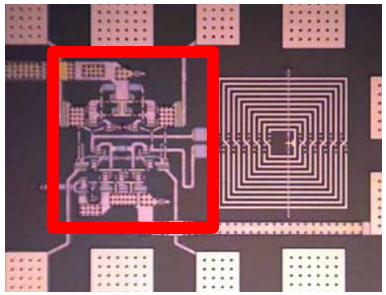




Even for 2 GHz operation, loop bandwidths must 20-40 GHz.

need very fast transistors

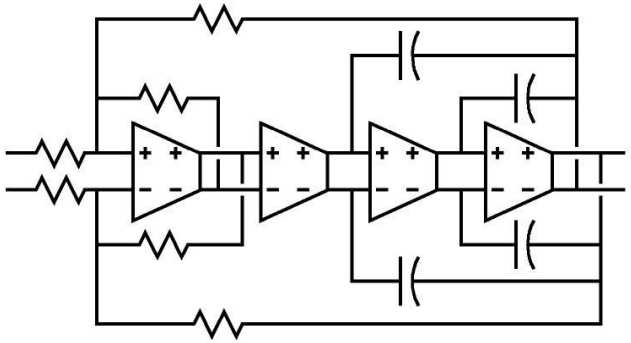




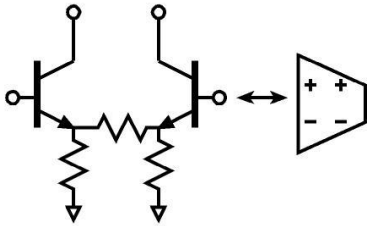
physically small feedback loop; bias components surround active core.

mm-wave Op-Amps for Linear Microwave Amplification

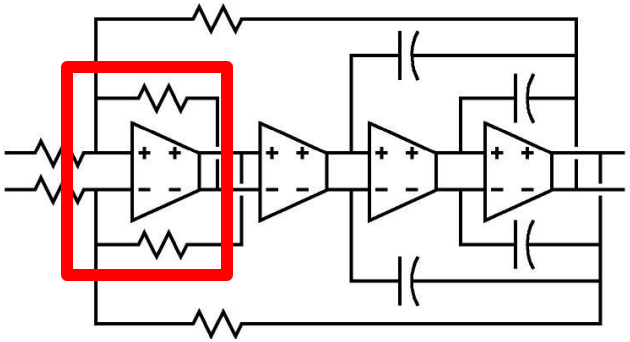
Griffith et al, IEEE IMS, June. 2011



current-mode analog design

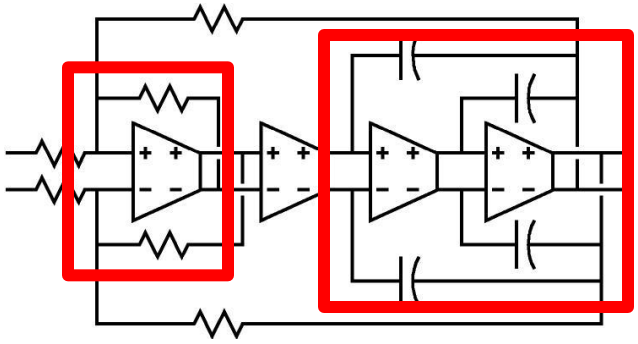


...node impedances kept low with transimpedance loading → high bandwidth



Virtual-ground input stage, Miller feedback around output stage, makes feedback insensitive to generator & load impedances.

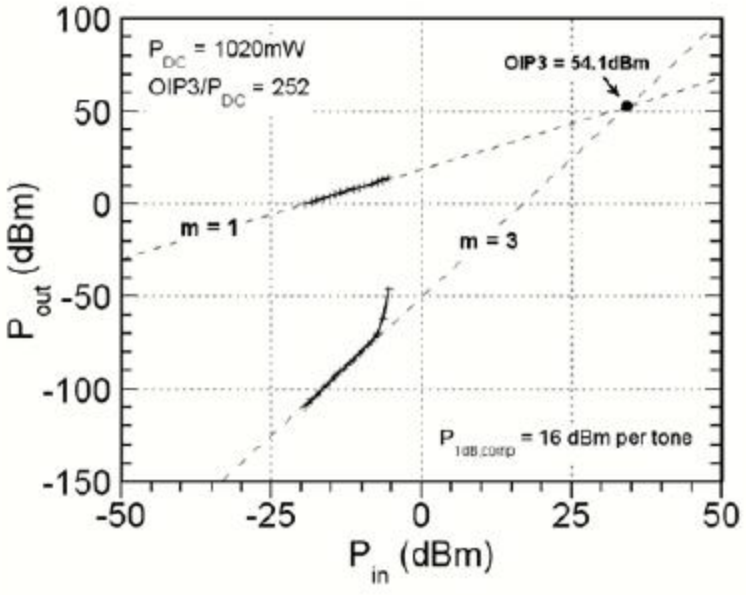
...critical for stability in a 50 GHz loop !
(what will the op-amp be connected to ?)

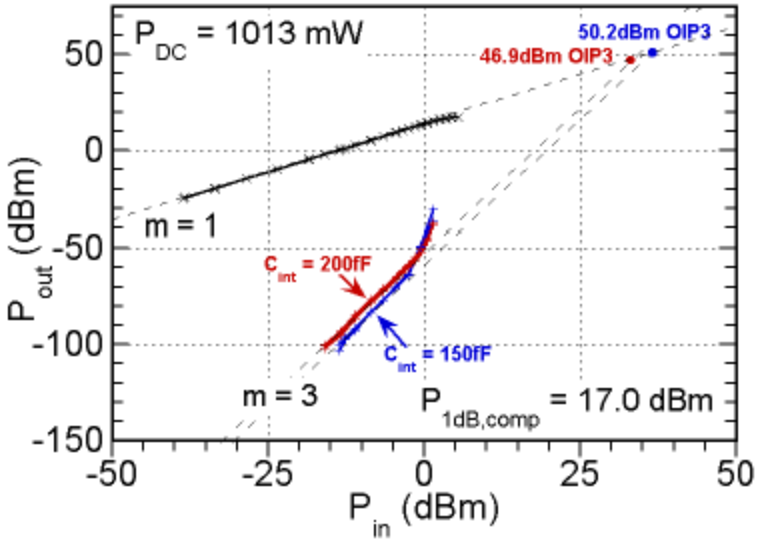


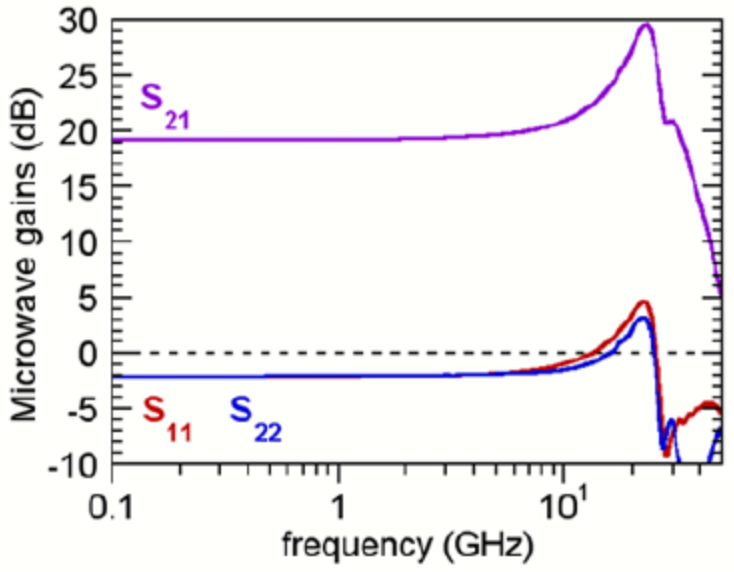
Z_t-stage and loop nesting for high gain even with fast resistor-loaded circuits

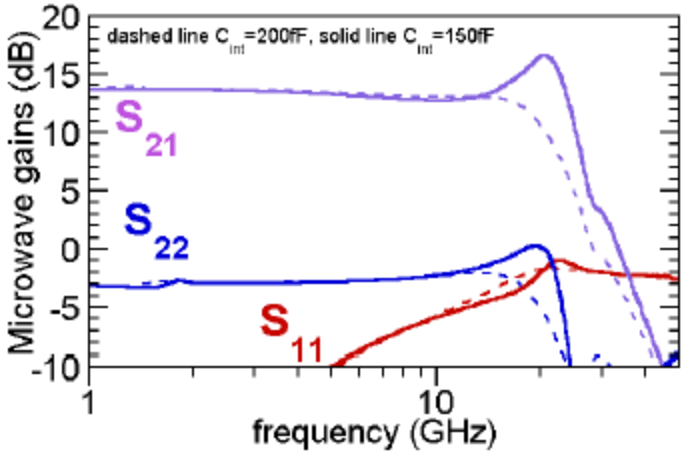
mm-wave Op-Amps for Linear Microwave Amplification

Griffith et al, IEEE IMS, June. 2011
Griffith et al, IEEE IPRM, May. 2008





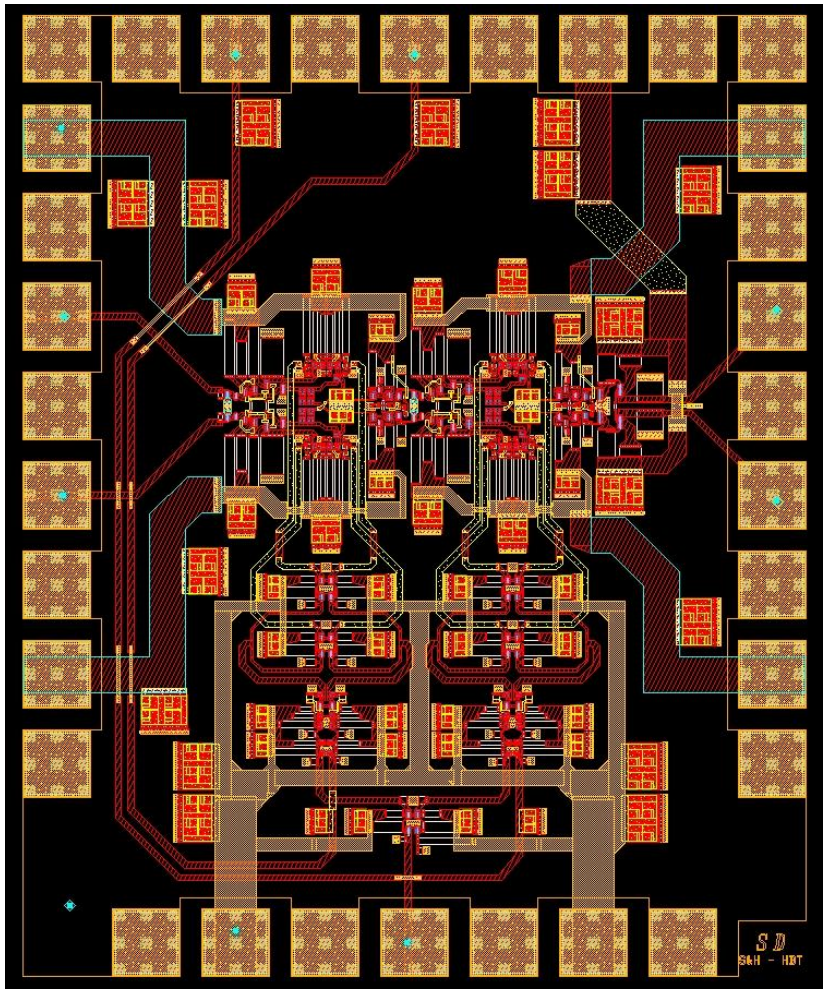


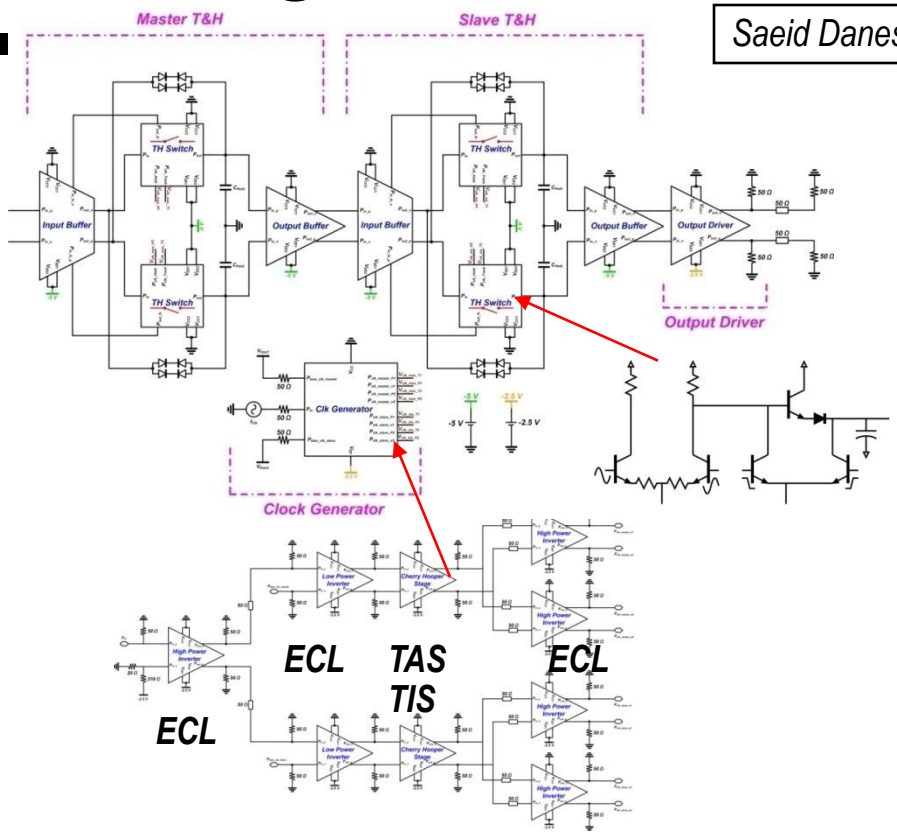


40 GSample/s Sample/Hold *Design*

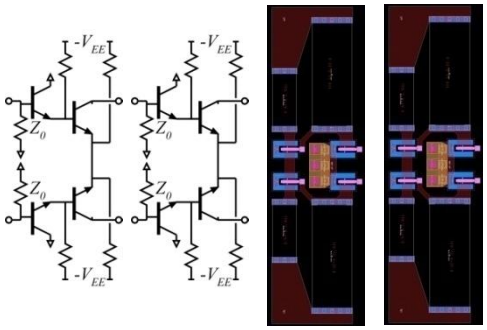
Saeid Daneshgar

master-slave track-hold
target 40 GS/s, 6 b (??)
256 nm InP HBT

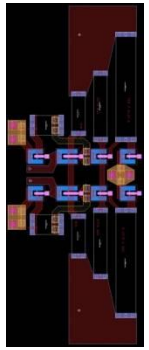




layout: ECL buffer.



layout: TASTIS.



Bias and transmission-line design strongly follows controlled-impedance ECL examples.

RF-IC design Principles & Examples

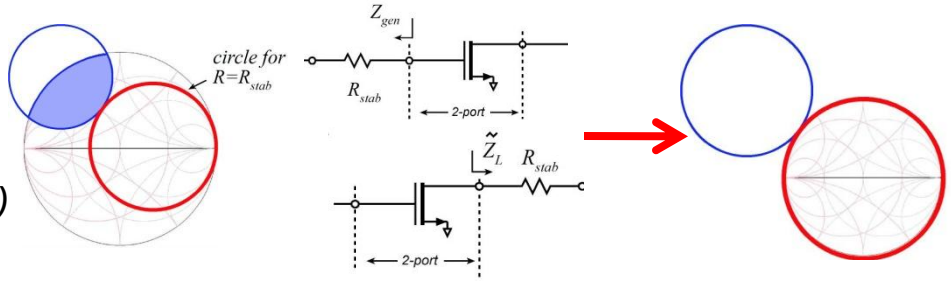
RF-IC Design: Simple & Well-Known Procedures

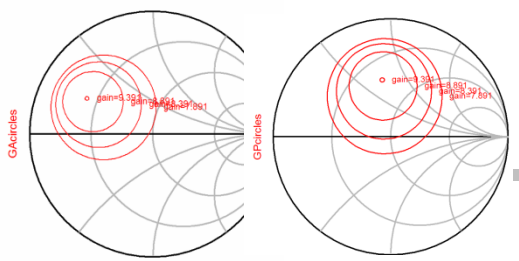
1: (over)stabilize at the design frequency
guided by stability circles

2: Tune input for F_{min} (LNAs) or output for P_{sat} (PAs)

3: Tune remaining port for maximum gain

4: Add out-of-band stabilization.

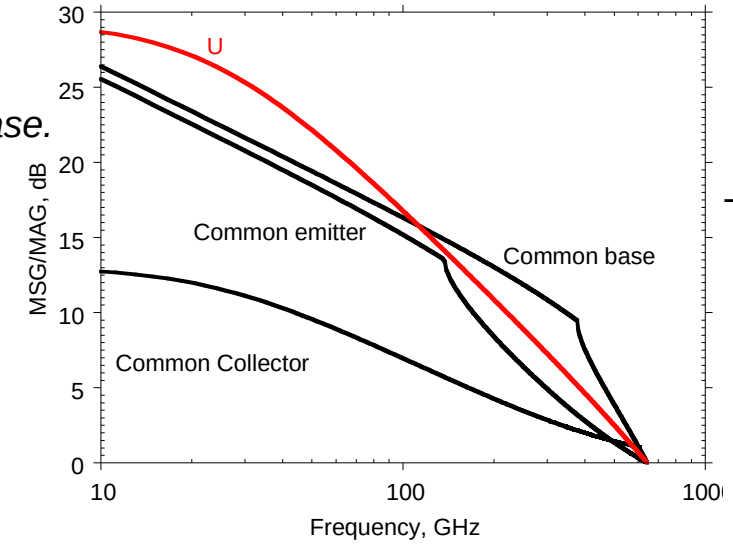


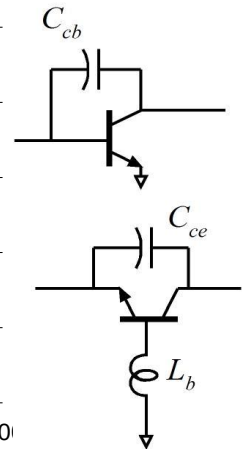


There are many ways to tune port impedances: microstrip lines, MIM capacitors, transformers
Choice guided by tuning losses. No particular preferences.

For BJT's, MAG/MSG usually highest for common-base.
→ preferred topology.

Common-base gain is however reduced by:
base (layout) inductance
emitter-collector layout capacitance.



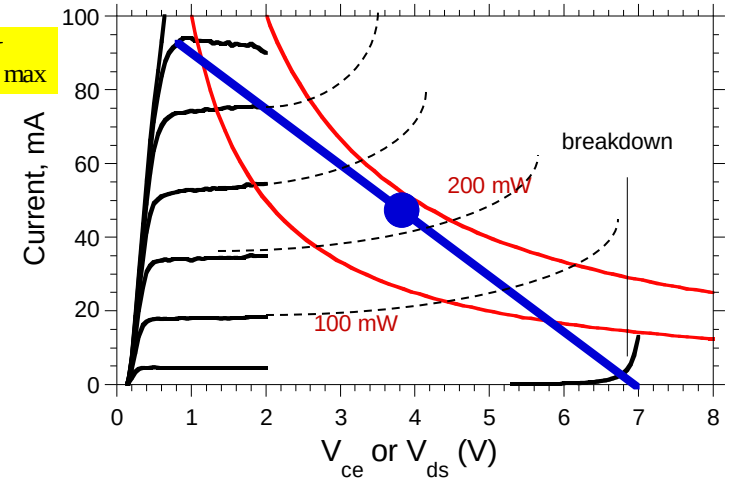


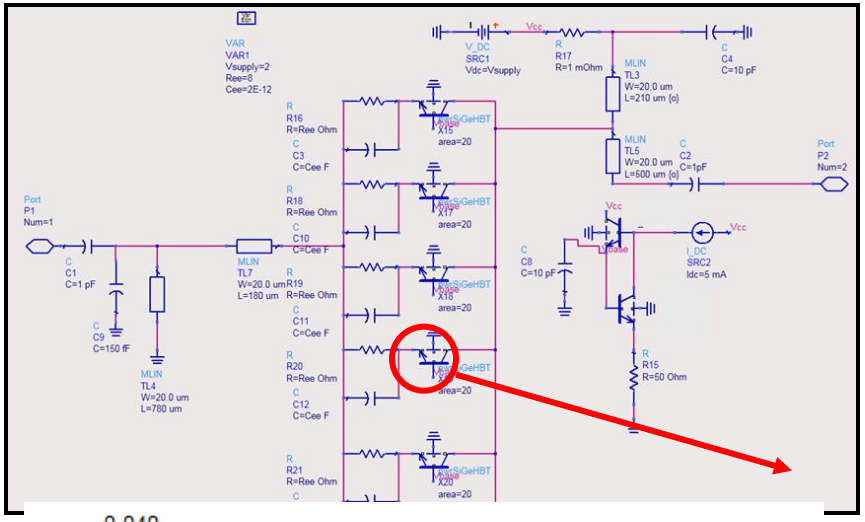
Power Amplifier Design (Cripps method)

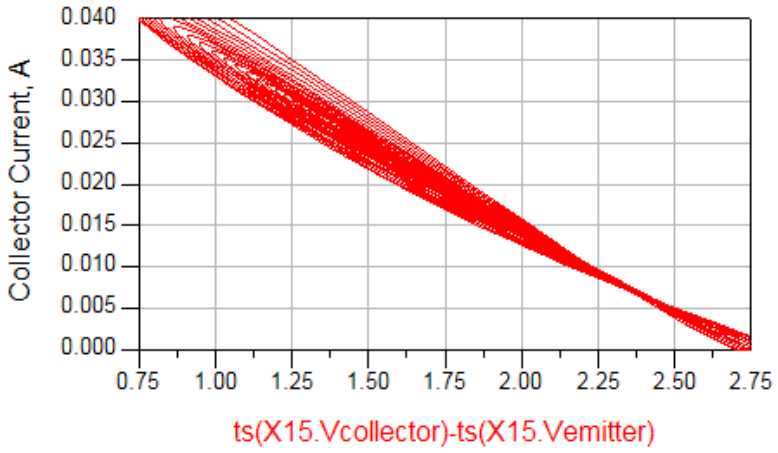
For maximum saturated output power, & maximum efficiency device intrinsic output must see optimum loadline set by:

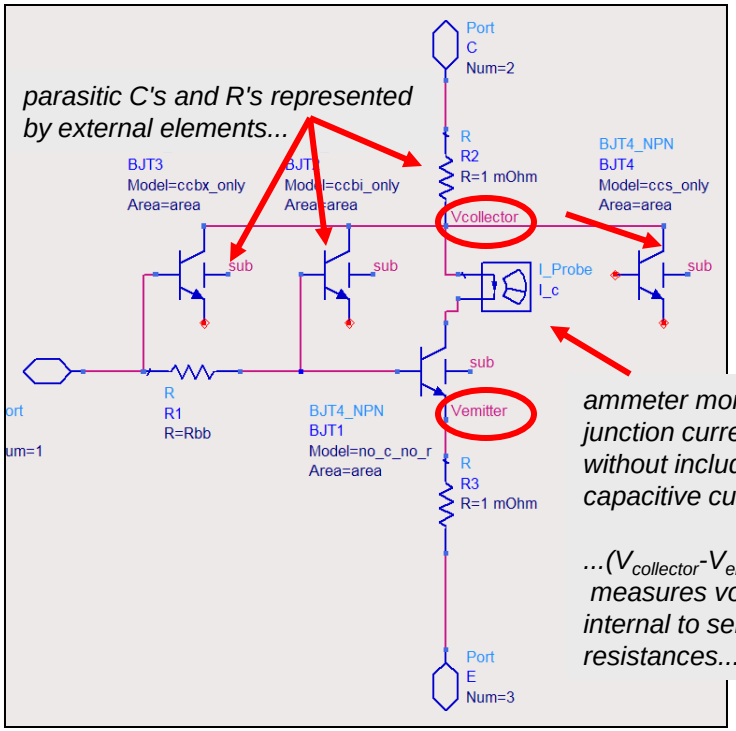
breakdown, maximum current, maximum power density.

$$P_{max} = (1/8)(V_{max} - V_{min})I_{max}$$









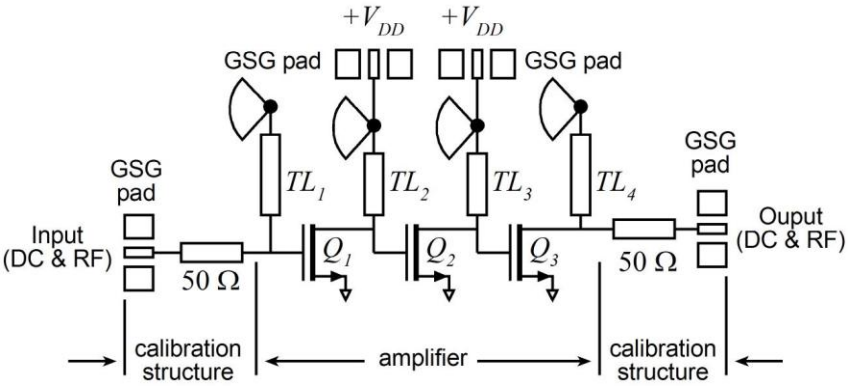
ammeter monitors intrinsic junction current without including capacitive currents

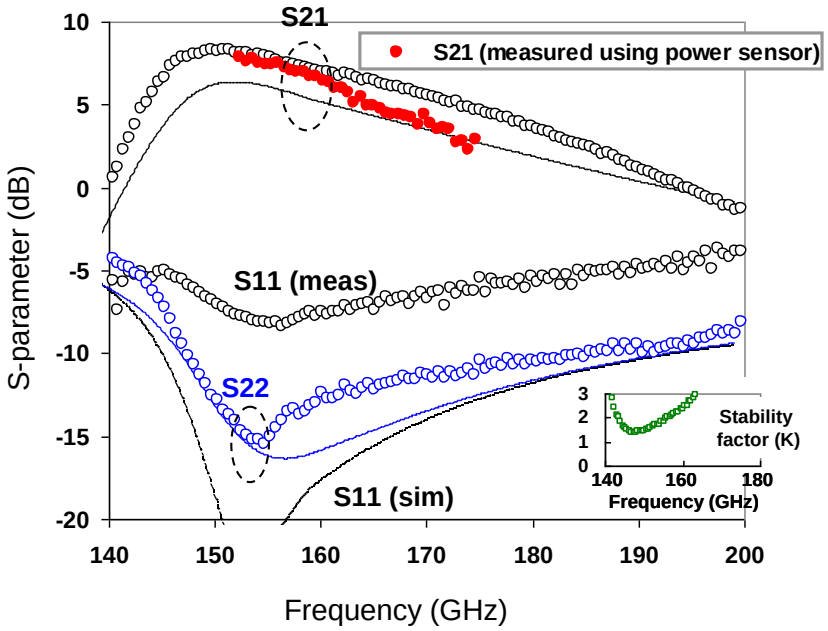
...($V_{collector}$-$V_{emitter}$) measures voltage internal to series parasitic resistances...

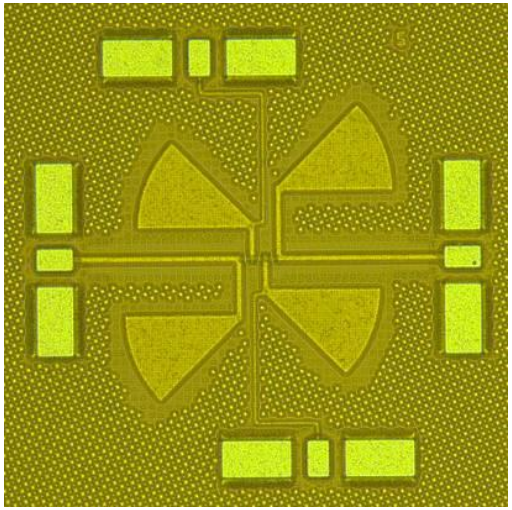
3-stage 150-GHz Amplifier; IBM 65 nm CMOS

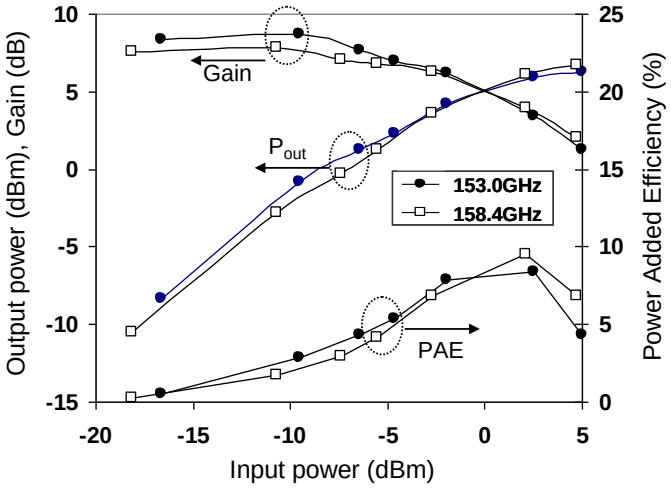
Acknowledgement:
IBM

M. Seo, B. Jagannathan, J. Pekarik, M. Rodwell, IEEE JSSCC, Dec. 2009

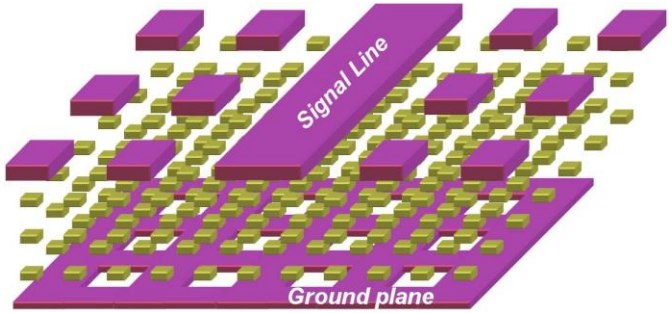








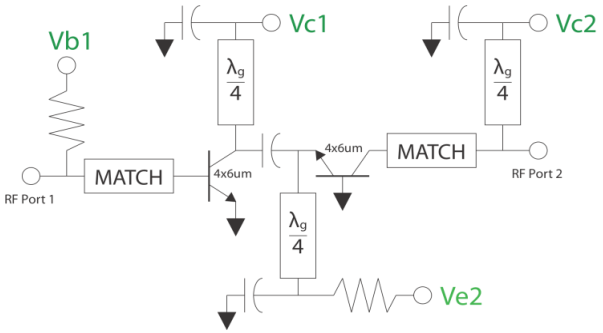
Dummy-prefilled microstrip lines



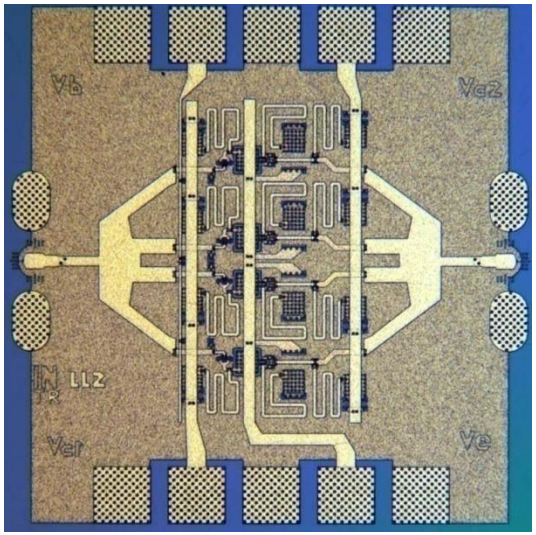
220 GHz, 48 mW HBT Power Amplifier

T. Reed et al, IEEE CSIC, Oct. 2011, to be presented.

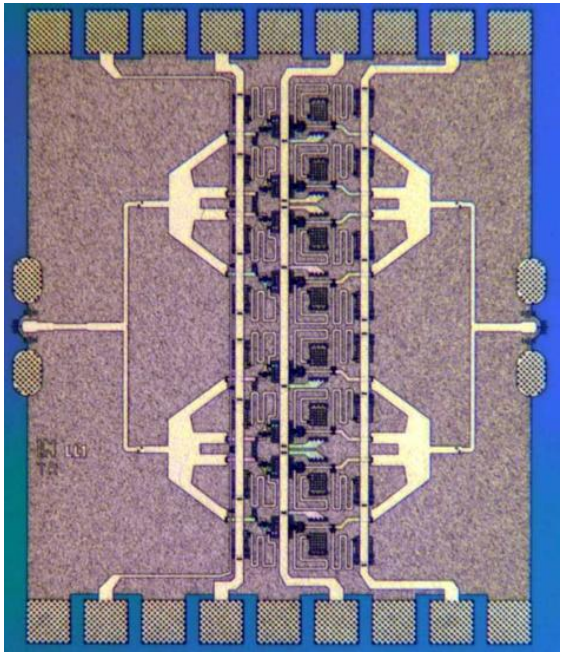
4-cell design: P_{sat} >48 mW @ 220 GHz



schematic of single cell



8-cell design: not yet fully tested: P_{sat} = ?



Technology:

- ***Teledyne 250 nm InP HBT***
- ***Right-side-up thin-film microstrip wiring.***
- ***Breaks in ground plane minimized.***

High Frequency Bipolar IC Design

Digital, mixed-signal, RF-IC (tuned) IC designs----at very high frequencies

Even at 670 GHz, design procedures differ little from that at lower frequencies: classic IC design extends readily to the far-infrared.

Key considerations: Tuned ("RF") ICs

Rigorous E&M modeling of all interconnects & passive elements
Continuous ground plane → required for predicable interconnect models.
Higher frequencies→ close conductor planes→ higher loss, lower current

Key considerations: digital & mixed-signal :

Transmission-line modeling of all interconnects
Continuous ground plane → required for predicable interconnect models.
Unterminated lines within blocks; terminated lines interconnecting blocks.
Analog & digital blocks design to naturally interface to 50 or 75Ω.

Next: TMIC designs for 340 GHz, 670 GHz transceivers.