InGaAs/InP DHBTs demonstrating simultaneous f_t/f_{max} ~ 460/850 GHz in a refractory emitter process

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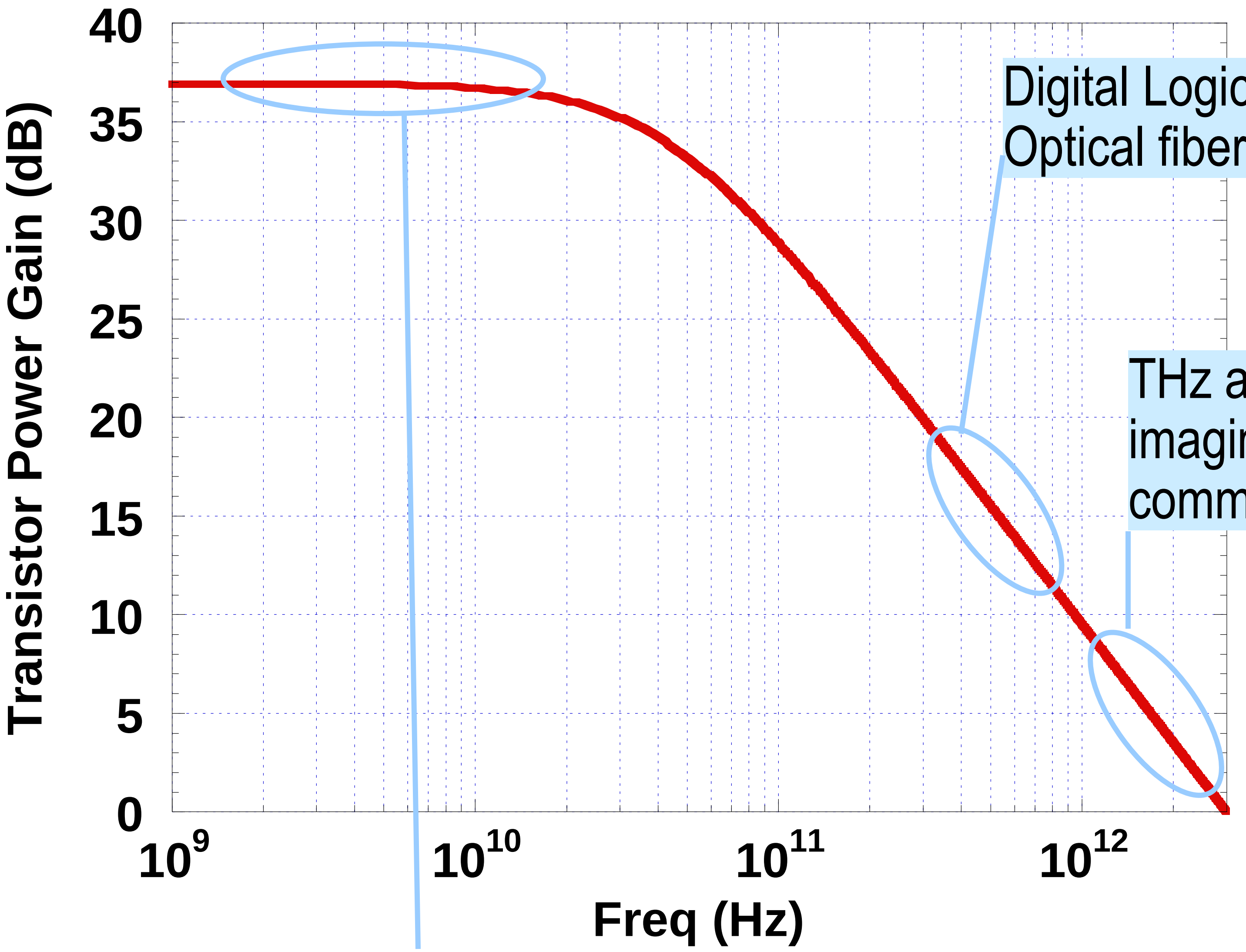
Outline

- Need for high speed HBTs
- HBT Scaling Laws
- Fabrication
  - Challenges
  - Process Development
- DHBT
  - Epitaxial Design
  - Results
- Summary

Why THz Transistors?



Digital Logic for
Optical fiber circuits

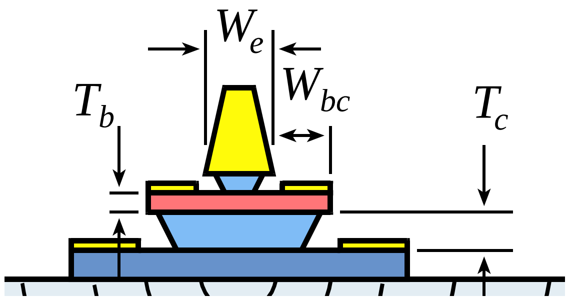
THz amplifiers for
imaging, sensing,
communications

High gain at microwave frequencies → precision analog design, high resolution ADC & DAC, high performance receivers

Bipolar transistor scaling laws

$$\frac{1}{2\pi f_\tau} = \tau_{tr} + RC$$

$$f_{\max} = \sqrt{\frac{f_\tau}{8\pi R_{bb,eff} C_{cb,eff}}}$$



(emitter length L_e)

To ***double cutoff frequencies*** of a mesa HBT, must:

Keep ***constant*** all ***resistances*** and ***currents***
Reduce all ***capacitances*** and ***transit delays by 2***

$$\tau_b \approx T_b^2 / 2D_n + T_b / v_{exit}$$
$$\tau_c = T_c / 2v_{sat}$$

Epitaxial scaling

$$C_{cb} = \varepsilon A_c / T_c$$
$$I_{c,\max} \propto v_{eff} A_e (V_{\mathrm{cb}} + \phi_{bi}) / T_c^2$$

Lateral scaling

$$R_{ex} = \rho_{\mathrm{contact}} / A_e$$
$$R_{bb} = \rho_{\mathrm{sheet}} \left(\frac{W_e}{12 L_e} + \frac{W_{bc}}{6 L_e} \right) + \frac{\rho_{\mathrm{contact}}}{A_{\mathrm{contacts}}}$$

Ohmic contacts

Base Access Resistance

$$\boxed{f_{\max} = \sqrt{\frac{f_\tau}{8\pi R_{bb} C_{cb}}}}$$

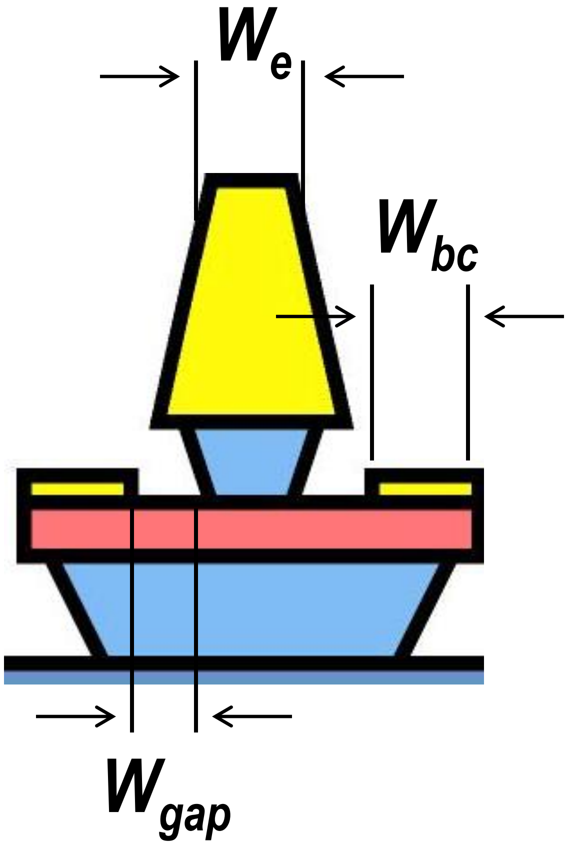
$$R_{bb} = \rho_{\mathrm{sh,e}} \cdot \frac{W_e}{12 L_e} + \rho_{\mathrm{sh,bc}} \cdot \frac{W_{bc}}{6 L_e} + \rho_{\mathrm{sh,gap}} \cdot \frac{W_{gap}}{2 L_e} + \frac{\rho_{\mathrm{contact}}}{A_{\mathrm{contacts}}}$$

$$\rho_{\mathrm{sh,gap}} >> \rho_{\mathrm{sh,e}}, \rho_{\mathrm{sh,bc}}$$

- Surface Depletion
- Process Damage

→ Need for very small W_{gap}

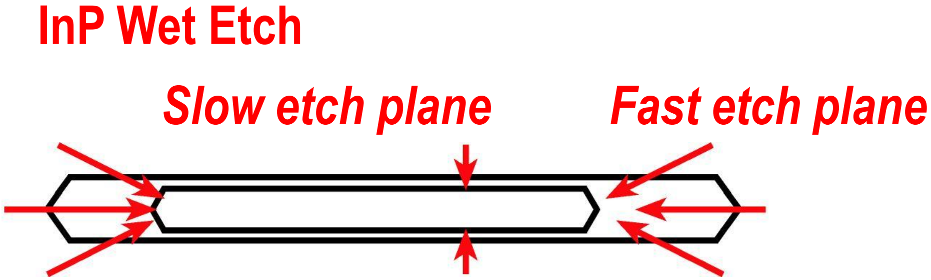
- Small undercut in InP emitter
- Self-aligned base contact

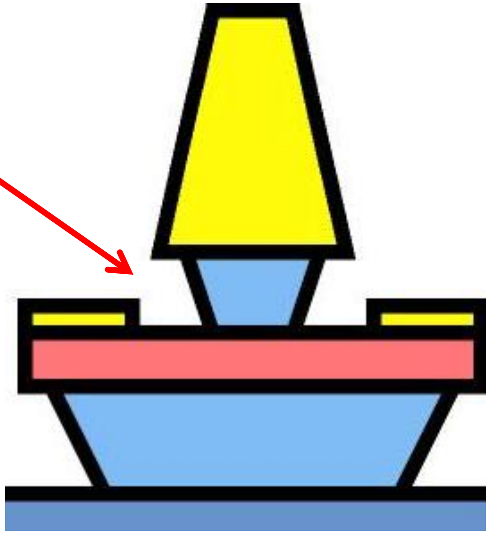


Base-Emitter Short

Undercut in thick emitter semiconductor

Helps in Self Aligned Base Liftoff





For controlled semiconductor undercut

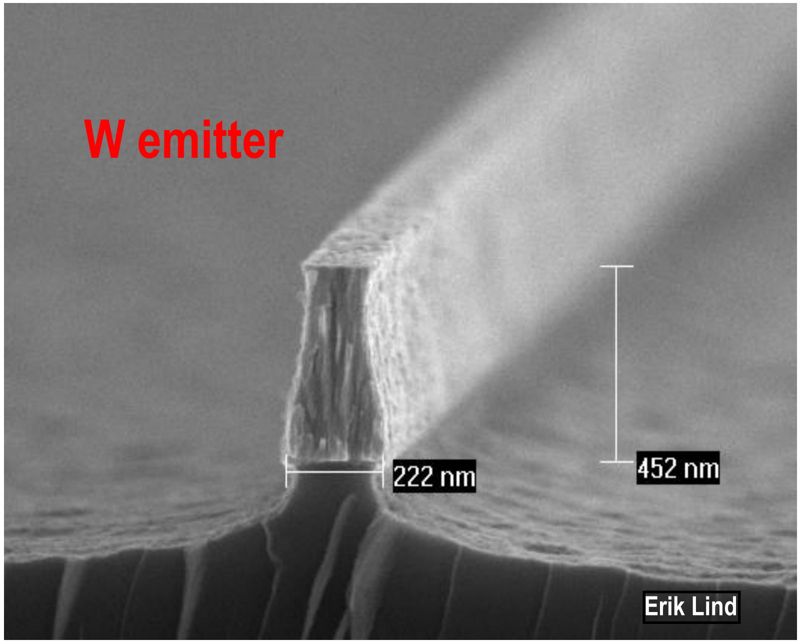
→ Thin semiconductor

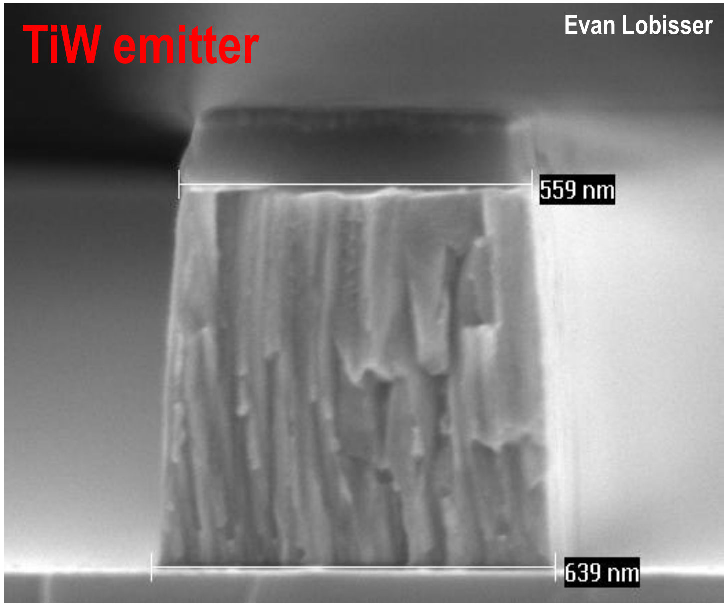
To prevent base – emitter short

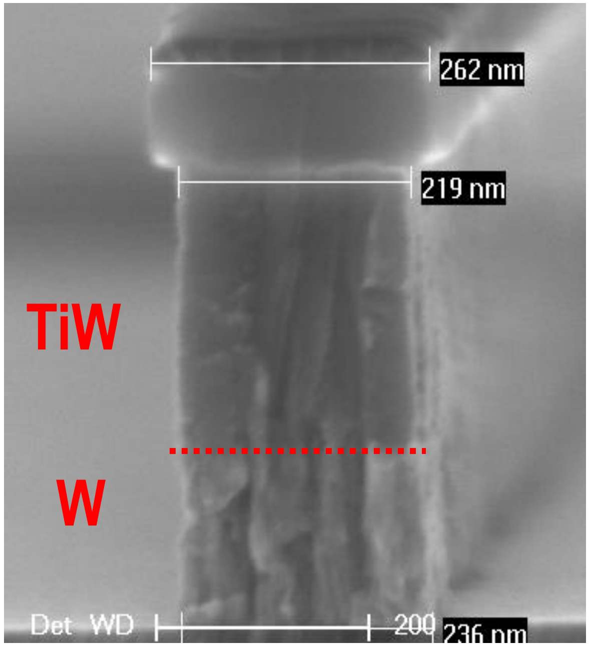
→ Vertical emitter profile and line of sight metal deposition

→ Shadowing effect due to high emitter aspect ratio

Composite Emitter Metal Stack



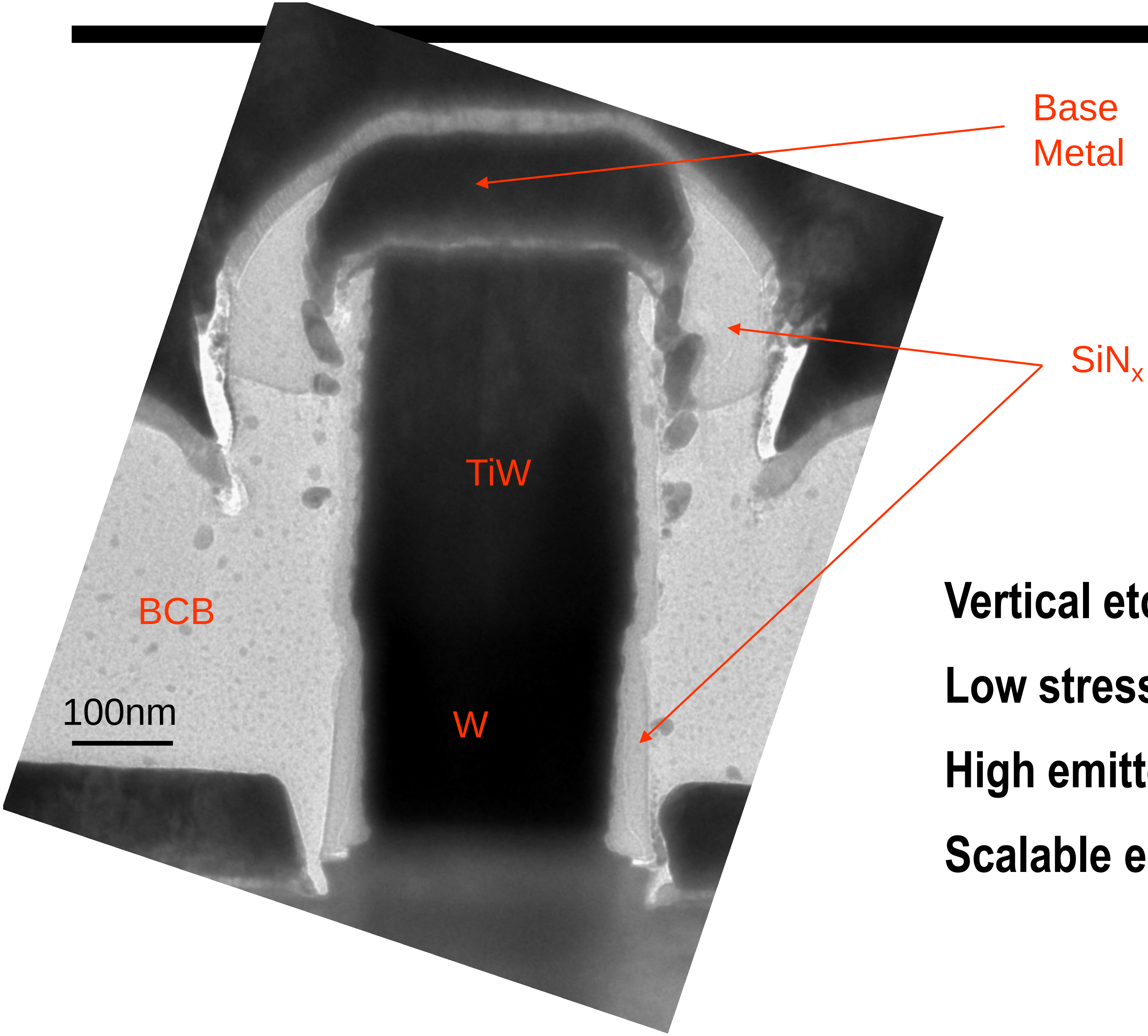




- W/TiW metal stack
- Low stress
- Refractory metal emitters
- Vertical dry etch profile

Vertical Emitter

FIB/TEM by E Lobisser



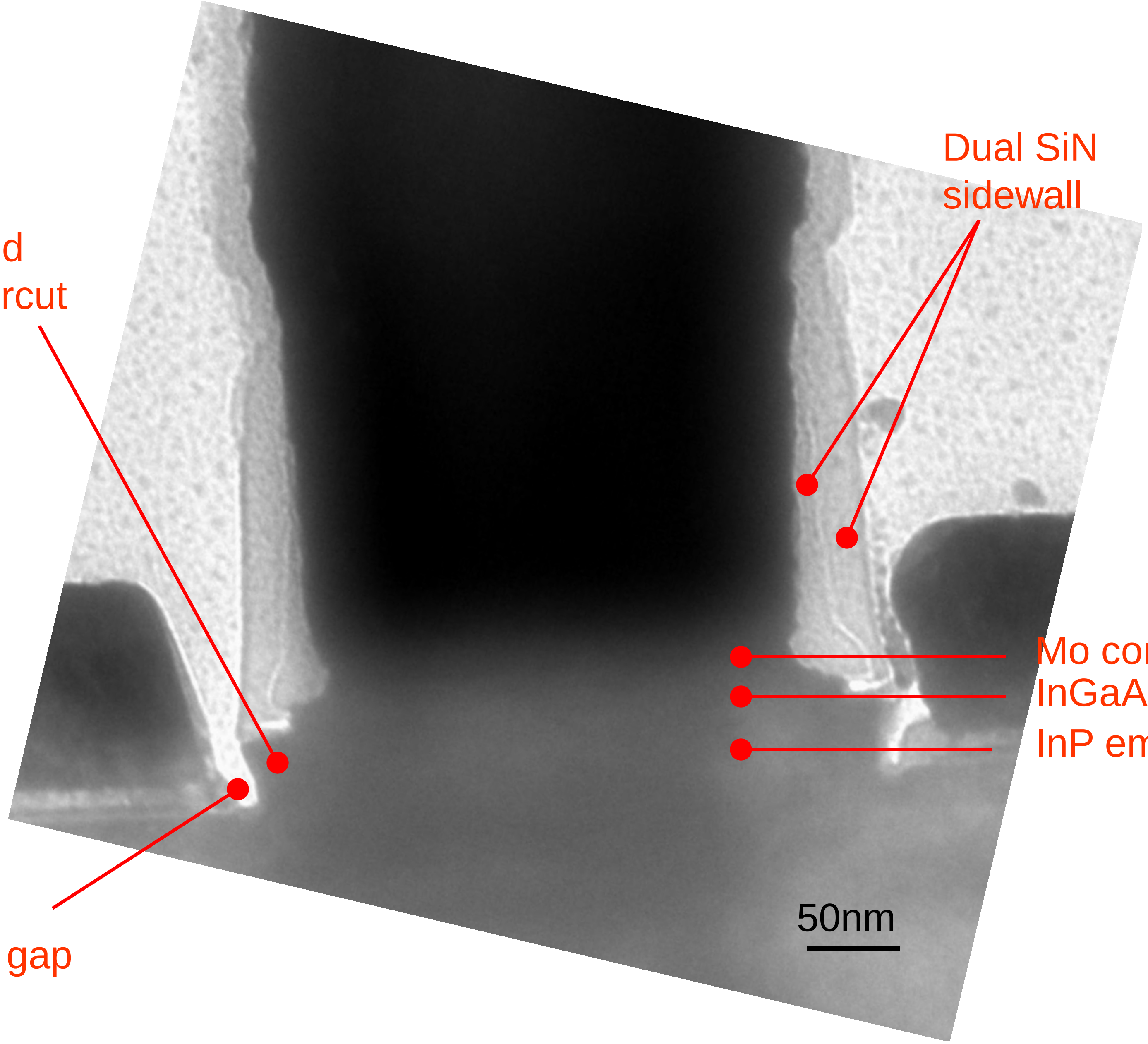
Vertical etch profile

Low stress

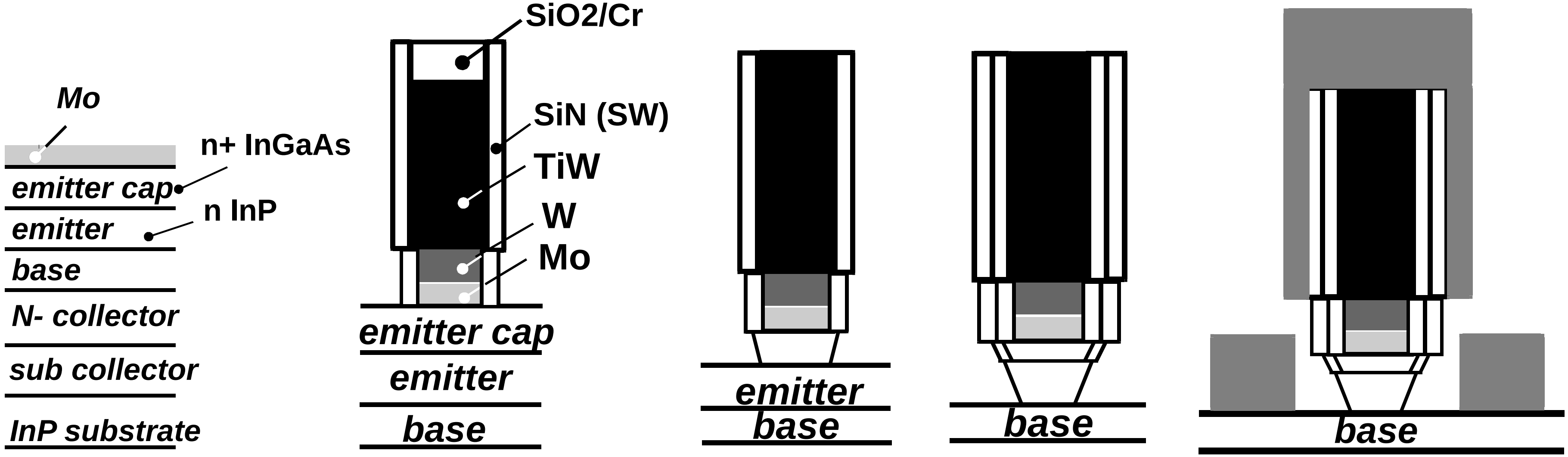
High emitter yield

Scalable emitter process

Narrow Emitter Undercut



Process flow



Mo contact to n-InGaAs for emitter

W/TiW/SiO$_2$/Cr dep

SF$_6$/Ar etch

SiN$_x$ Sidewall

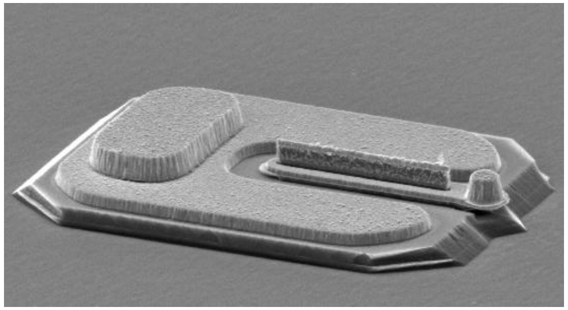
SiO$_2$/Cr removal

InGaAs Wet Etch

Second SiN$_x$ Sidewall

InP Wet Etch

Base Contact Lift-off



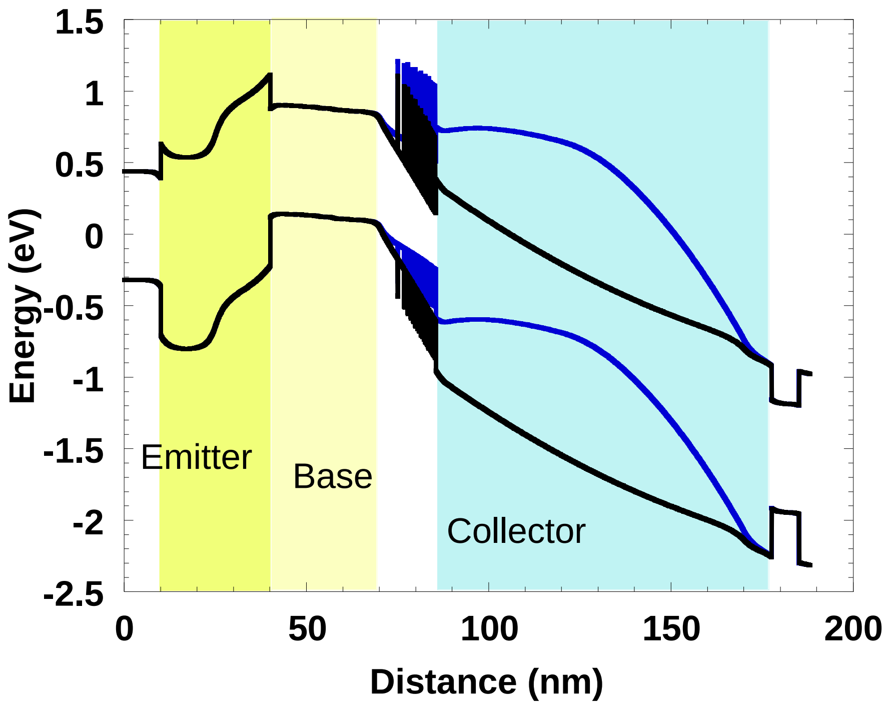
Base and ***collector*** formed via ***lift off*** and ***wet etch***

BCB used to passivate and planarize devices

Self-aligned process flow for DHBTs

Epitaxial Design

T(nm)	Material	Doping (cm^{-3})	Description
10	$In_{0.53}Ga_{0.47}As$	$8\cdot10^{19}$: Si	Emitter Cap
20	InP	$5\cdot10^{19}$: Si	Emitter
15	InP	$2\cdot10^{18}$: Si	Emitter
30	InGaAs	$9\text{-}5\cdot10^{19}$: C	Base
13.5	$In_{0.53}Ga_{0.47}As$	$5\cdot10^{16}$: Si	Setback
16.5	InGaAs / InAlAs	$5\cdot10^{16}$: Si	B-C Grade
3	InP	$3.6\cdot10^{18}$: Si	Pulse doping
67	InP	$5\cdot10^{16}$: Si	Collector
7.5	InP	$1\cdot10^{19}$: Si	Sub Collector
5	$In_{0.53}Ga_{0.47}As$	$4\cdot10^{19}$: Si	Sub Collector
300	InP	$2\cdot10^{19}$: Si	Sub Collector
Substrate	SI : InP		



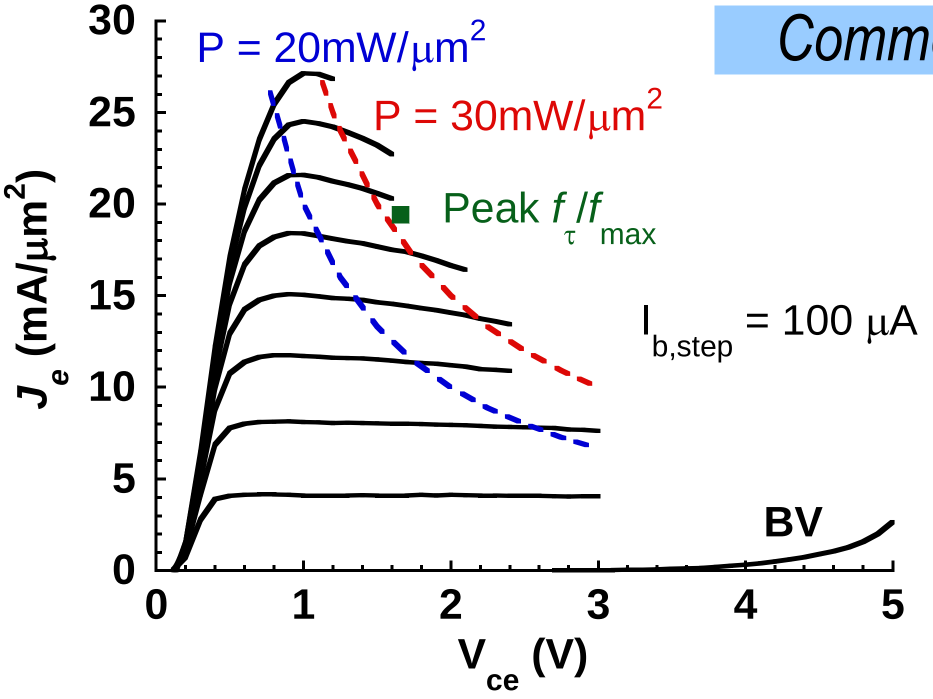
$V_{be} = 1\ V,\ V_{cb} = 0.7\ V,\ J_e = 24\ mA/\mu m^2$

Thin emitter semiconductor

→ Enables wet etching

Results - DC Measurements

Common emitter I-V



@Peak f_τ,f_{max}

J_e = 19.4 mA/µm^2

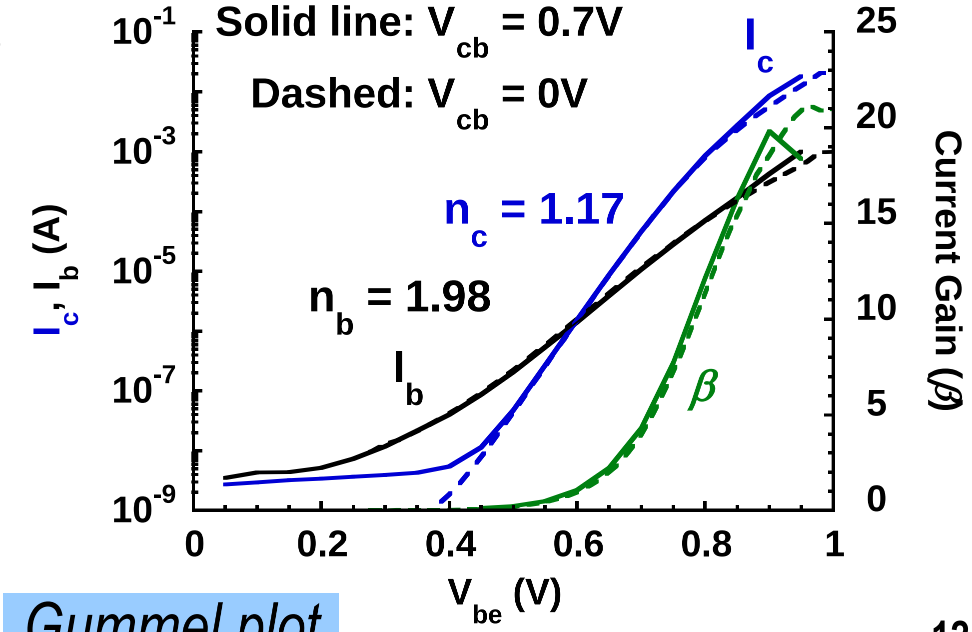
P = 32 mW/µm^2

BV_{ceo} = ***3.7 V*** @ J_e = 10 kA/cm^2

β = ***20***

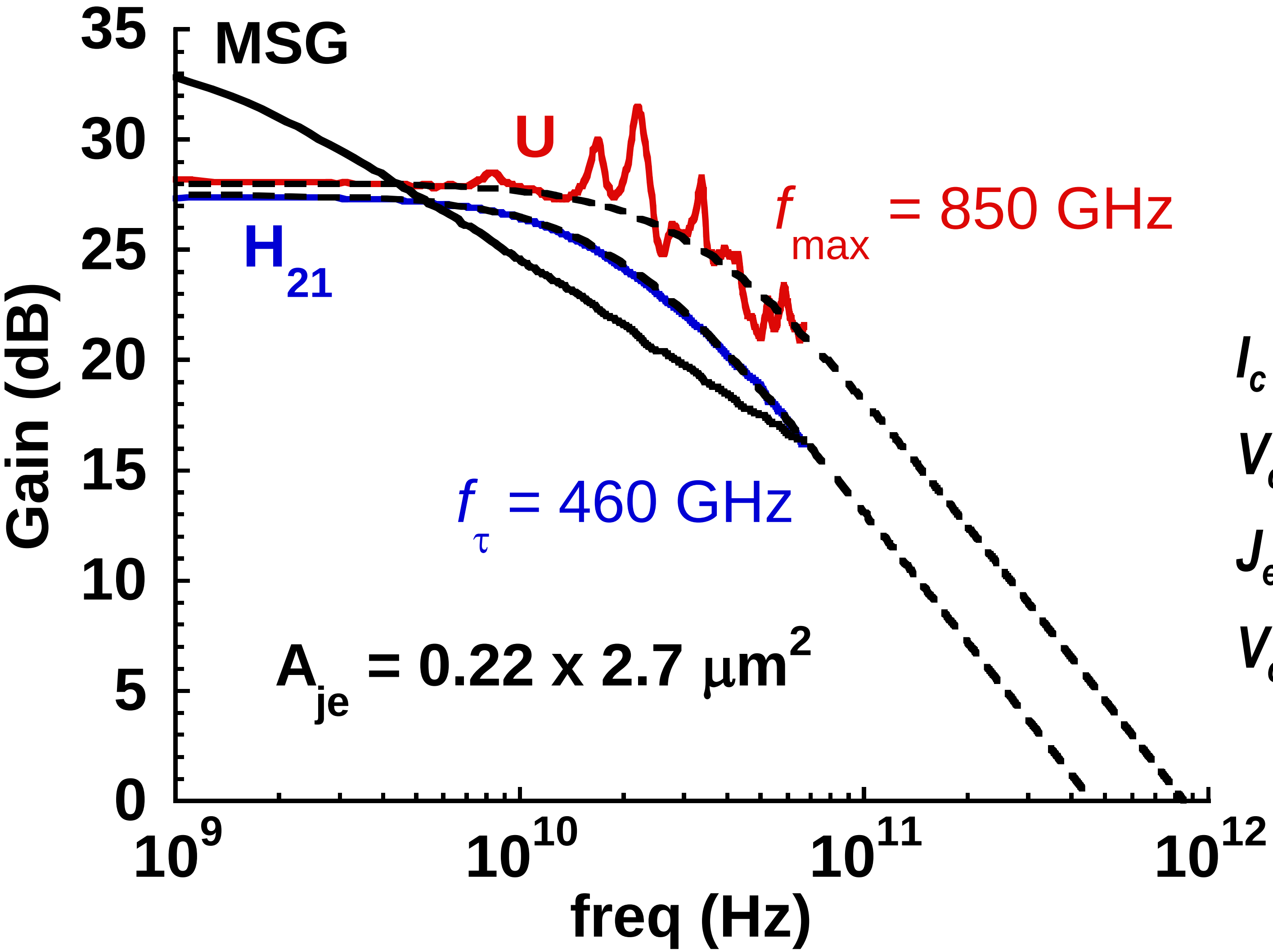
Base ρ_{sh} = ***710 Ω/sq***, ρ_c < ***5 Ω·µm***^{2}

Collector ρ_{sh} = ***15 Ω/sq***, ρ_c = ***22 Ω·µm***^{2}



Gummel plot

1-67 GHz RF Data



I_c = 11.5 mA

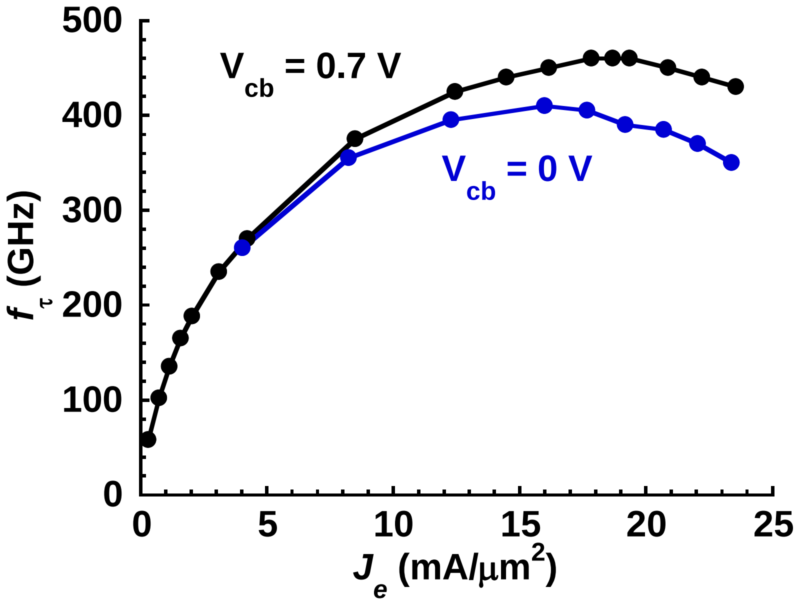
V_{ce} = 1.66 V

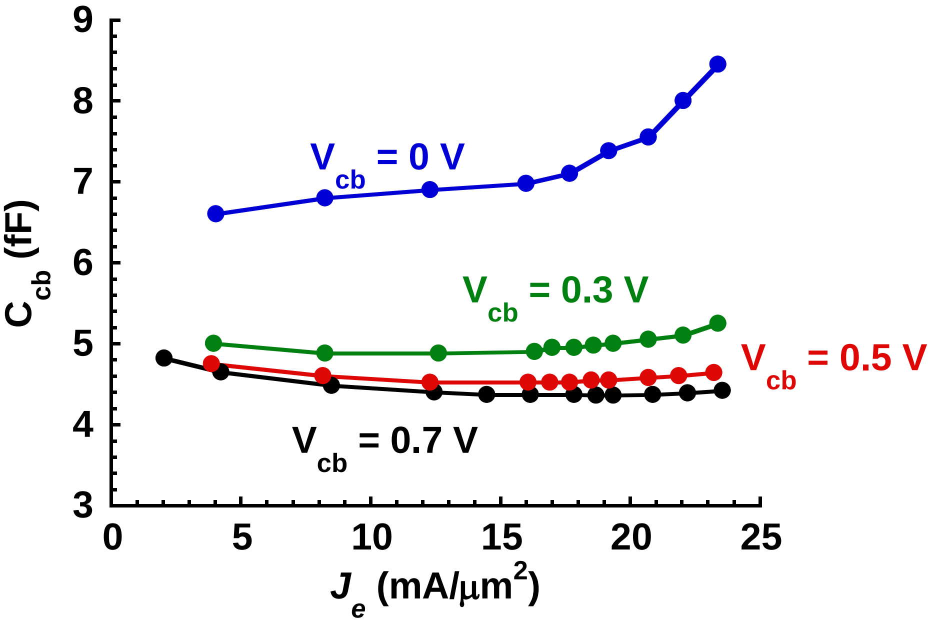
J_e = 19.4 mA/μm^2

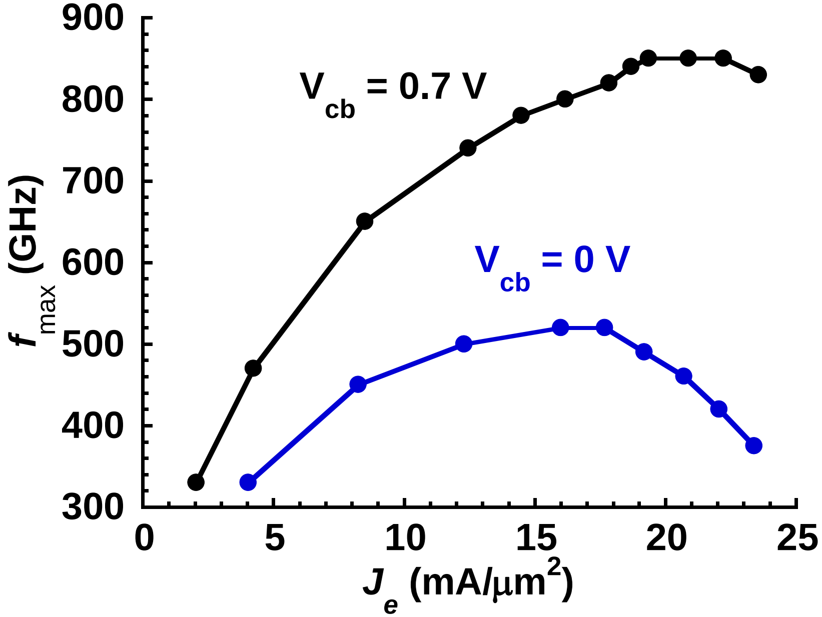
V_{cb} = 0.7 V

Single-pole fit to obtain cut-off frequencies

Parameter Extraction



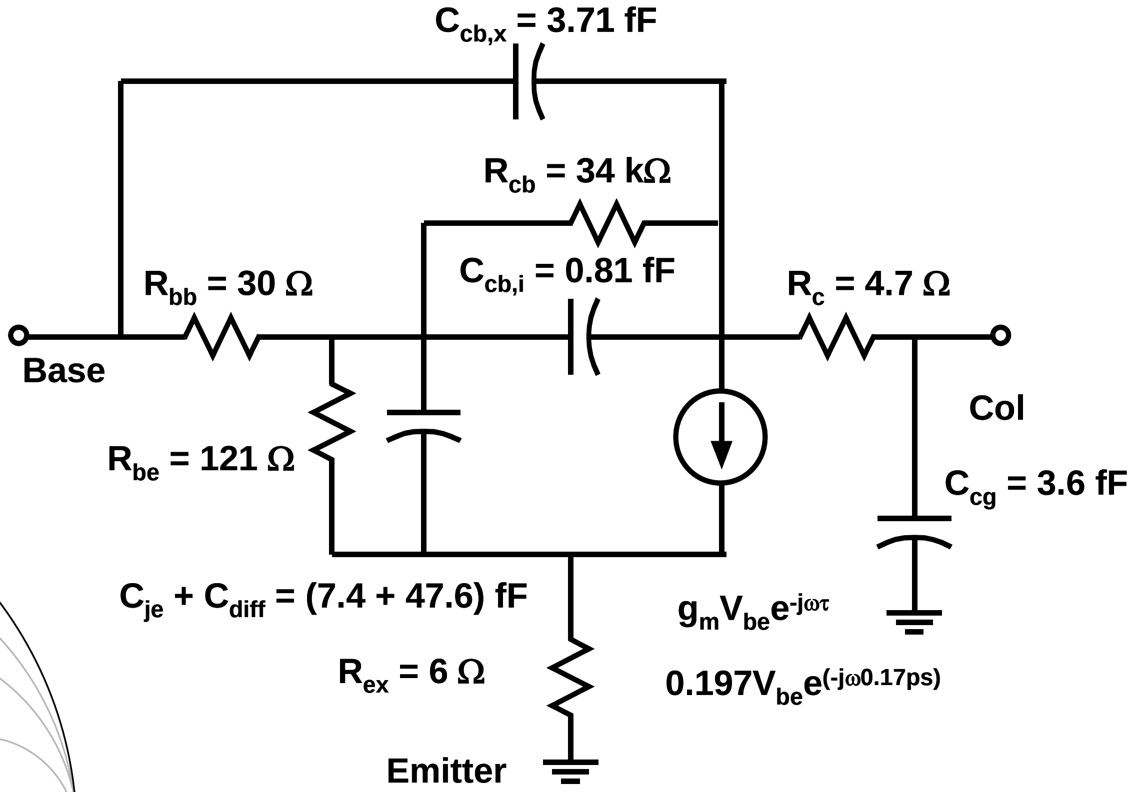


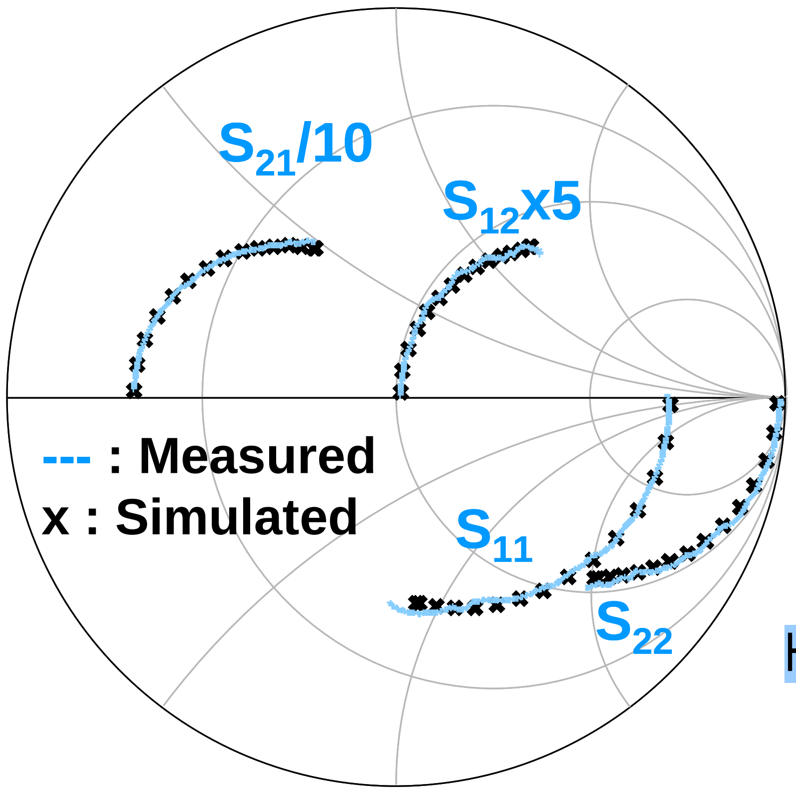


J_{kirk} = 23 mA/μm^2 (@V_{cb} = 0.7V)

Equivalent Circuit

$R_{ex} < 4\ \Omega\cdot\mu m^2$





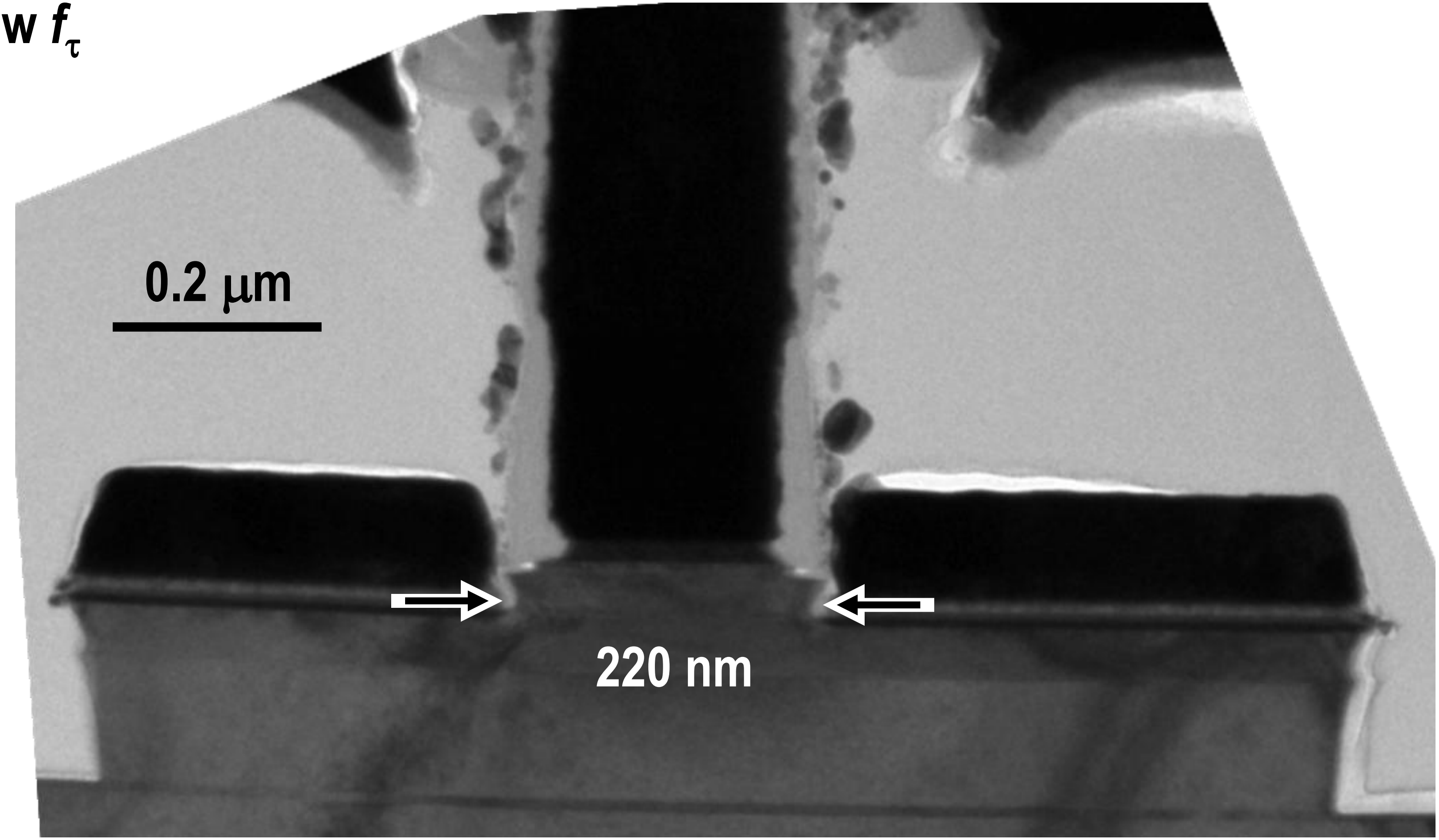
Hybrid-π equivalent circuit from measured RF data

TEM – Wide base mesa

High A_c / A_e ratio (>5)

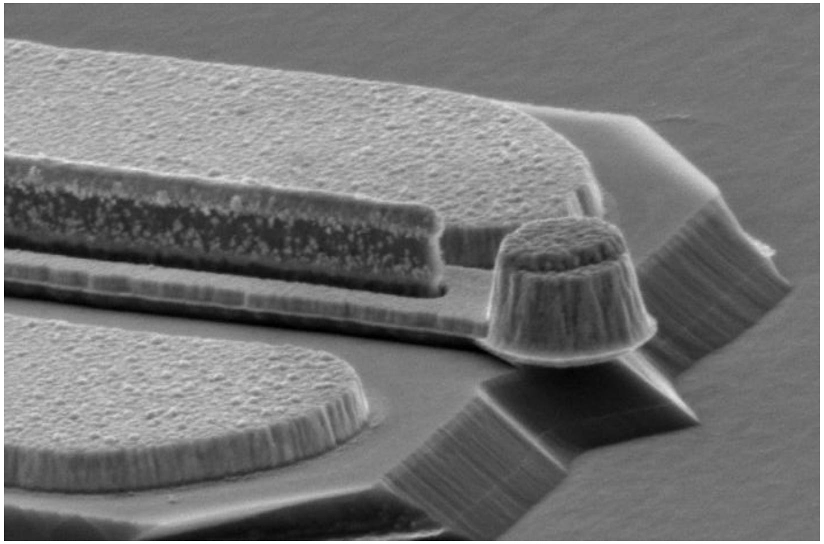
High $R_{ex} . C_{cb}$ delay

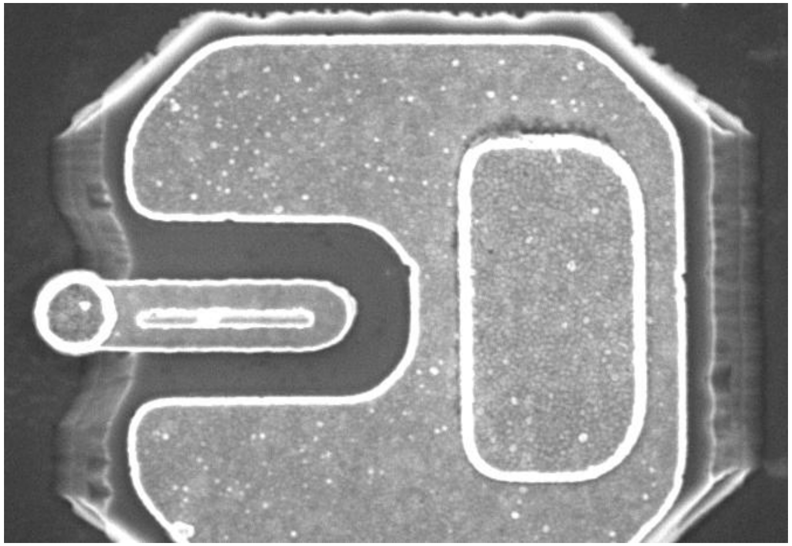
Low f_τ



Summary

- **Demonstrated DHBTs with peak f_τ / f_{max} = 460/850 GHz**
- **Small W_{gap} for reduced base access resistance → High f_{max}**
- **Narrow sidewalls, smaller base mesa and better base ohmics** needed to enable higher bandwidth devices





Thank You

Questions?

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