InP HBTs for THz Frequency Integrated Circuits

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Abstract

A 0.25µm InP DHBT process has been developed for THz frequency integrated circuits. A 0.25x4µm^2 HBT exhibits an extrapolated f_t/f_{max} of 430GHz/1.03THz at I_C =11mA, V_{CE}= 1.8V. The transistors achieve this performance while maintaining a common-emitter breakdown voltage (BV_{CEO}) >4V. Thin-film interconnects and backside wafer processes have been developed to support selected IC demonstrations. The technology has been used to build fundamental oscillators, amplifiers and dynamic frequency dividers all operating at >300GHz. Additionally, increasingly complex circuits such as a full PLL have been demonstrated.

1 Introduction

Transistor-based monolithic integrated circuits are rapidly being demonstrated at increasingly higher levels of the THz frequency band (0.3-3THz). The primary drivers for these advances are highly-scaled Indium Phosphide (InP)-based transistor technologies, both high electron mobility transistors (HEMTs), and heterojunction bipolar transistors (HBTs). These technologies benefit from the high electron velocities, low Ohmic contact resistances, and large heterojunction offsets achievable in the InGaAs/InP material system. Both transistor technologies have been demonstrated with power gain cut-off frequencies approaching or exceeding 1THz [1,2,3] and offer the potential for even higher frequency operation. THz monolithic integrated circuits (TMICs) will permit the realization of compact transmitters and receivers eliminating lossy waveguide transitions while making possible arrays with single wavelength element spacing.

While most reported TMIC demonstrations have been realized in high Indium-content InGaAs-channel HEMTS [4,5], our work focuses on the development of a THz InP HBT technology. InP double heterojunction bipolar transistors (DHBTs) with a widebandgap InP collector offer high power handling, high digital logic speeds and high levels of integration. Whereas, III-V HEMT technologies generally utilize two-level MMIC type wiring with air-bridges, InP HBTs are typically realized in multi-level thin-film wiring environments. The HBT platform, therefore, offers the potential for realizing highly integrated complex transmitter and receivers at THz frequencies.

In working towards this target, we have developed sets of building block IC components all operating at >300GHz. These demonstrations include: a two-stage cascode amplifier with 20dB gain at 315 GHz [6], fundamental oscillator circuits operating to >500GHz [7], and dynamic frequency dividers operating to >325GHz [8]. More recently, we have used these building block circuits to fabricate TMICs with increasing complexity. We have demonstrated a fundamental 300GHz phased locked loop circuit (PLL) that includes a fundamental VCO, 2:1 dynamic frequency divider, fifth-order sub-harmonic phase detector, and active loop filter integrated on a single chip (61 HBTs) [9].

In this work, we report on the details and characteristics of the 0.25µm InP HBT IC technology used for our TMIC demonstrations. Interconnect and packaging considerations are also reviewed.

2 InP HBT Technology

Scaling laws for increasing the bandwidth of InP HBTs are outlined in [10]. Structurally increasing the HBT bandwidth requires vertical scaling of the transistor epitaxy and lateral scaling of the transistor junction dimensions. Scaling of junction dimensions requires commensurate improvements in the emitter and base Ohmic contact resistivities.

A key technological challenge in obtaining InP HBTs with THz bandwidths is obtaining sufficiently low Ohmic contact resistivities in self-aligned process flows. These process flows must also maintain high yield as the transistor dimensions are scaled. Our HBT process features a vertical electroplated emitter contact with dielectric sidewall spacers for realizing a highly scaled self-aligned base-emitter junction.

2.1 HBT Epitaxy

The HBT epitaxy has a 30nm InGaAs base with high carbon doping (>5x10^{19}cm^{-3}) to reduce the base contact resistivity. A base contact resistivity ρ_c~5 Ω-µm^2 is extracted from Transmission Line Model (TLM) measurements on fabricated HBT wafers. The N- collector region is 150nm thick. The base-collector heterojunction grade design includes an InGaAs setback layer, a thin chirped-

superlattice InGaAs/InAlAs grading layer, and an InP pulse doping layer. We note that in scaling our 0.5μm InP HBT process [11] to 0.25μm we have not vertically scaled the collector thickness (150nm). This was done to enhance the HBT f_{max} for tuned-circuit operation at THz frequencies.

Super-lattice grading is also used at the base-emitter junction between the InP emitter and the InGaAs base The B-E grade and emitter cap design have been optimized to reduce the extrinsic emitter resistance. The grade is observed to significantly reduce the forward collector current ideality factor at high currents relative to abrupt junction HBTs, improving the HBT transconductance at a given collector current. Our graded junction HBTs demonstrate an ideality factor n_C = 1.1 extracted from measurements of the low-frequency (500MHz) transconductance versus collector current. From the same measurement, an extrinsic emitter resistance of ~4 Ω-μm^2 is extracted. The B-E grade can also be used to provide a passivation ledge in the extrinsic base region beneath the dielectric sidewalls. We have observed that for thin InGaAs base layers (<30nm), surface depletion of the exposed base can increase the sheet resistance by 20-30%. By leaving the base-emitter grade in the sidewall regions, this effect is reduced, thereby improving the base access resistance.

2.2 HBT IC Fabrication

2.2.1 Device Fabrication

Electron-beam lithography is used to define the emitter contact. The contact is formed using an Au-based electroplating process [11]. The electroplated metal is conformal the resist profile and provides a large height-to-width ratio and vertical sidewall profile. These properties facilitate the formation of dielectric sidewall spacers on the contact. After, emitter contact formation the self-aligned emitter mesa etch is performed using a combination dry/wet etch process. Dielectric sidewall spacers are then formed on the emitter contact passivating the base-emitter junction. The sidewall spacers provide electrical isolation and set the physical separation between the emitter contact and the self-aligned base contact that is deposited around it. I-line photolithography is used for all process steps besides the emitter contact and the remaining process flow follows that of a standard triple-mesa HBT. Benzocyclobutene (BCB) is used as a final HBT passivation and planarization layer. The BCB is etched to expose the emitter contact and vias are formed to the base and collector contacts. An electroplated Au process is used to form the first interconnect level. Figure 1 shows a top down SEM image of a 0.25μm HBT prior to BCB passivation.

2.2.2 Interconnect Fabrication and Packaging

The IC technology includes a thin-film 3-level IC wiring environment tailored to support the requirements for integrated THz transmitters and receivers. The wiring utilizes a BCB interlayer dielectric (ε_r = 2.7) and electroplated

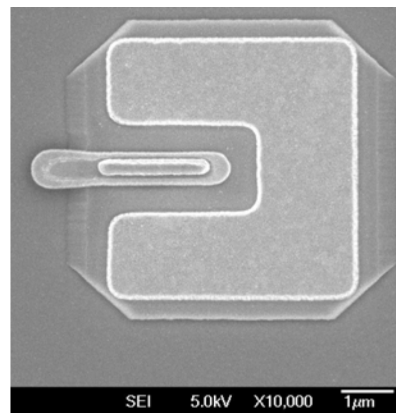

Figure 1 Top down SEM of 0.25μm HBT prior to BCB dielectric passivation.

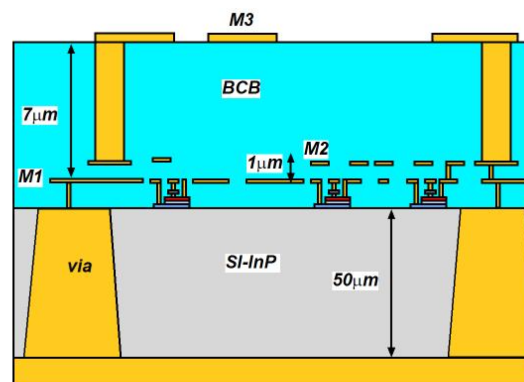

Figure 2 Schematic cross-section of InP HBT IC thin-film wiring environment.

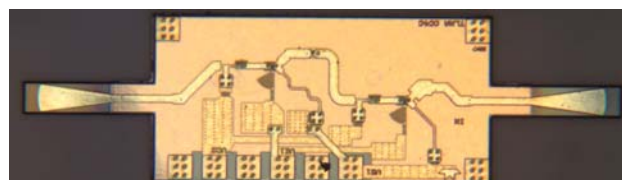

Figure 3 Chip photograph of 300GHz LNA design with integrated waveguide probes after backside etch singulation process. Chip dimensions are 1000×500μm^2

Au-based metallization. The first two wiring levels (M1, M2) are separated by a 1μm BCB layer. These layers support narrow lines and fine pitch and can be used for low delay, low parasitic wiring in lumped analog circuit blocks. The upper level metallization (M3) is separated from M1 by a thicker 7μm BCB layer. These layers can be used to form low-loss microstrip lines using either standard (M3 signal, M1 ground) or inverted (M1 signal, M3 ground) configurations. A cross-section of the HBT wiring environment is shown in Figure 2.

The use of top-side thin-film microstrip wiring permits the use of thicker InP substrate thickness than could be used with traditional CPW or microstrip utilizing a backside ground plane. For IC packaging, wafers are thinned to 50μm and substrate vias are formed for substrate mode control. The substrate vias are formed using an elevated

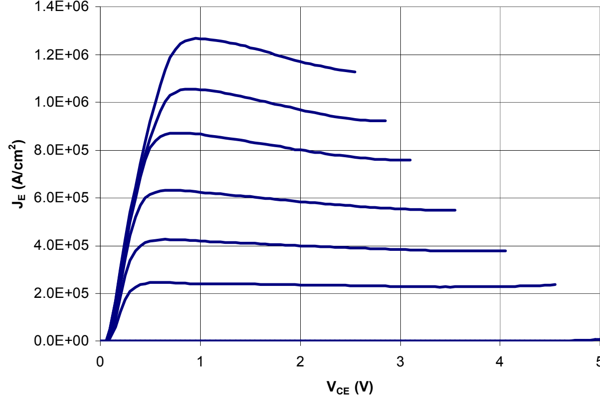

Figure 4 Measured common-emitter I-V characteristics 0.25x4 μm^2 HBT

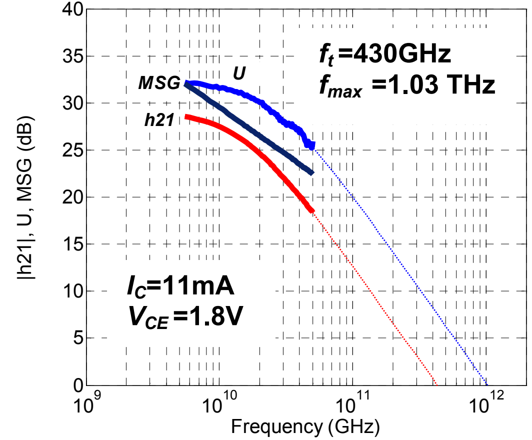

Figure 5 Measured transistor gains of 0.25x4 μm^2 HBT

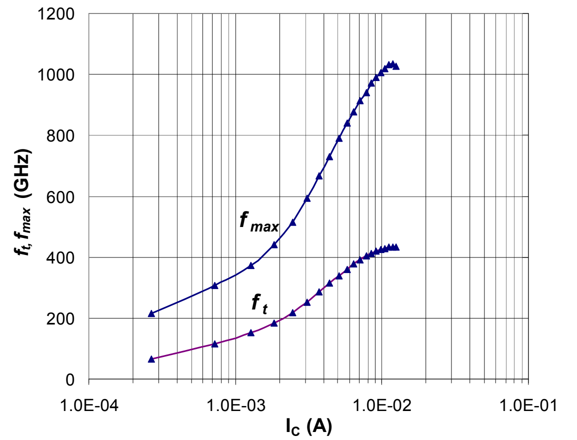

Figure 6 Extrapolated f_t and f_{max} of 0.25x4 μm^2 HBT versus collector current at V_{CE} = 1.8V

temperature HBr-based ICP etch process. To facilitate waveguide packaging, this etch process is also used for die singulation. This process permits the formation of narrow InP extensions that can support waveguide probes (waveguide-to-chip transitions) that extend into rectangular waveguide channels. The extension minimizes the break in the waveguide sidewall, and the etch process can be used to remove the substrate immediately beneath the probe improving probe performance. Figure 3 shows a chip photograph of a 300GHz LNA with integrated waveguide probes after chip singulation. Waveguide probes designs have been separately characterized with through-line test structures in waveguide blocks. Probe insertion losses of <1dB per transition have been measured in the WR-3 (220-325GHz) waveguide band.

2.3 HBT Characteristics

2.3.1 DC Performance

Fabricated HBTs demonstrate a DC current gain (β) of ~20, and a common emitter breakdown voltage of 4.3V (J_E = 10μA/μm^2). The transistors support high current and power densities. This is illustrated in the common-emitter I-V characteristics (Figure 4) that show the transistor operating at current densities of >10^6 A/cm^2, and power densities of >20 mW/μm2.

2.3.2 RF Performance

Accurate on-wafer S-parameter measurements of highly-scaled HBTs are challenging because the reverse transmission measurements (S12) are easily corrupted by coupling between on-wafer probes or by unwanted mode propagation in thick semiconductor substrates. To address these issues, we utilize thin-film microstrip on-wafer calibration structures. The microstrip is formed using the first layer metal (M1) as a ground plane and the topmost M3 level as the signal line.

A multi-line Through-Reflect-Line (TRL) calibration is performed using on-wafer standards. The calibration reference plane is placed at the middle of a 400μm long microstrip line, providing adequate probe separation and minimizing the extrinsic parasitics that are extracted from the transistor measurements. The capacitive and inductive loading effects of vias through the thick BCB layer are deembedded from the measurements using open and short circuit deembedding structures. With this method, an input and output capacitance of only ~4fF is deembedded from the transistor measurements.

Figure 5 shows the measured RF transistor gains to 50GHz of a 0.25x4μm^2 HBT. The measurements were performed with an Agilent PNA-X vector network analyzer. The maximum current gain cutoff frequency (f_t) and maximum power gain cutoff frequency (f_{max}) are extracted from least-squares fits to single-pole transfer functions of the measured h_{21} and Mason's unilateral power gain (U), respectively. The extrapolated f_t and f_{max} of the transistor are 430GHz and 1.03THz, respectively, at a bias condition of V_{CE} =1.8V I_C =11 mA. Figure 6 shows variation of f_t and f_{max} versus collector current for a 0.25x4 μm^2 HBT at a V_{CE}=1.8V.

We note that the f_{max} of the transistor is enhanced by collector-base capacitance cancellation. This well-known effect in III-V bipolar transistors [12] results from electron velocity modulation in the collector space charge region

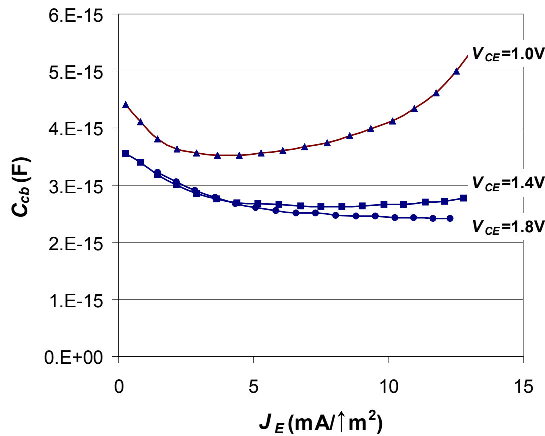

Figure 7 Extracted base-collector capacitance of 0.25x4 µm^2 HBT versus collector current. C_{cb} is extracted from –imag(Y_{12})/ω at low frequencies.

with applied potential. The redistribution of the charge density profile of mobile electrons caused by the change in velocity screens the base and collector terminals from changes in the electric field. At moderate base collector-voltages, an effective base-collector capacitance reduction of ~30% is observed with increasing current. Figure 7 shows the extracted C_{cb} versus collector current for a 0.25x4µm^2 HBT.

2.3.3 HBT Modeling

The Agilent III-V HBT model [13] is used for large signal modelling our InP HBTs. The model is capable of capturing many of the unique properties of III-V bipolar transistors that cannot be modelled with standard Silicon BJT models. These properties include: collector transit time modulation with applied bias, collector-base capacitance cancellation and base-collector current blocking at high collector currents.

Even with our thin-film microstrip calibration structures, accurate transistor measurements at THz frequencies (>300GHz) are difficult. Transistor parameters are therefore extracted from low frequency measurements. The HBT model includes all relevant transistor parasitic elements and should scale well to frequencies approaching the transistor cutoff frequencies; an assertion that is supported by the good agreement that we have observed between measurements and simulation for >300GHz IC designs.

3 Conclusions

We have presented a high performance 0.25 µm InP HBT IC technology with an extrapolated power gain cutoff frequency of 1THz. The technology is suitable for IC demonstrations at the lower end of the THz frequency band. The initial demonstration of key circuit building blocks presented shows the technology offers a promising path for developing fully integrated THz transceivers. Future work is focused on the development of a 130nm HBT technology for operation at even higher frequencies.

4 Acknowledgements

The authors thank the Teledyne Scientific cleanroom staff for IC fabrication. This work was supported by the Defense Advanced Research Projects Agency (DARPA) under the Program, contract N0. HR0011-09-060. Program support from Dr. John Albrecht (PM DARPA) and Dr. Alfred Hung (PM ARL). The views, opinions and/or findings contained in this article are those of the authors and should not be interpreted as representing the official policies, either expressed or implied, of DARPA, or the Department of Defense.

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