60 nm gate length Al_2O_3 / $In_{0.53}Ga_{0.47}As$ gate-first MOSFETs using InAs raised source-drain regrowth

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Overview

- Why III-V MOSFETs?
- Device Physics and Scaling Laws
- Process Flow
- Measurements
- Conclusions

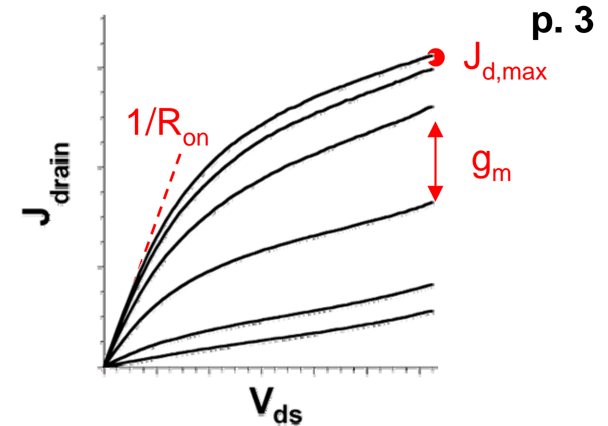
Why III-V VLSI?

Higher electron velocities than Si MOS

For short L_g FETs, $J_{drain} = q \cdot n_{s,channel} \cdot v_{sat}$

Transconductance, $g_m = C_{effective} \cdot v_{sat}$

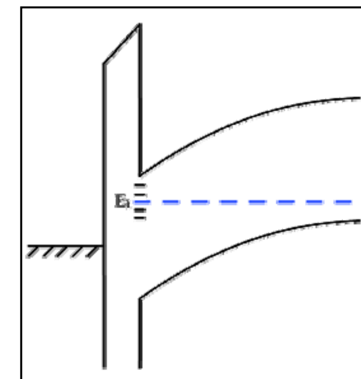
J_d and g_m are key figures of merit in VLSI



However:

J_d and g_m degraded by source large R_{access}

J_d and g_m degraded by interface trap density, D_{it}

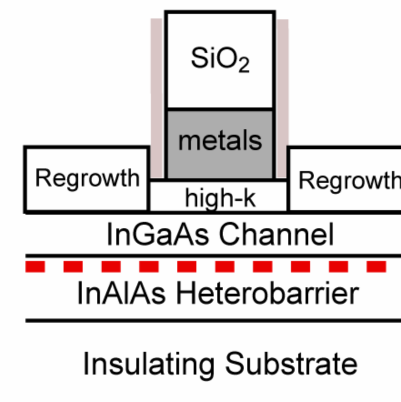


Therefore, we must develop:

Low access resistance source/drain contacts

Thin, high-k, low D_{it} dielectrics on InGaAs

Fully self-aligned process modules



*MOSFETs have been, and <u>always</u> will be, a **materials challenge**.*

FET Device Physics

$$C_{ox} = \frac{\varepsilon_o \varepsilon_r}{t_{ox}}$$

$$C_{depth} \approx \frac{\varepsilon_o \varepsilon_{channel}}{t_{channel}/2}$$

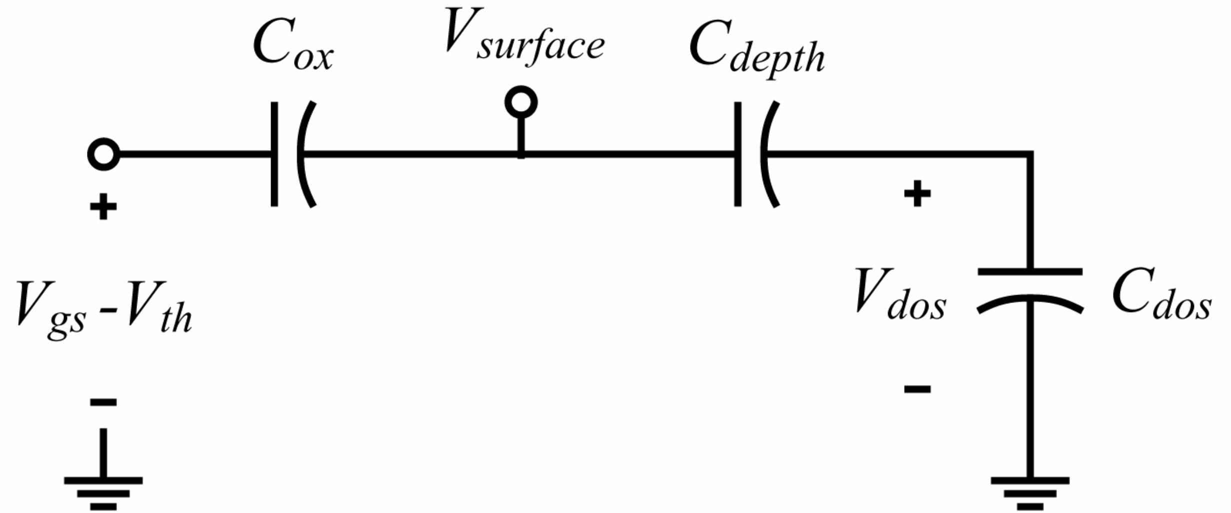
$$C_{dos,2D} = \frac{q^2 g m^*}{\pi \hbar^2}$$

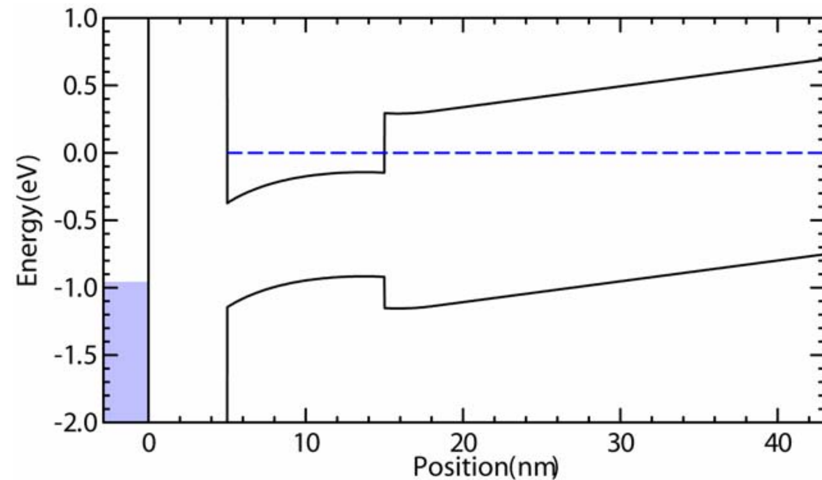
$$n_{channel} = \frac{C_{dos}}{q}(V_{dos})$$

$$J_{drain} = q \cdot n_{s,channel} \cdot v_{sat}$$

$$g_m = C_{effective} \cdot v_{sat}$$

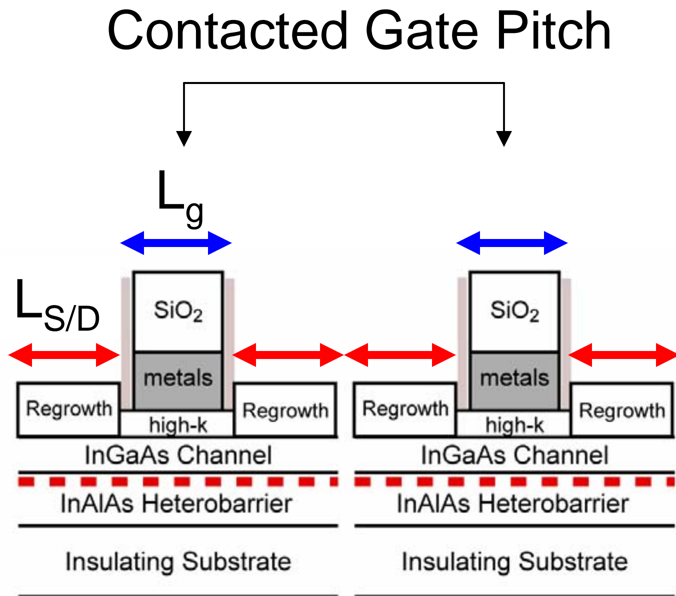
*$C_{effective}$ includes C_{ox}, C_{depth}, C_{dos}

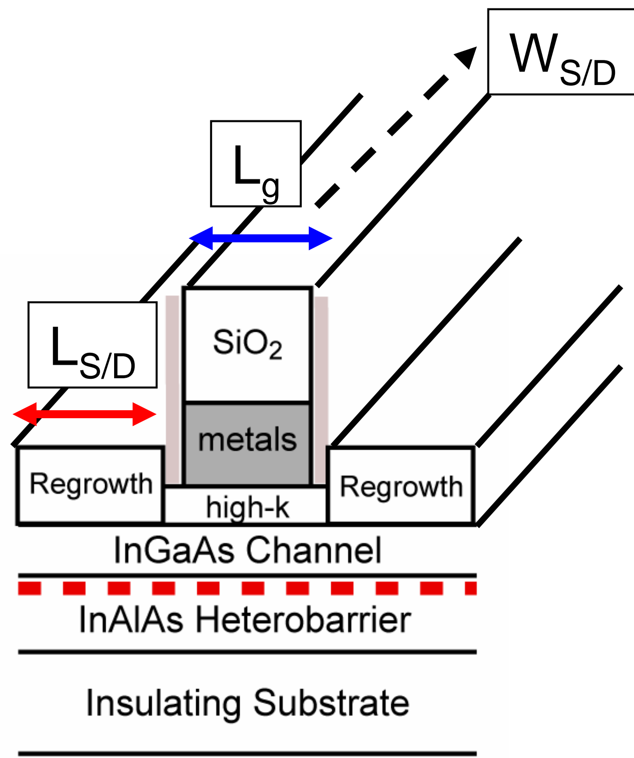




Electron band diagram of a quantum well FET

FET Device Scaling





Si CMOS scaling: Contacted gate pitch 4x the gate length[1)]

4:1 reduction of contact area[2)] → 4:1 reduction of $\rho_{contact}$

22 nm node → 33 nm $L_{S/D}$ → For $L_{S/D} = L_T$, requires 5×10^{-9} ohm-cm^2 $\rho_{contact}$

$$\text{Contact Transfer Length} = L_T = \sqrt{\frac{\rho_c}{R_{sh}}}$$

[1)] S. Natarajan, *et al*, IEDM 2008.

[2)] M.J.W. Rodwell, *et al*, IPRM 2010.

Gate First FET Process Flow

Thick (10 nm) channel

Process damage mitigation

Heavy (~ 9×10^{12} cm^{-2}) δ doping

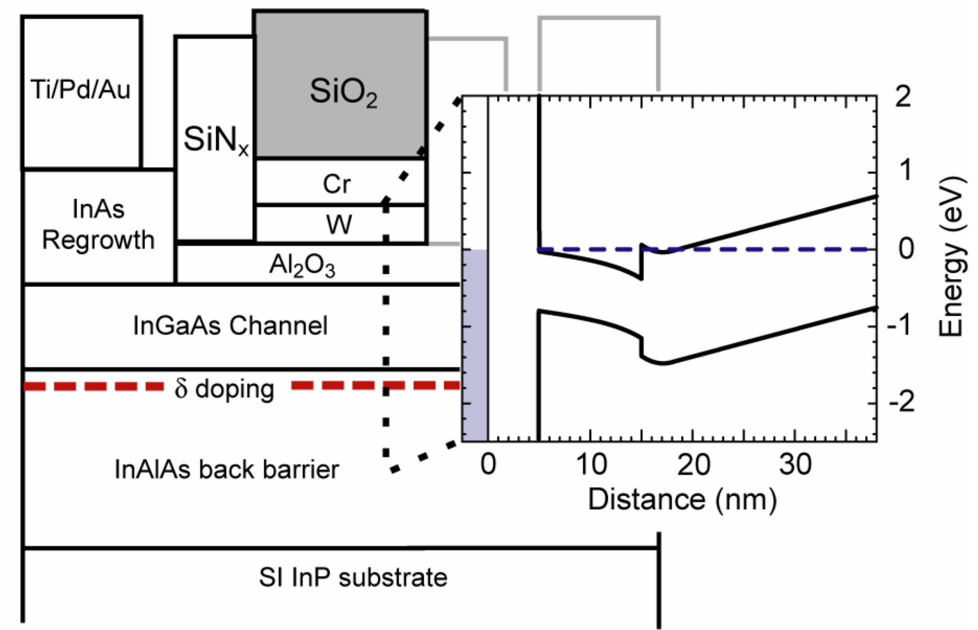
Prevents ungated sidewall current choke

$In_{0.52}Al_{0.48}As$ heterobarrier

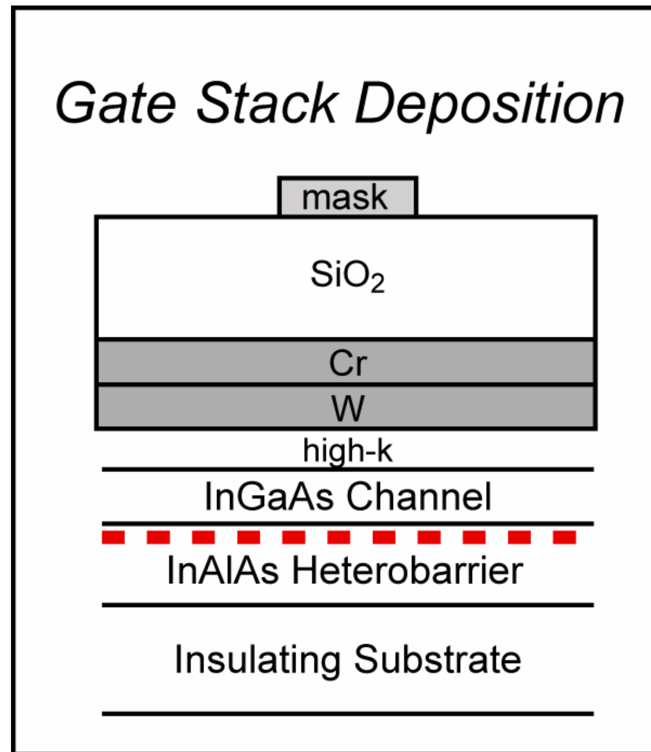
Carrier confinement

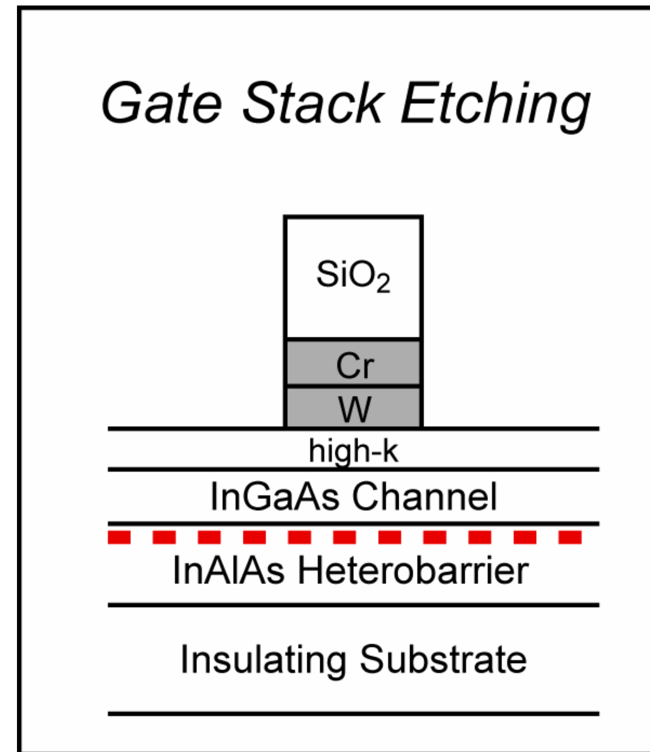
Semi-insulating InP

Device isolation



Gate First FET Process Flow





Front End: Gate Stack Definition

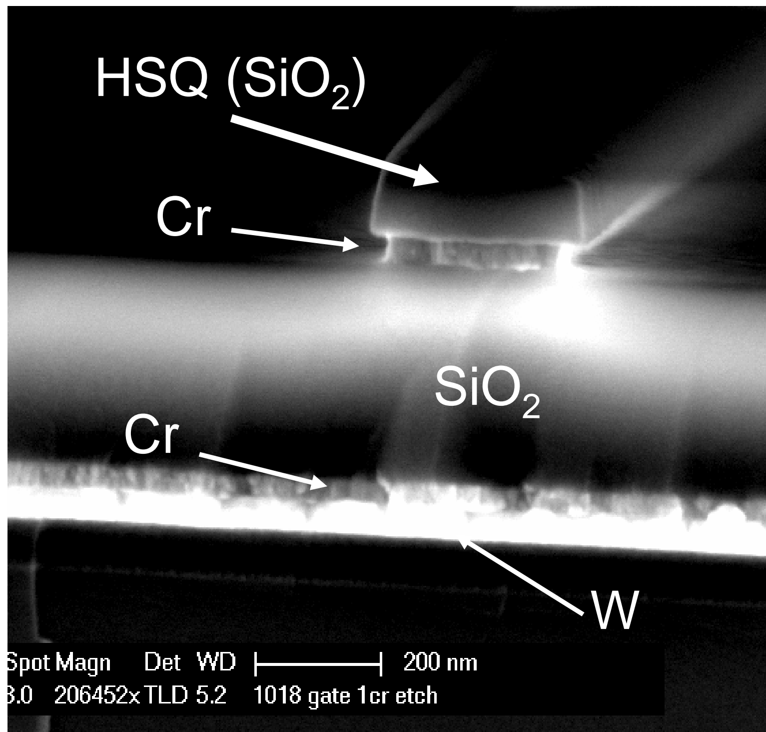
- *In-situ* hydrogen plasma / TMA treatment before Al_2O_3 growth
- Mixed e-beam / optical lithography
- Bi-layer gate (Sputtered W + e-beam evaporated Cr)
  - High selectivity, low power dry etch

FET Process Development

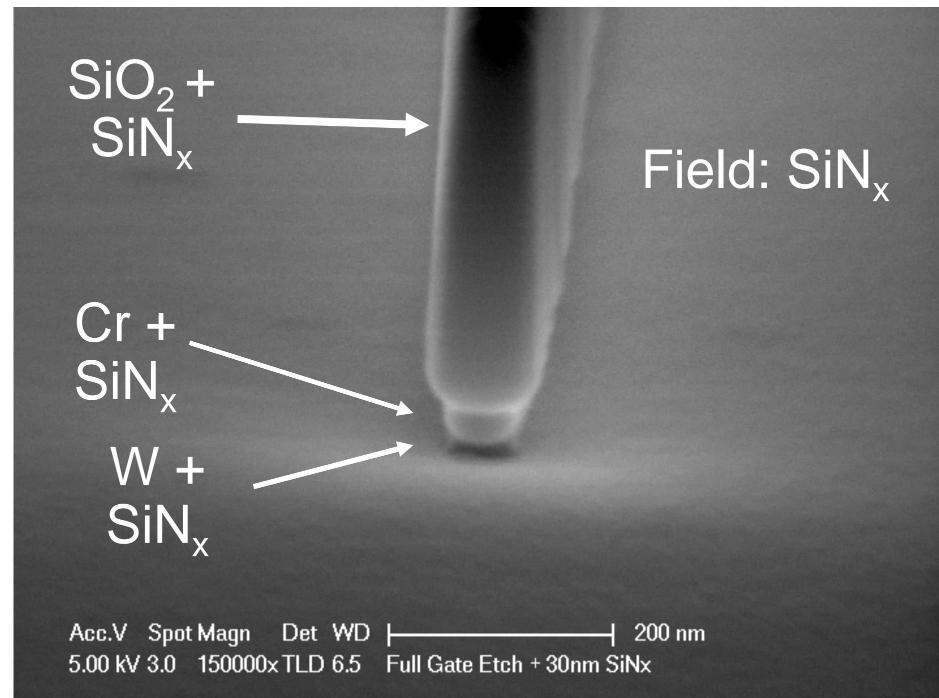
Use optical lithography to produce >0.5um gates

Use electron beam lithography to produce sub-100nm gates

Need to investigate possible e-beam damage to oxides



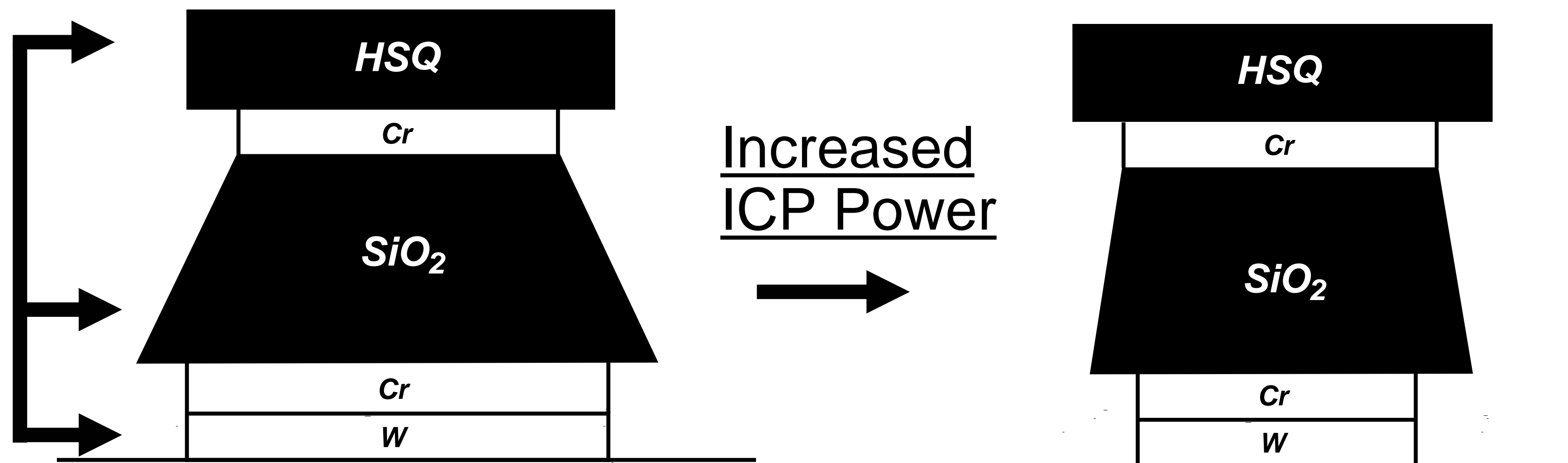
EBL Tests



Finished Gate Etch + Sidewall Deposition

FET Process Development

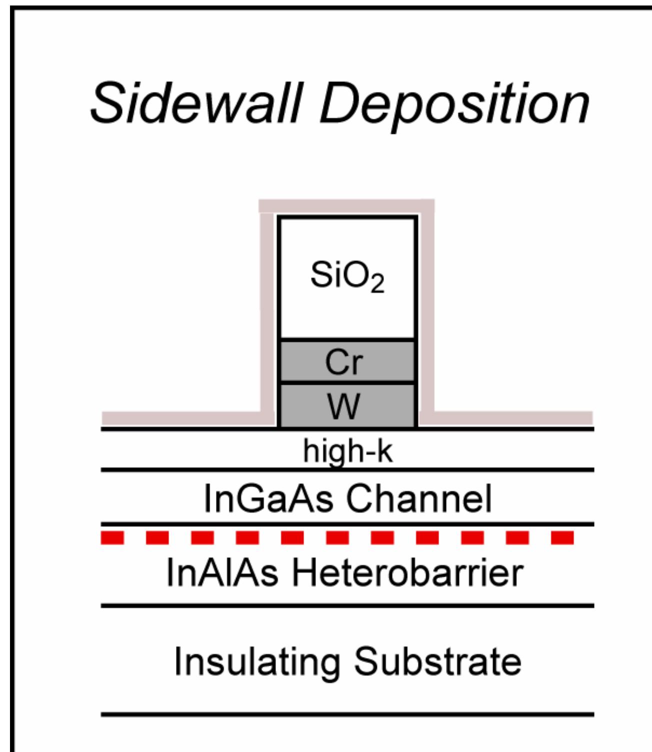
ICP dry etches calibrated to perform at sub-100nm scale

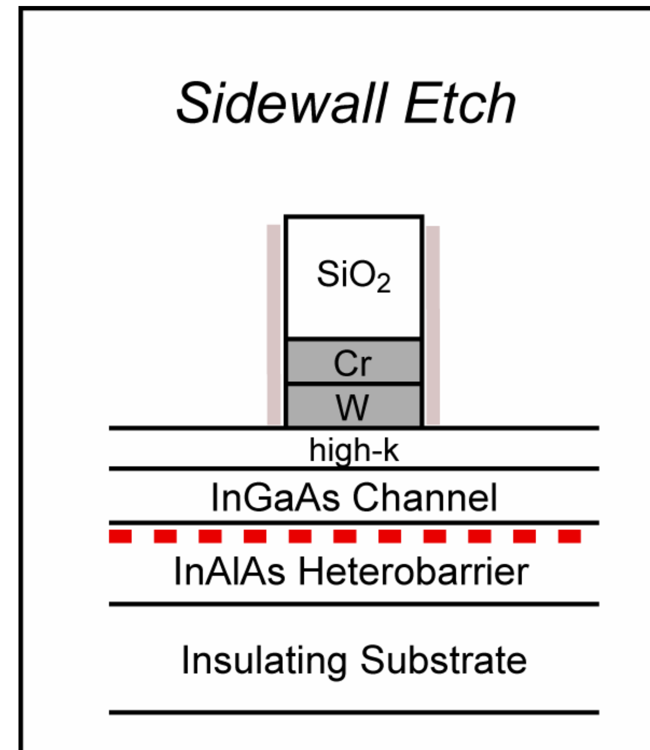


Higher power dry etch → vertical gate stack

Undercutting leads to fallen gates, ungated access regions
→ Minimize Cr undercut by reducing thickness

Gate First FET Process Flow



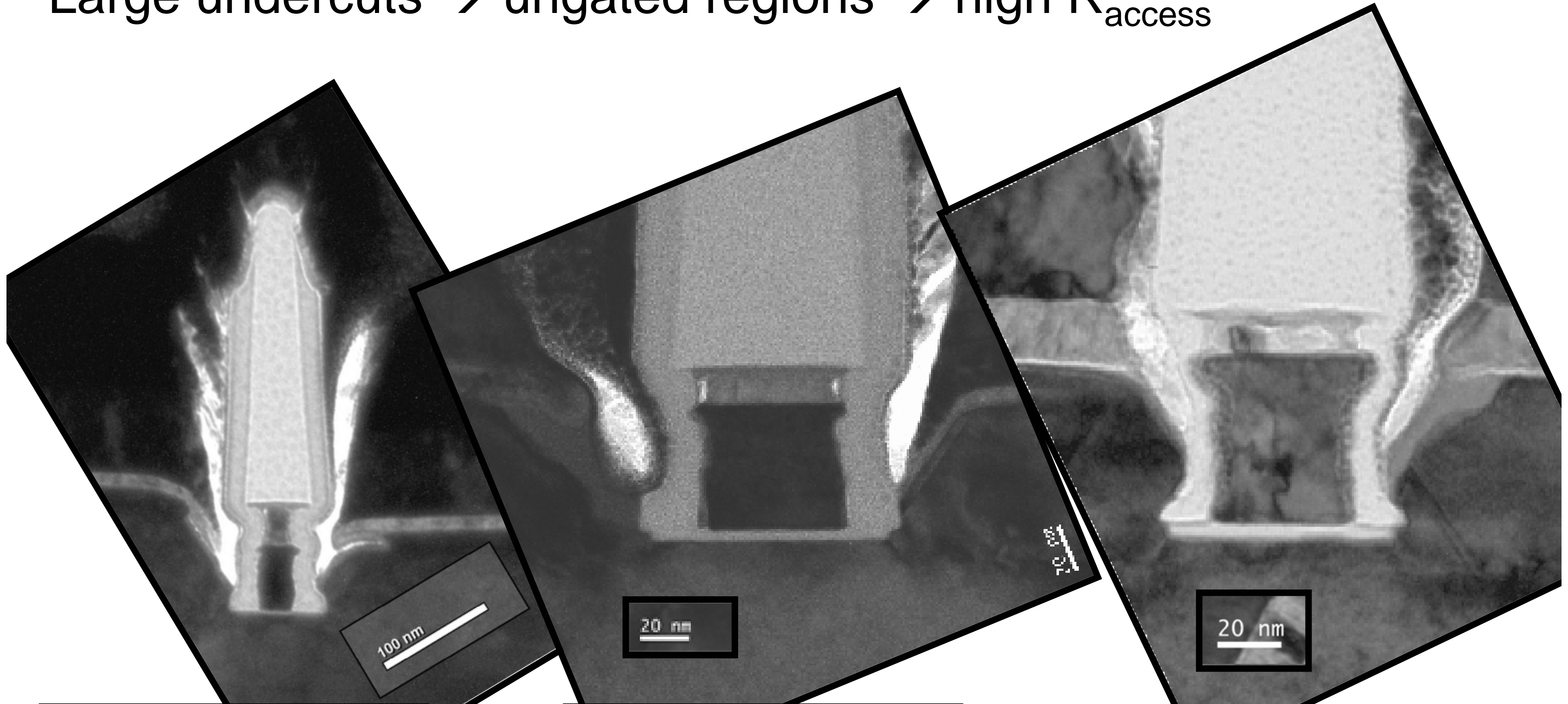


Front End: Gate Stack Definition

- Sidewall Deposition
  - Conformal, protects S/D short circuit to gate
- Sidewall etch
  - Vertical gate stack → self aligned sidewall

FET Process Development

Low power etch → Isotropic etching + undercut → fallen gates
Large undercuts → ungated regions → high R_{access}

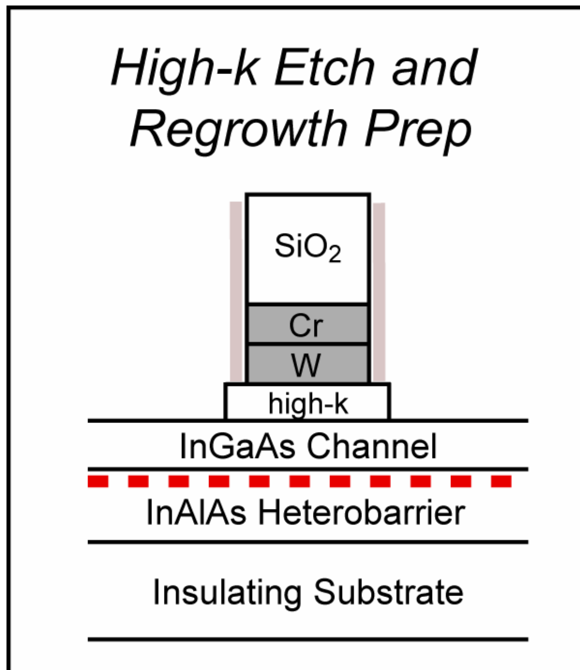


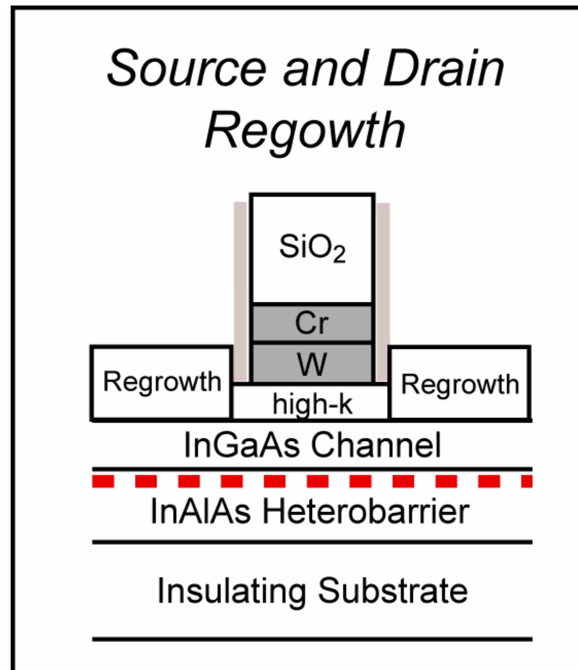
Thick gate stack:
Small L_g ☺
Large sidewall foot ☹
Unreliable gates ☹

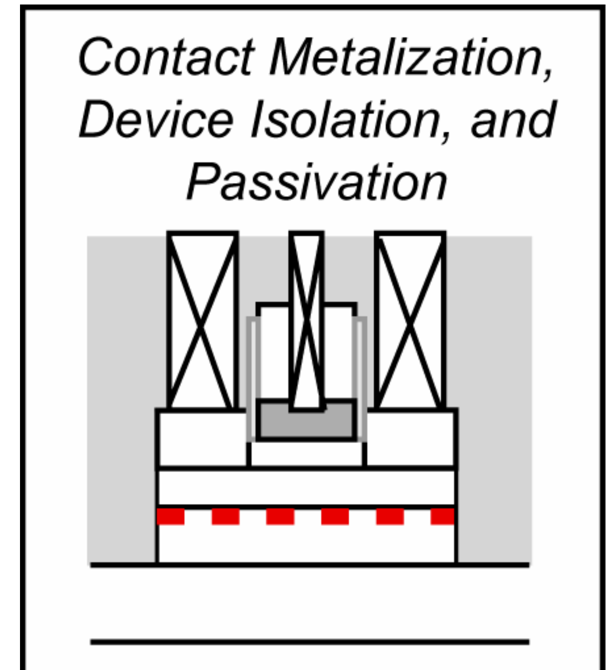
Thin Cr stack:
Small L_g ☺
Large sidewall foot ☹
Repeatable gate etch?

ALD SiO_2 sidewall:
Small L_g ☺
Still sidewall foot! ☹
Unrepeatable gate undercut ☹

Gate First FET Process Flow



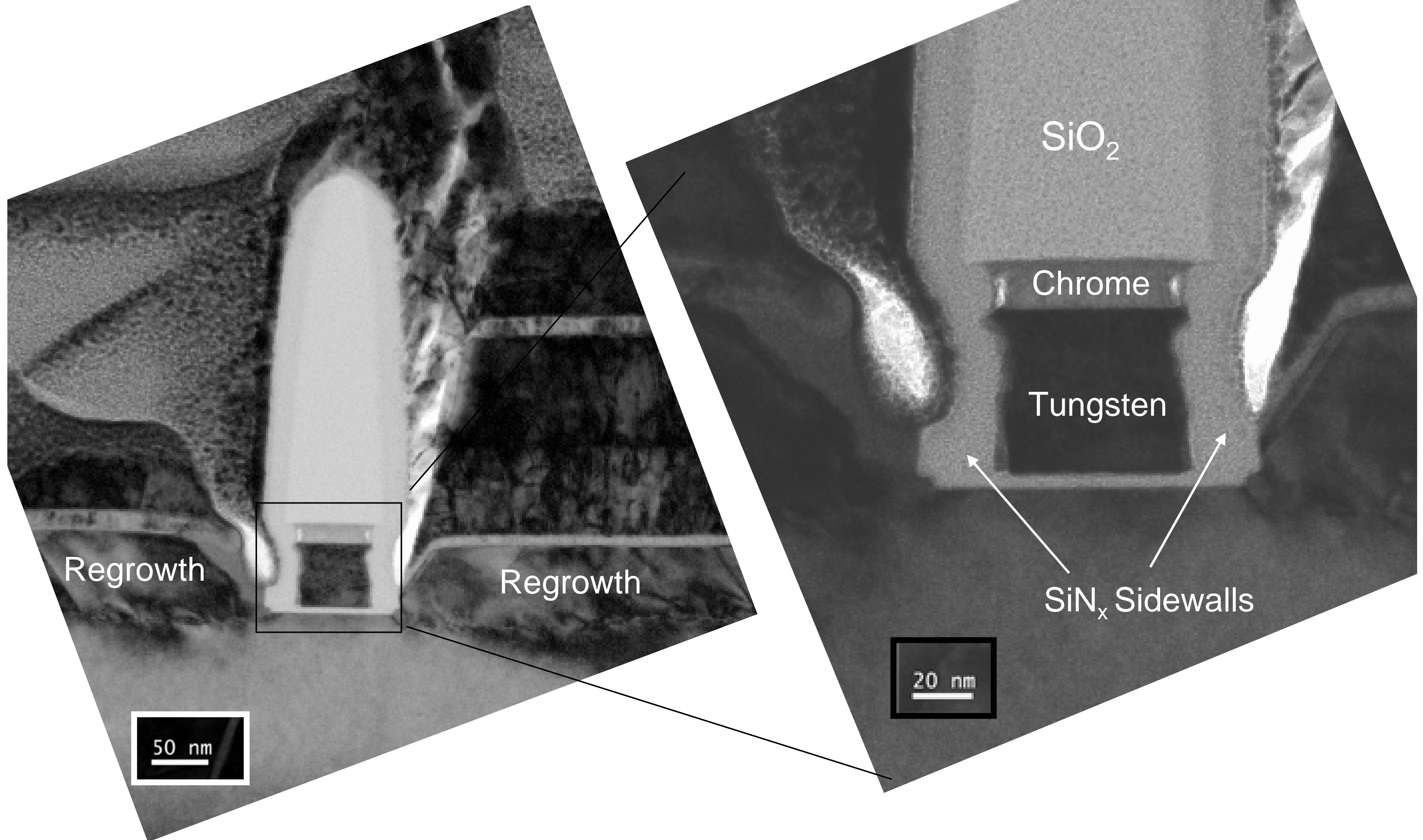




Regrowth and Back End

- Surface preparation
  - UV O_3 exposure to clean the source/drain, removed *ex-situ* before MBE load
- MBE InAs Regrowth
  - Low arsenic flux, high temperature → near gate fill in
- Metallization and Mesa Isolation
  - *In-situ* Mo in MBE optional for lower ρ_c
  - Ti/Pd/Au liftoff
  - Wet etch for mesa isolation

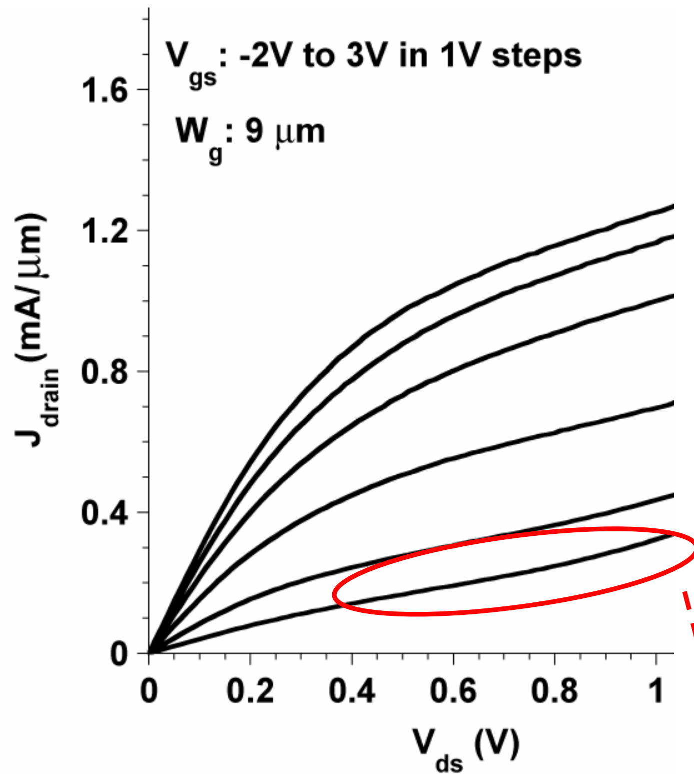
Gate First FET Process Flow



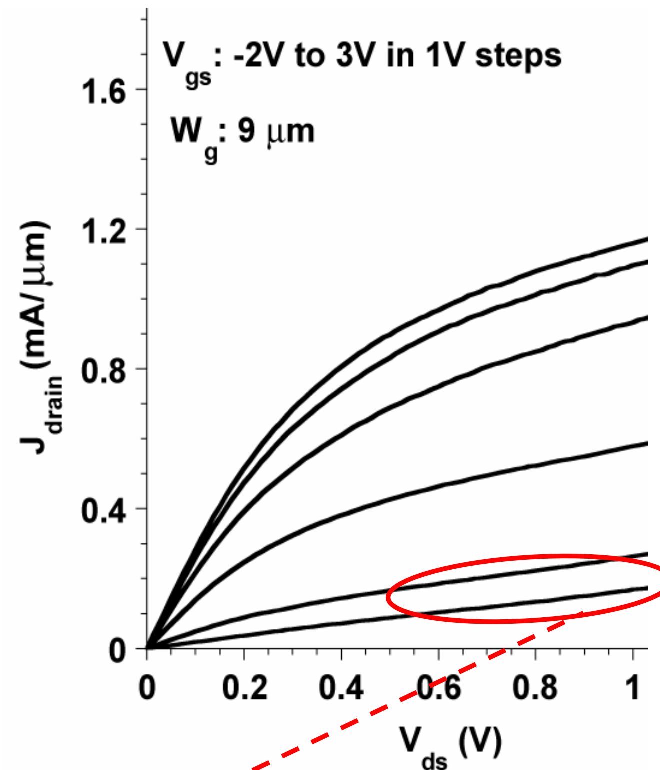
TEM micrographs of 60 nm L_g device

Gate First FET Results

60 nm L_g



115 nm L_g

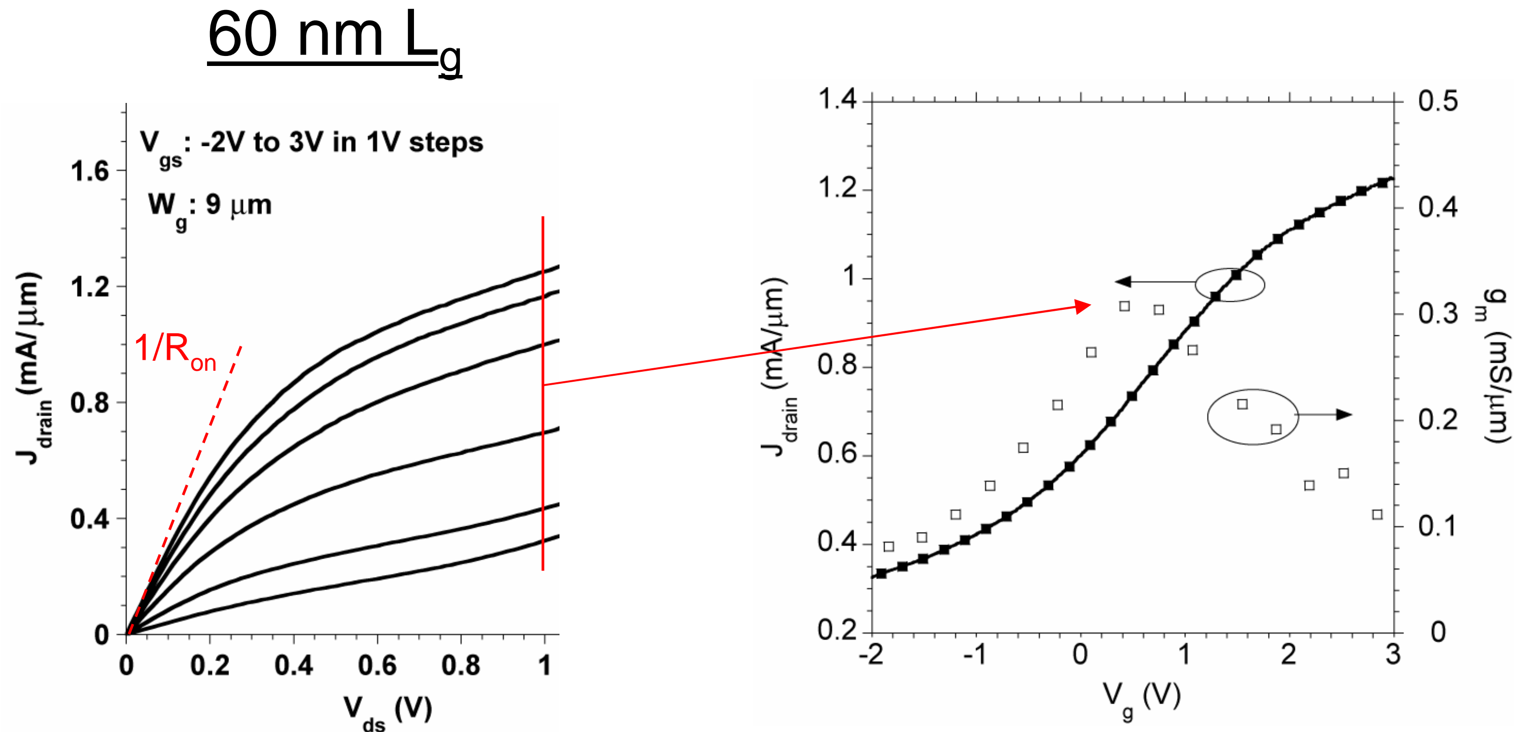


Increased leakage current:

Heavy δ doping leakage path

Drain induced barrier lowering

Gate First FET Results



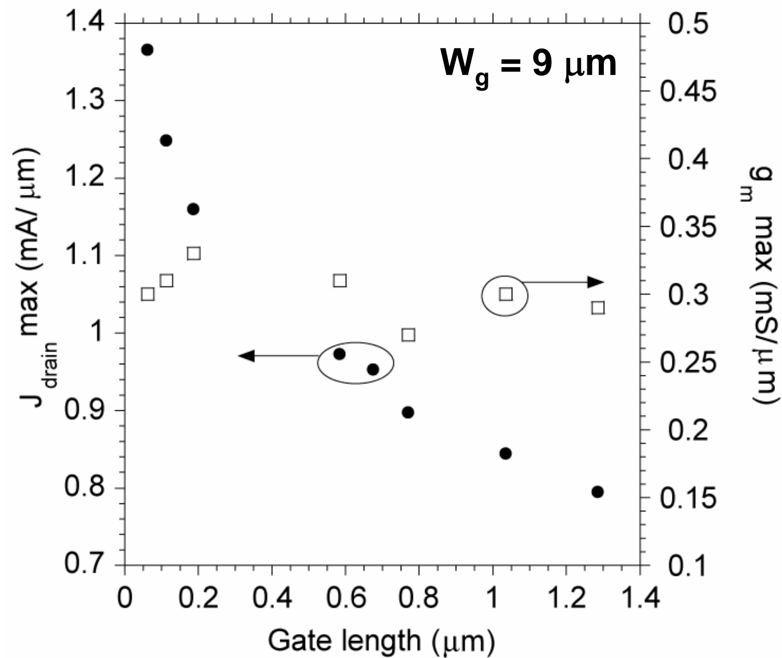
High J_{drain} but depletion mode

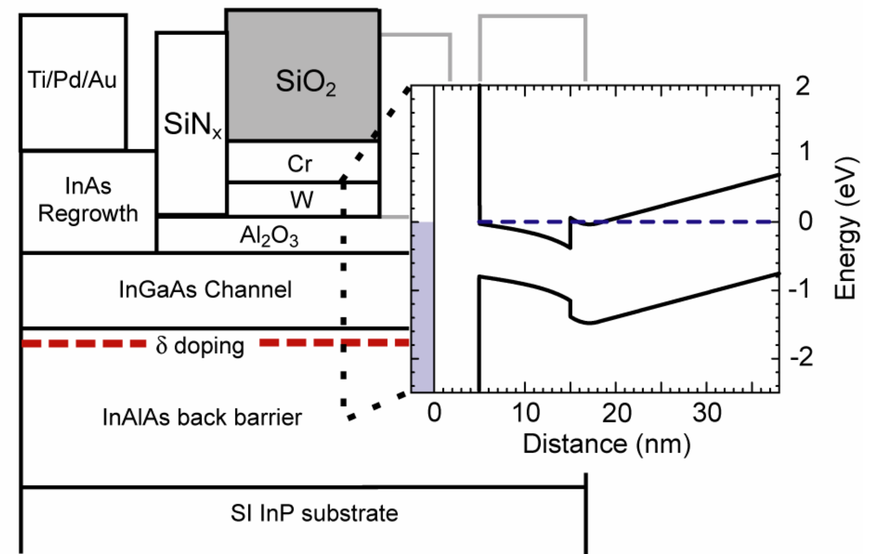
Transconductance: Similar to previous results* (~0.3mS/µm)

Low R_{on} (371 ohm-µm) for InGaAs MOSFETs

*) U. Singisetti *et al, IEEE EDL Nov. 2009.*

Gate First FET Results



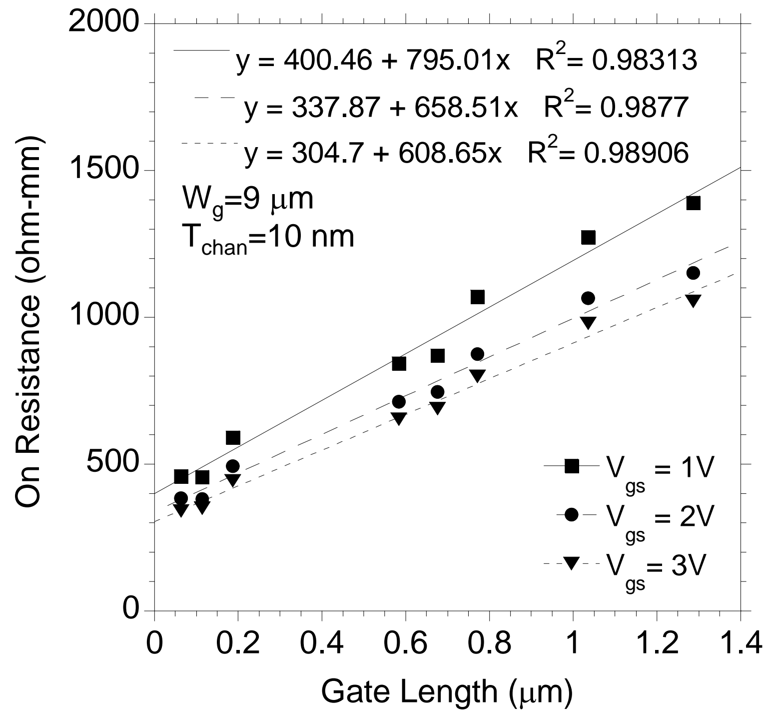


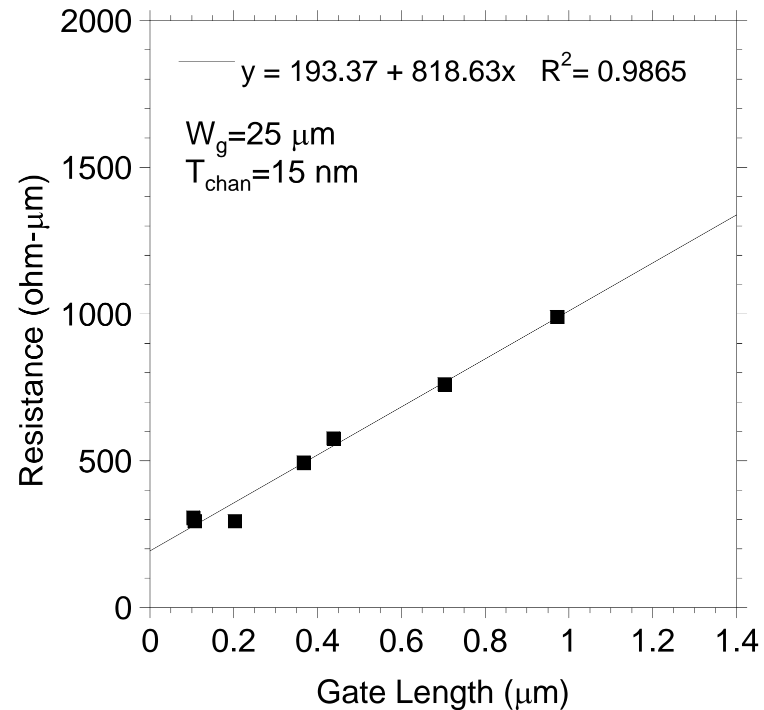
J_{drain} increases rapidly with gate length scaling

Transconductance: Relatively flat with gate length scaling

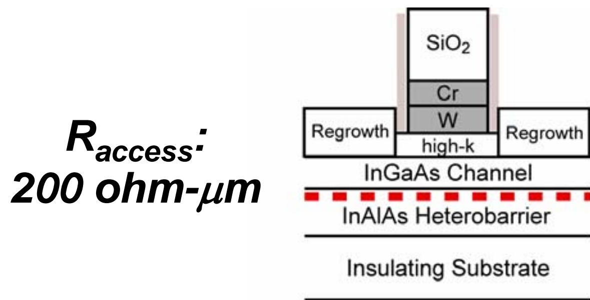
*) U. Singisetti *et al, IEEE EDL Nov. 2009.*

FET: Access Resistance

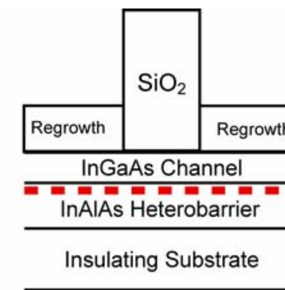




***R_{access}*: 200 ohm-µm**



$$R_{measured} = \frac{R_{sh} L_{gap}}{W} + 2R_{access}$$



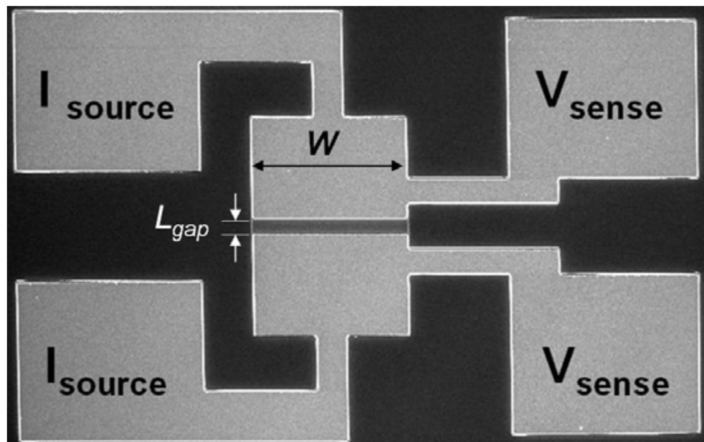
***R_{access}*: 100 ohm-µm**

MOSFET On Resistance

Gateless Transistor Resistance

Gateless transistor effective diagnostic of regrowth

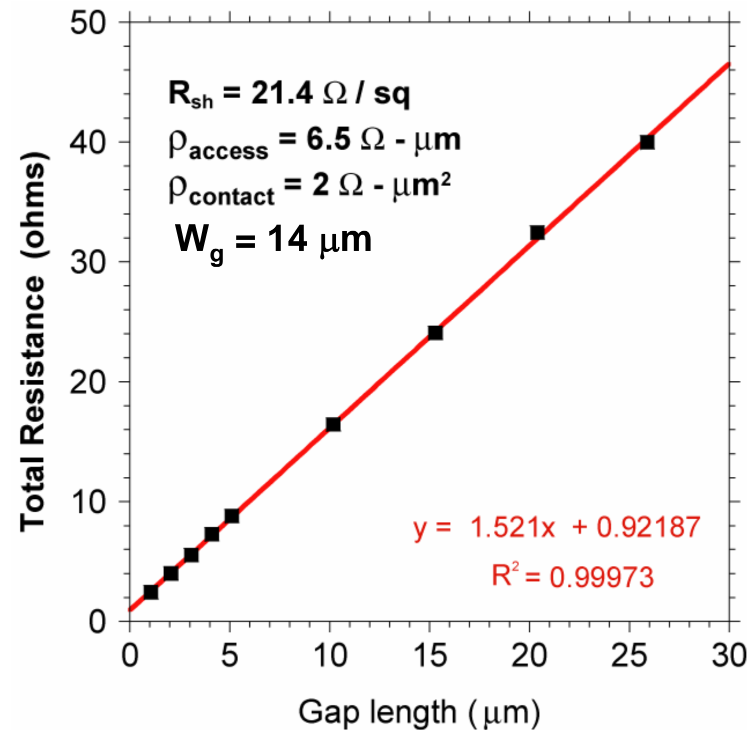
Gate First FET: Metal-Regrowth TLM



$$R_{measured} = \frac{R_{sh} L_{gap}}{W} + 2R_c$$

$$R_c \approx \frac{\rho_c}{L_T W} \text{ for } L > 1.5 L_T$$

$$L_T = \sqrt{\frac{\rho_c}{R_{sh}}}$$



Metal-Regrowth access resistance is not a limiting factor in J_{drain}

Ex-situ Ti/Pd/Au / n-type InAs contacts: $\rho_c = 2 \times 10^{-8}$ ohm-cm^2

In-situ Mo / n-type InAs contacts have shown $\rho_c = 6 \times 10^{-9}$ ohm-cm^2 *

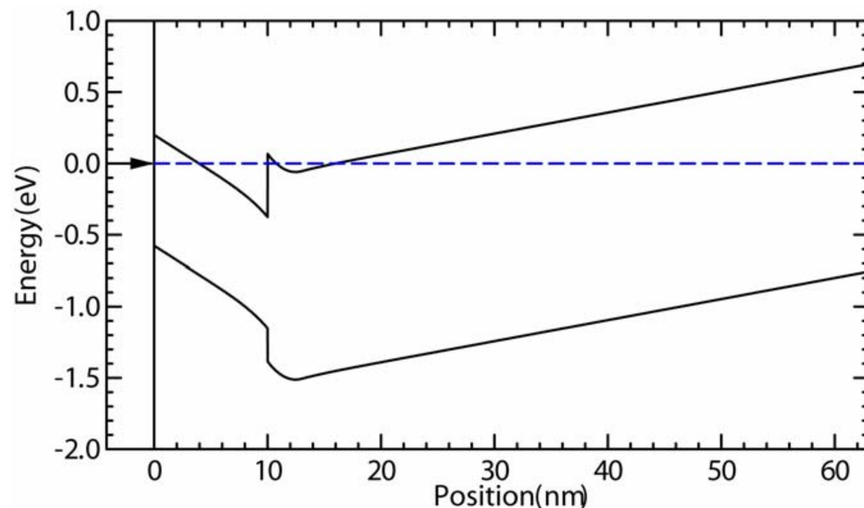
*) M.J.W. Rodwell, *et al*, IPRM 2010.

Gate First FET: Issues

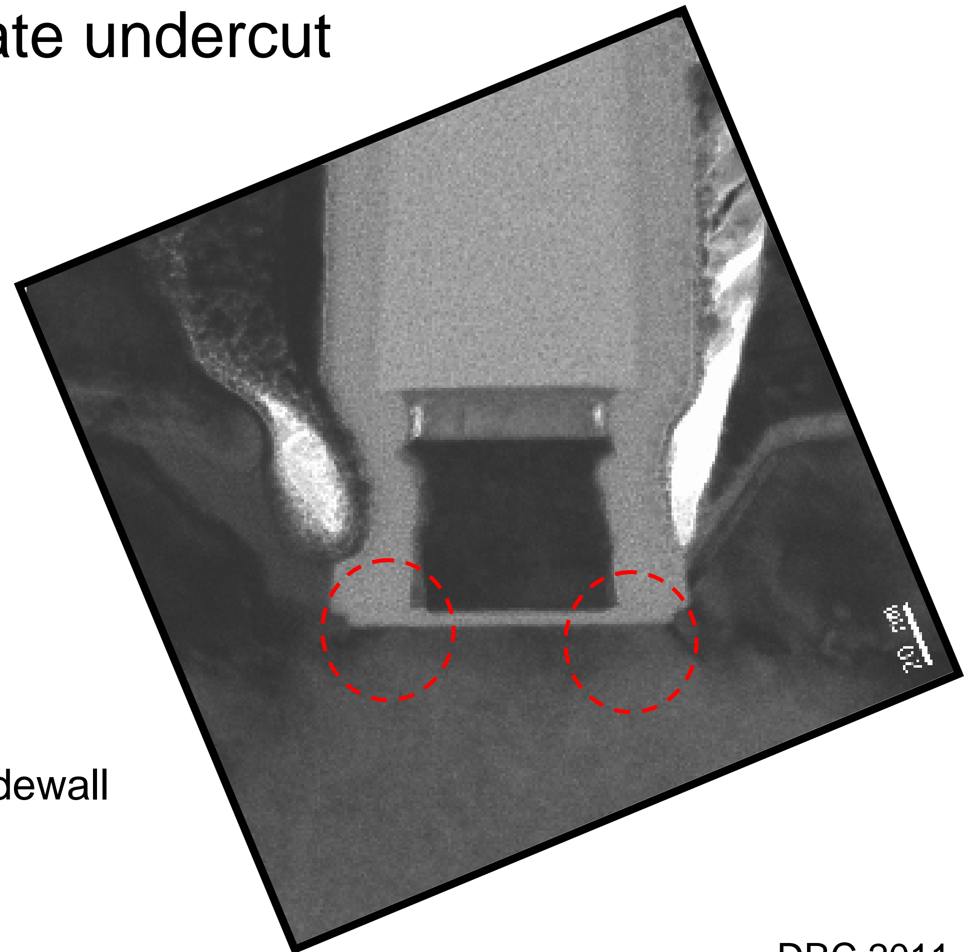
Ungated region → potential current choke

Thinner sidewall can help…

… but hard to control with gate undercut



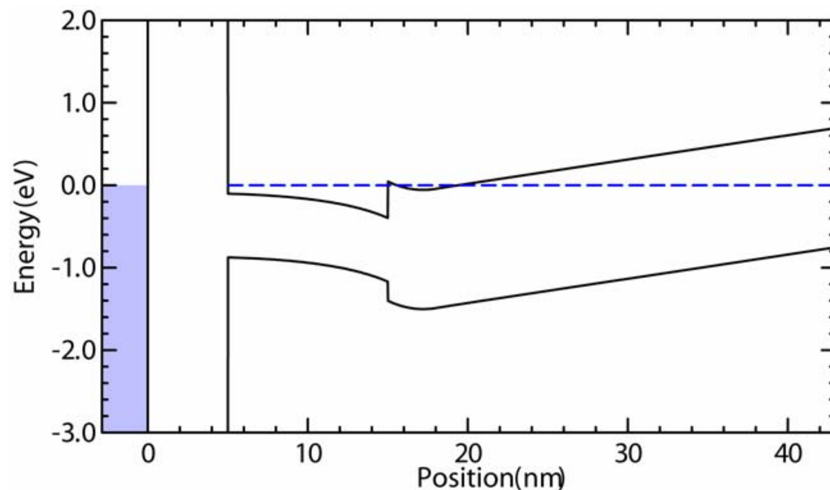
Electron band diagram of channel underneath sidewall



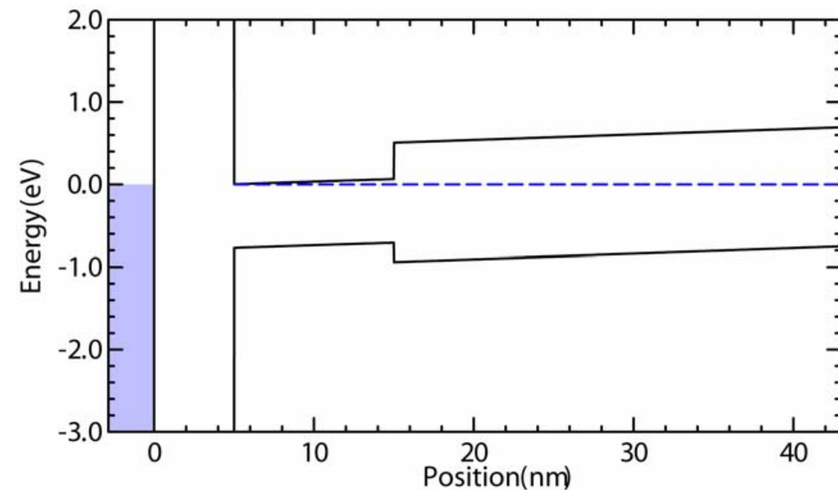
Gate First FET: Issues

Heavy δ doping → parallel conduction, poor g_m

- Large leakage current in device
- Decreases C_{depth} → limits g_m



$9 \cdot 10^{12} cm^{-2}$ δ doping



no δ doping

Must reduce δ doping while maintaining low R_{access}

Conclusions

60 nm gate first InGaAs MOSFET process flow

J_{drain} exceeding 1.2 mA/μm

Low R_{on} = 371 ohm-μm

Self-aligned process flow for sub-100 nm III-V VLSI

Continued research areas

- Minimizing ungated regions
- Thinner dielectrics
- D_{it} passivation techniques

Thanks for your time!
Questions?

contact address: adc [at] ece.ucsb.edu

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