# A 3-Stage Shunt-Feedback Op-Amp having 19.2dB Gain, 54.1dBm OIP3 (2GHz), and 252 OIP3/$P_{DC}$ Ratio

Zach Griffith, M. Urteaga, R. Pierson, P. Rowell, M. Rodwell†, B. Brar

Teledyne Scientific Company, Thousand Oaks, CA 91360, USA

†Department of Electrical and Computer Engineering
University of California, Santa Barbara, CA 93106-9560

e-mail: zgriffith@teledyne.com, phone: 805-373-4104

# Standard design for low distortion amplification

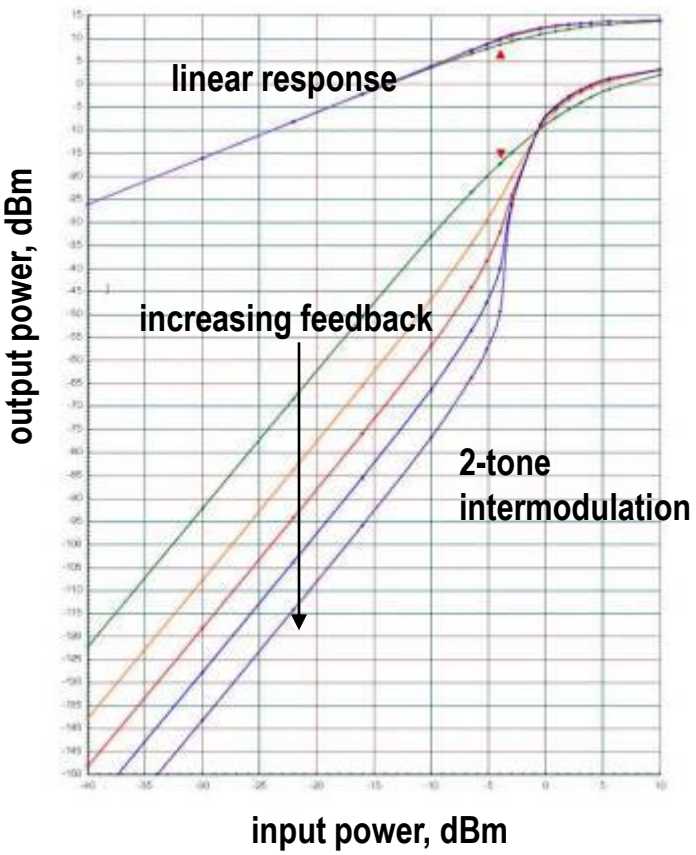


- In simple reactively-tuned RF amplifiers, the output-referred intermodulation distortion intercept (OIP3) is proportional to the DC current (i.e. DC power) dissipation
  - To have high OIP3 (very low power IM3 products), high bias currents and voltages are required
  - Continued system evolution (sensors, radar receivers, multi-carrier communications) requires increased linearity, dynamic range, *and* lower $P_{DC}$
    - This is not possible with existing architectures, invariant of device bandwidth

# mm-wave Op-Amps for linear microwave amplification

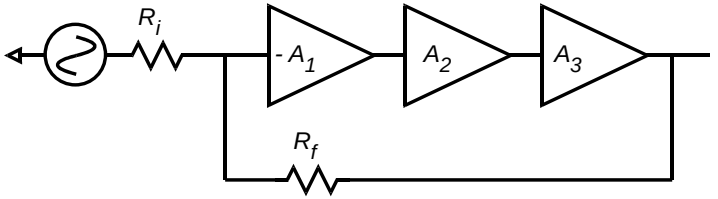


**Strong negative feedback *can* greatly reduce distortion**




modern transistors have high bandwidth, can provide large feedback gain at 2-5 GHz.

but: feedback helps *less* with stages near input




and: any parasitic nonlinear feedback through transistor parasitics will ruin performance

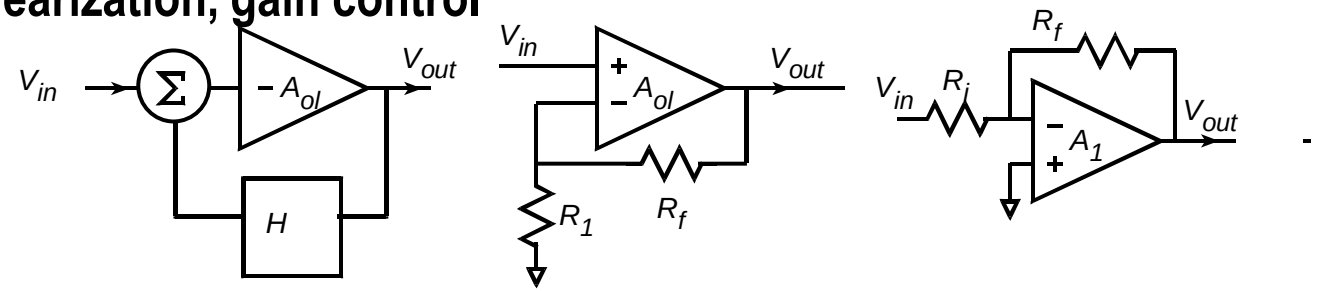
and: compensation for loop stability reduces feedback gain and increases distortion (slew rate)

**Nevertheless**:
...with appropriate IC topologies
...and with fast devices
100 GHz GBW op-amps and
*very low* IM3 levels at 2-5 GHz

# Strong global feedback → strong linearization

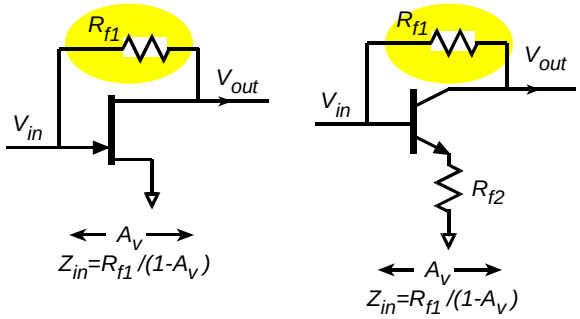


**amplifiers with strong global negative feedback**
**-- for linearization, gain control**

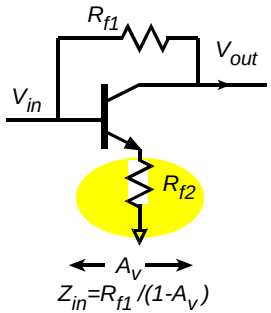



General form  voltage summing  current summing

**weak shunt negative feedback**
**--- for 50 Ohm $Z_{in}$**

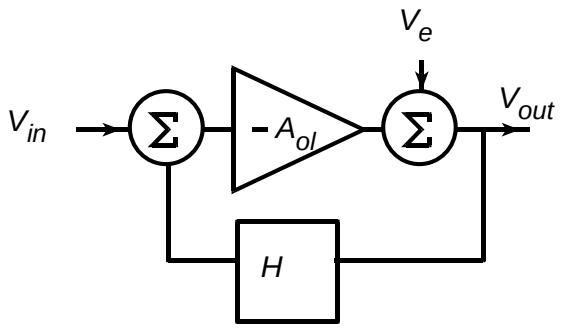



**strong local negative feedback**
**--- linearization**



# Background: suppression of distortion by feedback

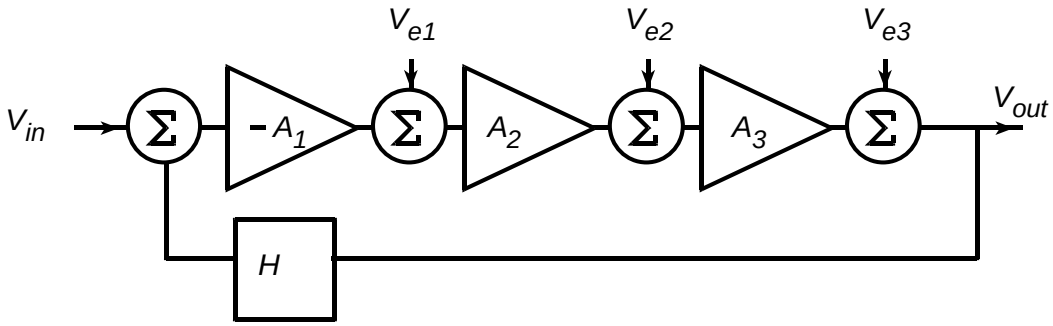





Approximate distortionas independent additive error signal $V_e$

$$V_{out} = A_{CL}V_{in} + (A_{CL}/A_{OL})V_e \quad \text{where } A_{CL} \cong 1/H$$

distortionis reducedin proportionto the ratio of closedloop $A_{CL}$ to open-loop gain $A_{OL}$




With multiplestages

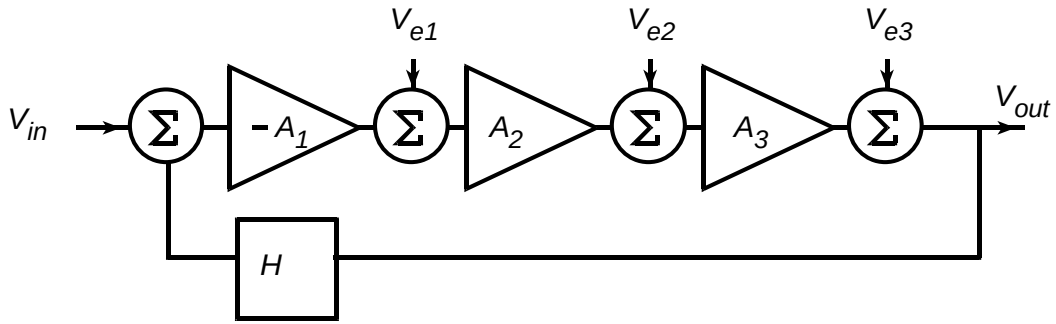
$$V_{out} = A_{CL}V_{in} + (A_{CL}/A_1)V_{e1} + (A_{CL}/A_1A_2)V_{e2} + (A_{CL}/A_1A_2A_3)V_{e3}$$

Distortionof stagesnear the output are stronglyreduced,

Distortions of stagesnear the input are not stronglyreduced

# Background: magnitude of local distortion generation






$$V_{out} = A_{CL}V_{in} + (A_{CL}/A_1)V_{e1} + (A_{CL}/A_1A_2)V_{e2} + (A_{CL}/A_1A_2A_3)V_{e3}$$

$$V_{e1} = (V_{out}/A_{v2}A_{v3})^3 / V^2_{oip3,1} \qquad V_{e2} = (V_{out}/A_{v3})^3 / V^2_{oip3,2} \qquad V_{e3} = V^3_{out} / V^2_{oip3,3}$$

The locally-generated distortion depends on the local signal level & the stage IP3

These locally-generated distortion signals are then suppressed
---in proportion to the amount of gain between that point and the input

This is a simplified discussion, where a more complete analysis is included in the manuscript
--- must consider voltages and currents,
--- must consider frequency-dependent impedances

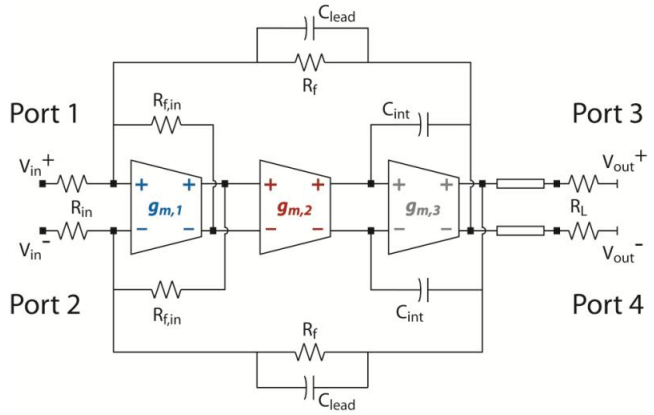
# Challenges for low distortion, stable 50GHz op-amps



- Technology: 0.5um InP HBT, 350GHz $f_t$ and $f_{max}$, ~5V breakdown
- No InP HBT complimentary devices available
  - No active loads for high stage gain
    - RF choke inductor needed, effective at 2GHz → $Z = R + j\omega L$
  - Positive level-shifting not available
    - Bias currents and voltages carefully selected for low local-stage IM3
    - Voltage difference across the feedback network must be considered
- Non-linear capacitive loading of the HBT junction capacitances on the feedback network can introduce distortion that is not suppressed by strong feedback
  - Current summing avoids device $C_{je}$, $C_{cb}$ loading of the feedback network
- Amplifiers must be stable across its bandwidth for varying source impedance
- Low noise figure – small input padding resistance $R_{in}$ = 5-Ohm used
- Feedback network must be electrically short at 50GHz
- Low-power budget $P_{DC} \leq 1.0W$

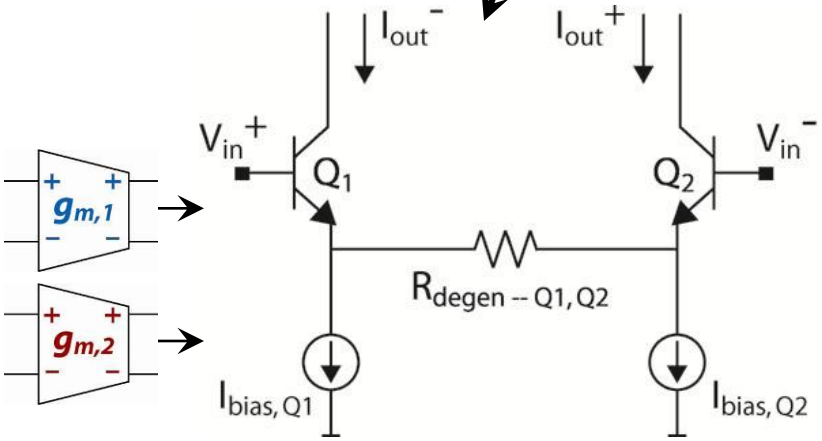
# Differential current-mode building blocks

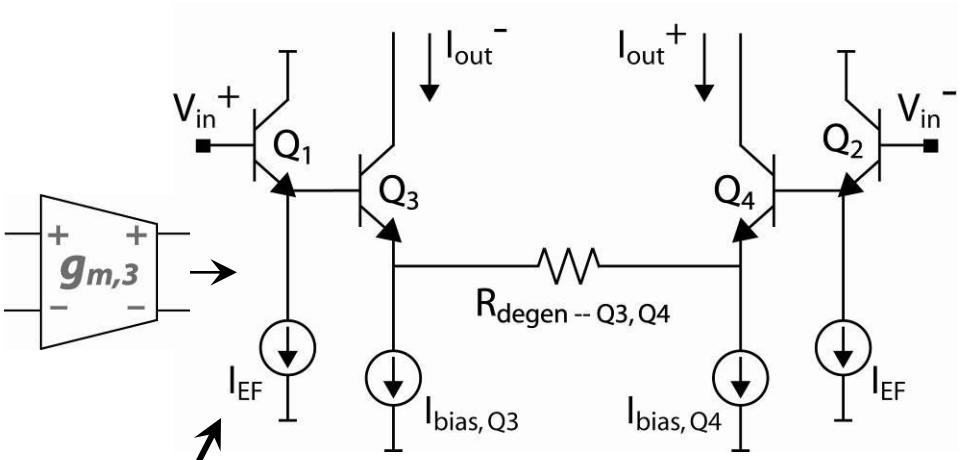





**Simple-Miller example – basic differential amplifier building blocks**
**-- simple differential pair ($g_{m,1}$ $g_{m,2}$) and**
**Darlington differential pair amplification ($g_{m,3}$)**

**Simple differential pair, split current biasing**



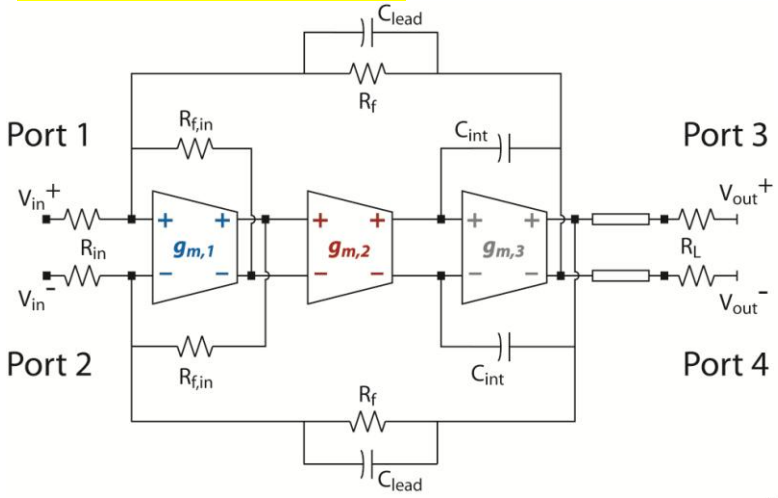




**Darlington differential pair used for the output stage**

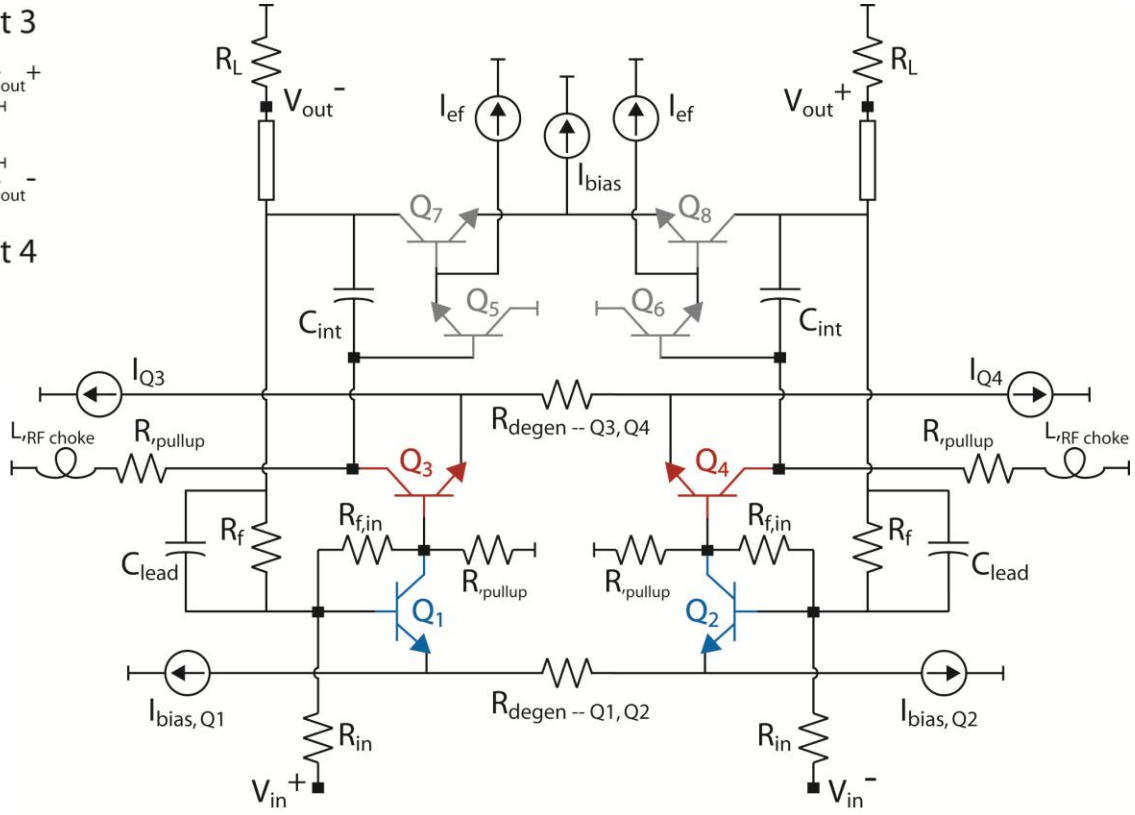
# Differential Op-amp floorplan



**Simple-Miller schematic**




**Detailed Simple-Miller floorplan**

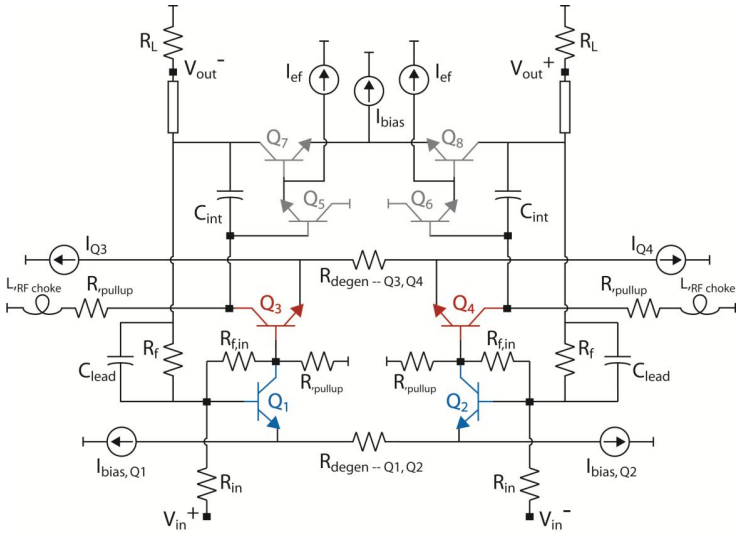



**Because the passives are large, all biasing components and loading elements are pulled away from the forward signal path and feedback network**

**Only transistors and horizontal interconnects set the length of the feedback path**

# Equivalent half circuit – bias conditions

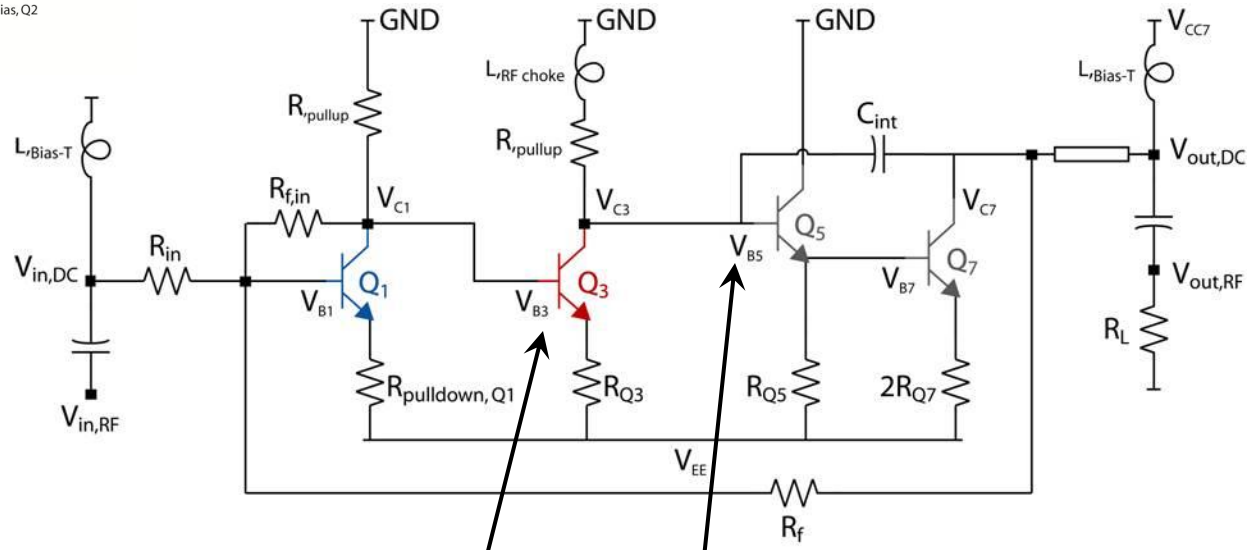





Circuit floor plan

HBT base-collector voltage is $V_{cb}$ > 300mV to keep small distortion due to modulation of the capacitance $C_{cb}$

Equivalent op-amp half-circuit

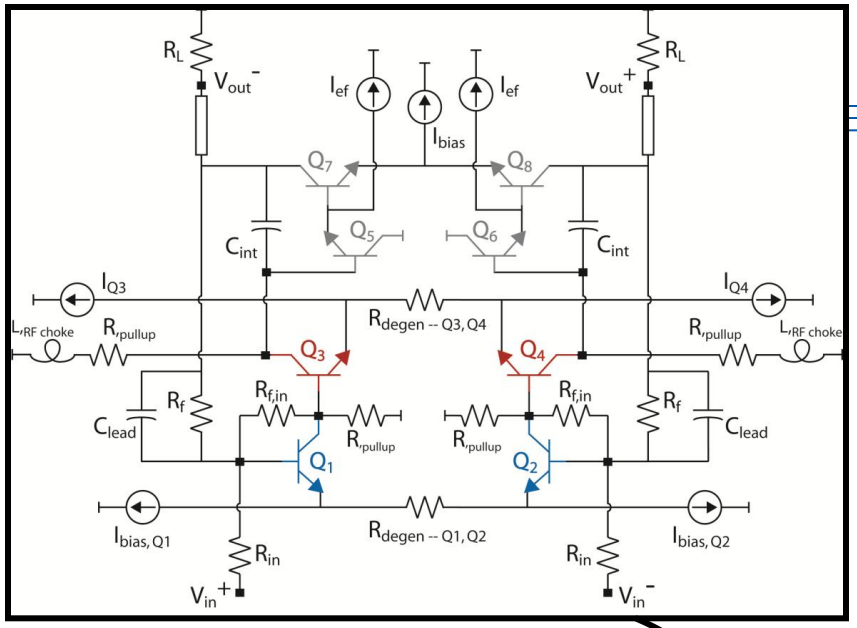



Self-biasing voltages are set by previous stage current and load resistance

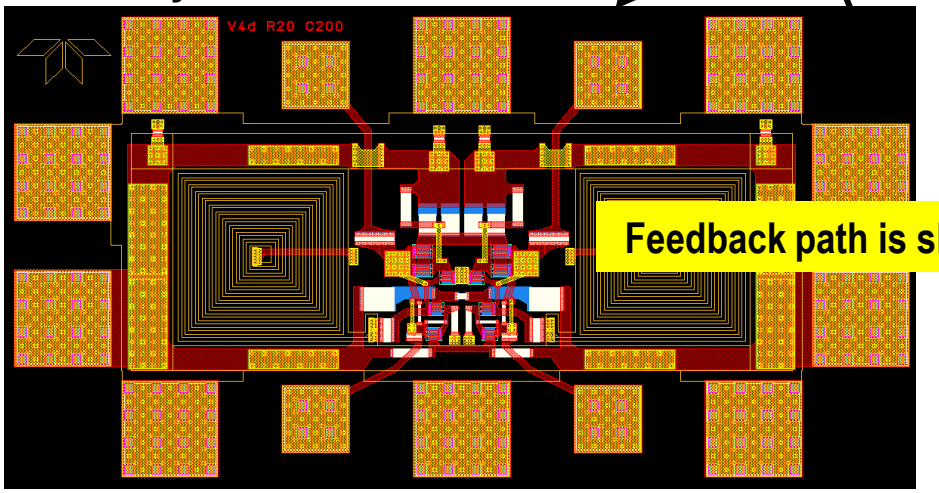
# Layout and IC micrograph



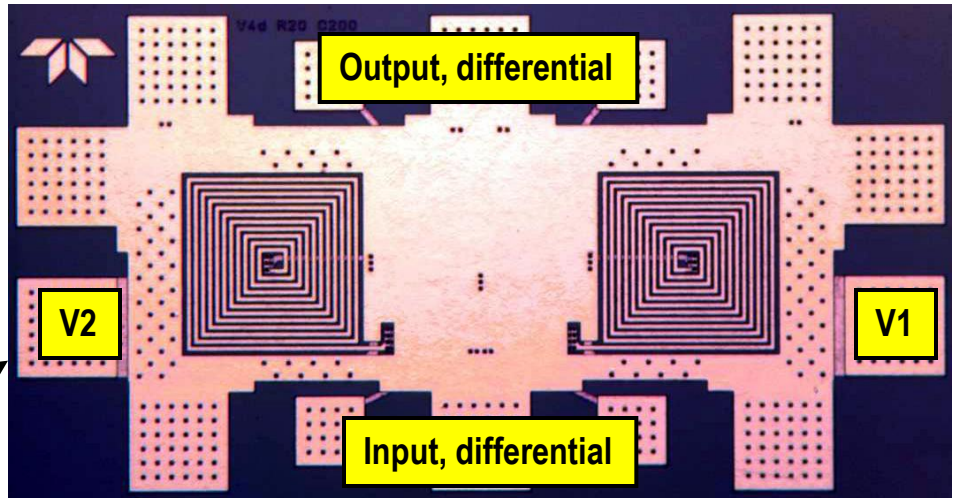
## Circuit floorplan, Simple-Miller op-amp




## Circuit layout




Dimensions: 0.92 x 0.46-mm$^2$




IC micrograph of TSC fabricated op-amp

**Feedback path is short, only ~ 65μm**

The electrical length of the feedback path is only…
- 3.5 degrees (λ/100) at 25GHz operation
- 14 degrees (λ/25) at 100GHz operation

# Amplifier measurements



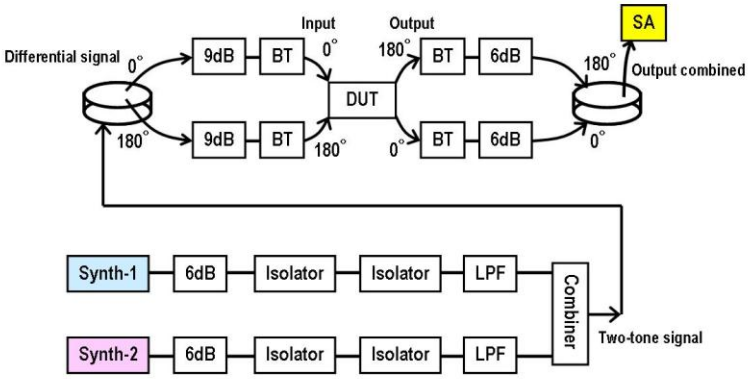
## VNA measurements:

- 4-port S-parameters, 100MHz-50GHz (Agilent PNA-X)
- Discrete measurements of each port
- Differential amplifier performance computed
  - True-mode differential stimulus to be performed

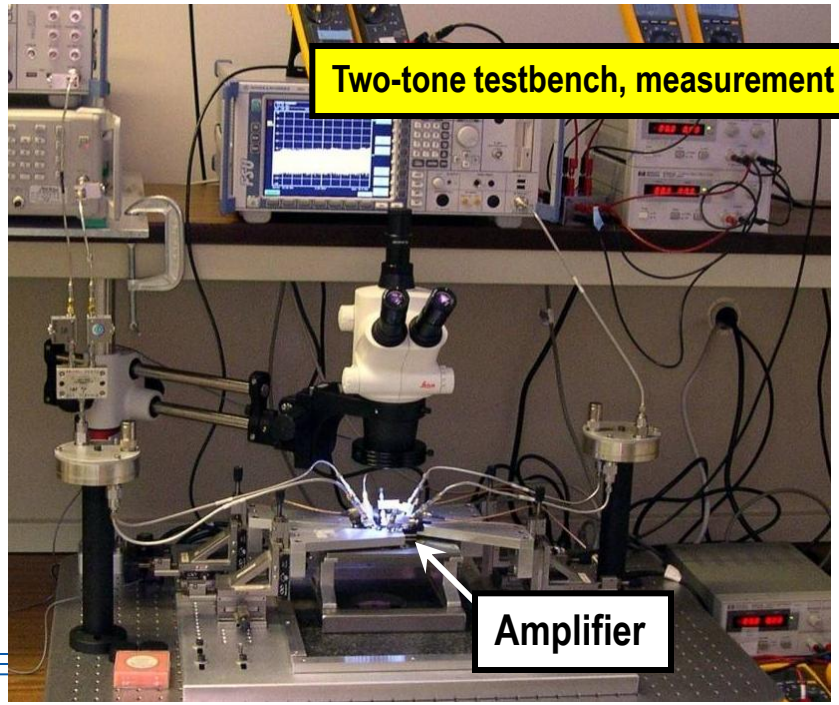
## Two-tone and IM3 distortion measurements:

- Agilent 4440A spectrum analyzer
- Use of attenuators, isolators, and low-pass filters are required for very low VSWR throughout the system
- Residual overall system distortion is 56dBm
  - From thru-lines probed on cal substrate

**Two-tone testbench, schematic**



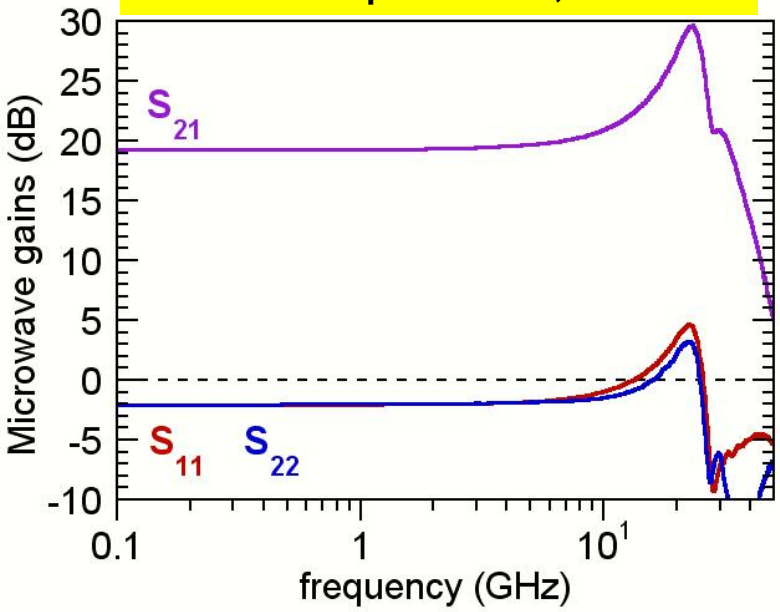

**Two-tone testbench, measurement**



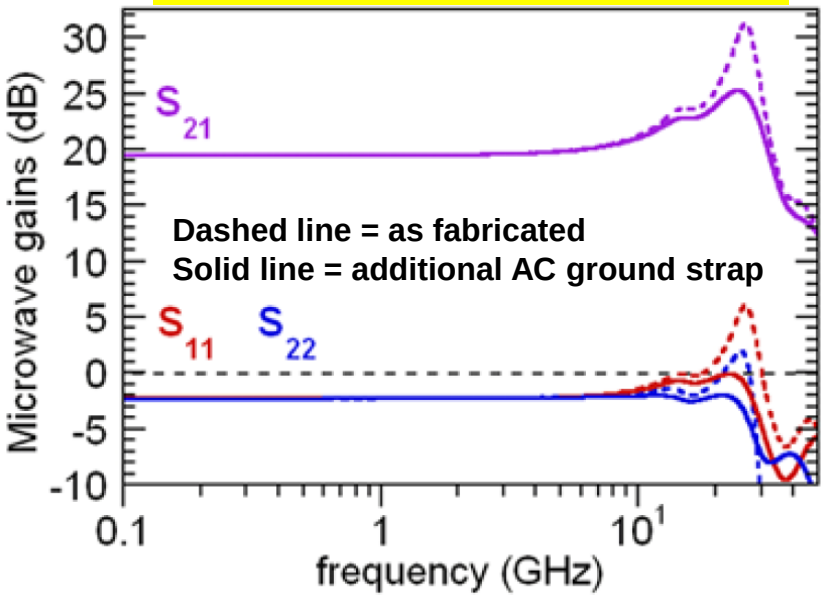
# Amplifier measurement: Differential S-parameters



**Differential S-parameters, measured**




**Differential S-parameters, simulated**

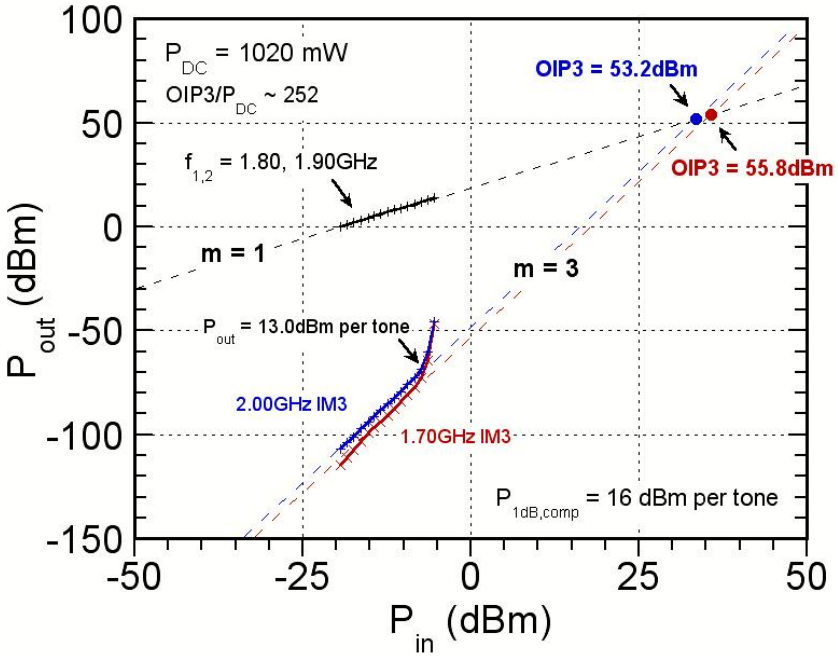



**$S_{21,\ mid\text{-}band}$ = 19.2dB**
**Bandwidth, 3dB > 30GHz**
**Noise figure = 5.5dB**
**$P_{DC}$ = 1020mW**

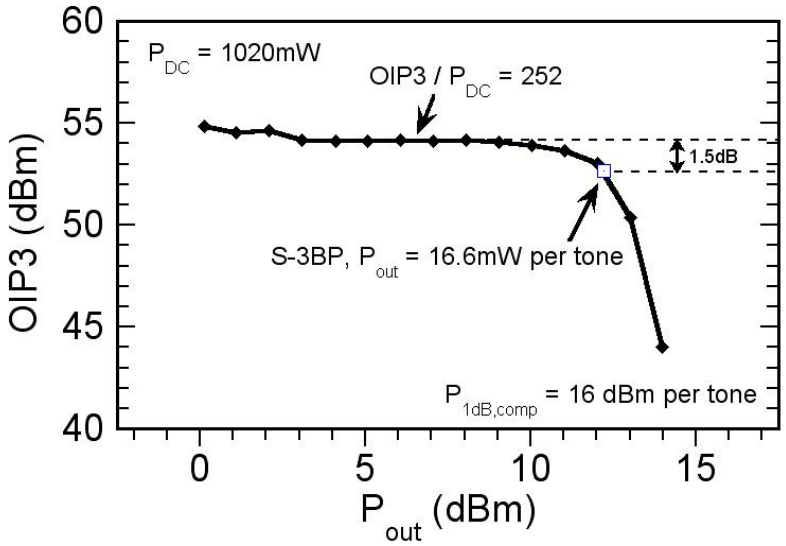
- Inadequate interconnect at the emitter of the output stage differential pair causes excessive phase accumulation at higher frequency
  - This was not fully modeled during design
  - Re-evaluation by simulation shows the peaking observed in measurement
- Additional emitter ground straps (w/ no other changes) greatly improves phase margin and the gain peaking is greatly reduced

# Amplifier measurement: Two-tone power and IM3



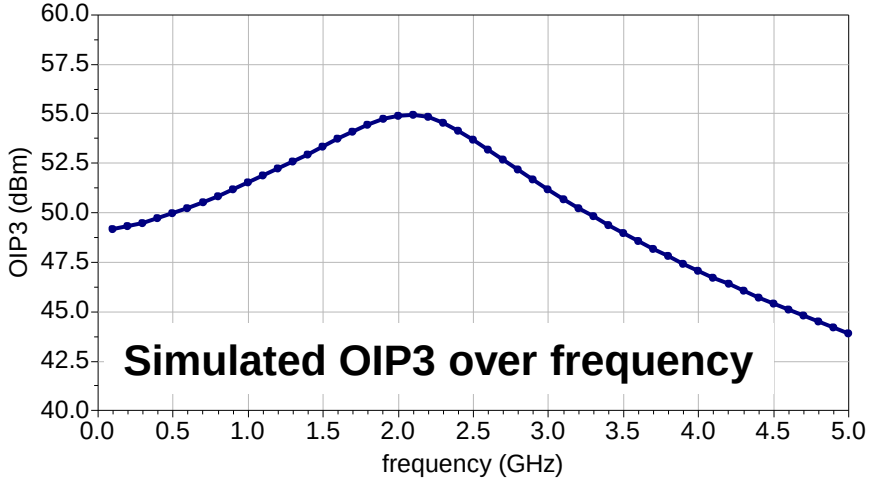



**$P_{out}$, $P_{IM3}$ versus $P_{in}$**




**Variation of OIP3 (2GHz) with $P_{out}$**

**OIP3, 2GHz = 54.1dBm**
**OIP3 to $P_{DC}$ ratio = 252**
**S-3BP at $P_{out}$ = 16.6mW/tone**
**OIP2 ($f_1$+$f_2$) > 90dBm**




**Simulated OIP3 over frequency**

# Summary



- Shunt-feedback amplifiers demonstrating high OIP3 have been presented
  - OIP3 = 54.1dBm at 2GHz, Slope-3 breakpoint $P_{out}$ = 16.6mW/tone
  - 19.2dB $S_{21}$ gain
  - 5.5dB noise figure
  - $P_{DC}$ = 1020mW
  - Record OIP3/$P_{DC}$ ratio = 252

- Future work requires examining…
  - Current source biasing to decrease common-mode gain
  - Improved layout for higher loop bandwidth, higher loop gain at low-GHz
  - Single DC source biasing, remove bias sequencing
  - Improve input and output VSWR

This work has been sponsored by the DARPA FLARE program
Dr. Sanjay Raman, Program Manager
Dr. Richard Eden, Program oversight