Performance enhancement of GaAs UTB pFETs by

strain, orientation and body thickness engineering Abhijeet Paul^{1*}, Saumitra Mehrotra^{1*}, Gerhard Klimeck¹ and Mark Rodwell²

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III-V semiconductors can provide a viable option for continuous scaling of future CMOS technology [1-3]. We report a significant enhancement in the ON-current (I_{ON}) of ultra-thin body (UTB) GaAs intrinsic channel p-MOSFETs using biaxial compressive strain. Our theoretical investigation shows that valence bands (VB) become hyperbolic under compressive strain in GaAs rendering effective mass approximation (EMA) invalid. The ballistic I_{ON} ($\sim Q_{inv}$ (hole density) x V_{inj} (injection velocity)) is governed mainly by the asymptotic group velocity ($V_{grp} \sim \alpha.V_{inj}$) of the hyperbolic VBs, These bands can be engineered using GaAs body thickness (T_{ch}) scaling, compressive strain value and wafer orientation. V_{inj} is primarily controlled by strain and T_{ch} whereas, Q_{inv} is governed mainly by the gate electrostatics, thus providing two separate design parameters to control I_{ON} . Isotropic strain enhances V_{inj} which gives a maximum improvement in I_{ON} of ~ 23 -40% for [100]/(100) and [110]/(111) pMOSFETs for 5 nm body thickness at 4% compressive biaxial strain. Scaling body thickness from 5nm to 2nm improves I_{ON} by $\sim 2X$ for all the device orientations considered in this study.

The analysis of I_{ON} involves the following steps. VB E(k) is calculated using an atomistic sp3d5s* tight-binding model with spin orbit (SO) coupling [4] under the action of biaxial compressive strain (0 to 4%) for the following [transport]/(wafer) orientations: [100]/(100), [110]/(110) and [110]/(111) (Fig.1a), for T_{ch} varying from 2 nm to 5 nm. DOS and modes (M(E)) are calculated numerically using the VB E(k) which are eventually used to calculate the inversion hole density (Q_{inv}) and drain current (I_{ds}), respectively. V_{inj} is calculated using I_{ds}/Q_{inv} . Gate electrostatics is accounted for by considering a gate oxide of thickness T_{ox} . Quantum hole charge density correction (T_{inv}) is obtained using SCHRED [5]. The entire procedure and the equation to calculate gate over drive (V_{gt}) is similar to the method in [3] (Fig. 1).

With III-V n-FETs, the density of states (DOS) is low, the bands are approximately parabolic, and electron velocity varies as the square root of kinetic energy; the channel effective mass, m^* , is selected for highest drive current by balancing its opposing effects on charge density and on injection velocity [2-3]. In marked contrast, over the range of Fermi energies expected in p-FET operation, the computed VB E (k) fits closely to a hyperboloid, with carrier group velocity approaching an asymptotic maximum with increased kinetic energy. The calculated VB E(k) for a 4nm thick GaAs UTB under 4% strain fits very well to hyperbolic bands (Fig 2a), and the injection velocity shows little variation with energy (Fig. 2b). Further, because the state density is high, highest current is obtained by designing the channel for highest group velocity, and by selecting a thin body and dielectric for high charge density. Approximating the hyperbolic bands as $E(k) = \hbar v_0 + k + 1$, the injection velocity is constant, $v_{inj} = (2/\pi)v_0$ and the sheet hole density, $v_0 = k_f^2/\pi = \pi^{-1}(E_f/\hbar v_0)^2$ is large and varies as the inverse square of the asymptotic velocity (v₀); strained VB in GaAs can be well represented by hyperbolic bands where the velocity, rather than the effective mass, is constant with energy.

The valence bands are highly anisotropic and respond very differently to strain applied in different directions. Figure 3 shows the VB E(k) for 4nm thick GaAs UTB channel for -4%, -1% and 0% biaxial strain. Strain causes an isotropic compression of VB E(k) for [100]/(100) (Fig.3 a-c) and [110]/(111) (Fig. 3 g-i) channels. However, for [110]/(110) channel the strain causes anisotropic compression in VB E(k) (Fig.3 d-f).

The calculated I_{ON} , under strain at V_{gt} =0.3V and t_{ox} = 0.5nm (low-operating-power devices [1]) are shown for various GaAs body thickness. The I_{ON} improves ~2X for all the orientations with body scaling from 5nm to 2nm under 0% strain (Fig.4 a-c). The anisotropic strain effect on VB E(k) reveals itself in the computed I_{ON} vs. strain. [100]/(100) and [110]/(111) pFETs improve monotonically with strain (Fig.4 a&c) showing a maximum improvement of ~38% and 23%, respectively for 5nm thick GaAs channel under -4% biaxial strain. This is an outcome of the compression of the VB E(k) under strain which increases the V_{inj} (Fig.3). The highest I_{ON} is obtained in the [110]/(110) orientation, though strain has no benefit (Fig.4 b).

A crucial aspect for designing III-V pFETs is the action of strain and gate electrostatics on the drive current. As an example the V_{inj} , Q_{inv} and I_{ON} for [100]/(100) pFETs with T_{ch} for two different V_{gt} are shown in Fig.5. An important observation is that V_{inj} is primarily enhanced by strain (Fig. 5a) whereas Q_{inv} is dominated by the gate electrostatics. This behavior is observed in all the orientations. The independent control of Q_{inv} and V_{inj} can essentially allow us to design III-V pFETs with required I_{ON} . Thus, a proper choice of wafer/transport orientation and strain, providing a high hole group velocity, along with an optimal gate oxide thickness can lead to better III-V pFETs for the future CMOS technology.

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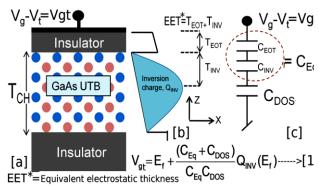


Figure 1: Schematic of an atomic GaAs UTB pFET channel alon with inversion hole density. T_{inv} is calculated using SCHRED [5]. Gate electrostatics is taken into consideration using Eq. (1).

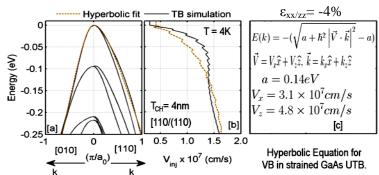


Figure 2: (a) TB calculated (grey) and hyperbolic fitted (brown) E(k) along kx (at kz=0) and kz (at kx=0). (b) Comparison of injection velocity obtained from hyperbolic E(k) to the simulated value at T=4K. Constant Vinj vs. E_f is a signature of hyperbolic band. (c) Hyperbolic E(k) expression and the parameters values for the fitted TB E(k).

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<u>x</u> 10⁶

[100]/(100)

T=300K

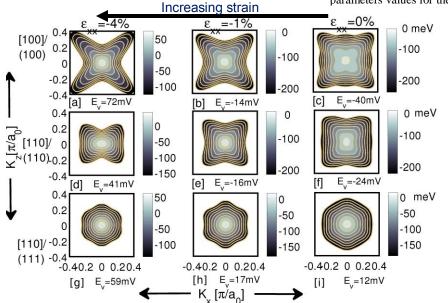


Figure 3: 2D E(k) of the highest VB in the 4nm thick strained GaAs UTB for (a-c) [100]/(100) **high V**_{grp} (d-f) [110]/(110) **low V**_{grp} and (g-i) [110]/(111). **high V**_{grp} Strain value is -4%, -1% and 0% for left, middle and right column, respectively. The VB max values (Ev) are shown Energy range is from Ev to 8KT below Ev. Kx is the transport direction.

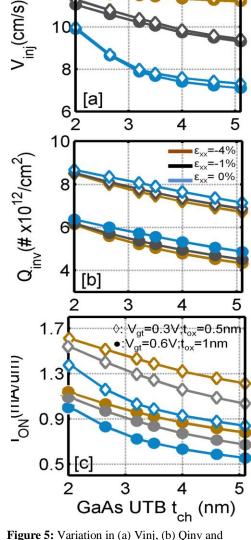


Figure 5: Variation in (a) Vinj, (b) Qinv and (c) I_{ON} with GaAs body thickness for 3 strain values (-4%, -1% and 0%) and two gate overdrive biases (Vgt). Filled (open) symbol represents Vgt =0.6V (0.3V) for Tox = 1nm (0.5nm). **Inversion charge is governed by the gate electrostatics while injection velocity is governed mainly by strain.**

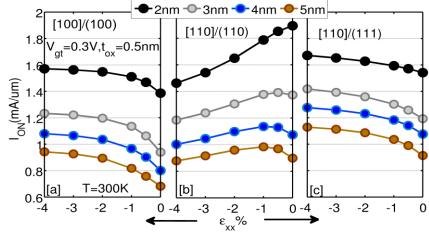


Figure 4: $I_{\rm ON}$ variation with strain for (a) [100]/(100), (b) [110]/(110) and (c) [110]/(111) oriented GaAs p-FETs for 4 different body thickness. [100]/(100) and [110]/(111) devices show improvement with strain and body thickness scaling, whereas [110]/(110) degrades with strain. In [100]/(100) $I_{\rm ON}$ improves a maximum of 38% (5nm,-4%) with strain and ~2X with body scaling. [110]/(110) $I_{\rm ON}$ degrades by 29% (2nm,-4%) but improves by ~2X with body scaling. In [110]/(111) $I_{\rm ON}$ improves a maximum of 23%