A 300 GHz PLL in an InP HBT Technology

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***Abstract* — We present a 300 GHz fundamental PLL, based on a 300 GHz VCO, 2:1 dynamic frequency divider, fifth-order sub-harmonic phase detector, and active loop filter, fabricated in an InP HBT technology. The PLL achieves locking from 300.76 to 301.12 GHz, with -23 dBm of output power and -78 dBc/Hz of phase noise at a 100 KHz offset, while consuming 301.6 mW. The PLL occupies 0.84 mm^2 including pads. This work represents the highest frequency PLL reported thus far, 2× to 3× faster than previously reported PLLs.**

***Index Terms* — Phase-locked loops, hetero-junction bipolar transistors, dynamic frequency dividers, voltage controlled oscillators.**

I. Introduction

Sub-millimeter-wave and terahertz (THz) frequency bands covering 300 GHz to 3 THz have applications in security/medical imaging systems, radar, chemical/bio sensors, and high-rate data communications. Phase-locked loop (PLL) circuits provide a coherent local oscillator (LO) signals for frequency up/down-conversion, and are a critical building block for high-performance THz systems.

Millimeter-wave PLLs have been demonstrated up to 164 GHz [1-5] in SiGe or nano-scale CMOS technologies. This paper presents a 300 GHz PLL IC using an InP HBT technology, where the use of a fundamental VCO and a dynamic frequency divider enables fundamental PLL operation.

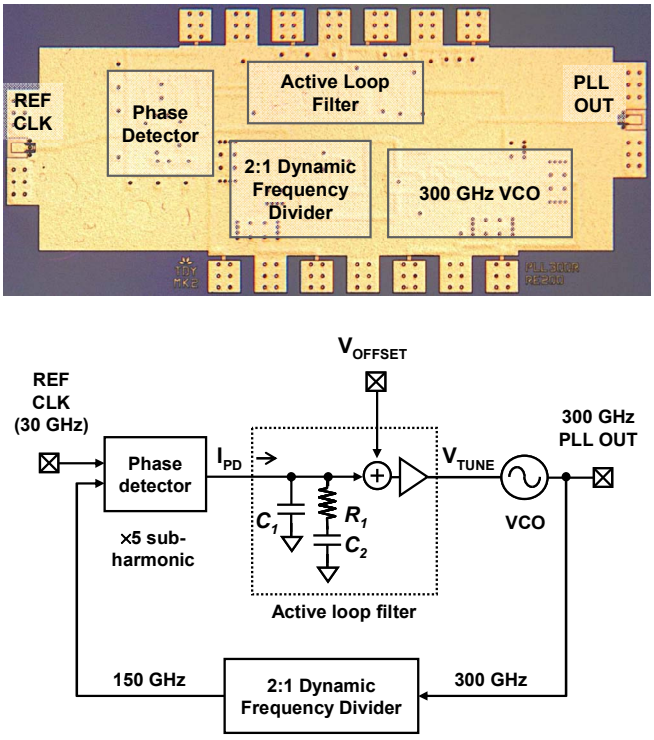

Fig. 1. 300 GHz InP HBT PLL: chip photograph (top) and block diagram (bottom). Chip size: 1,380×610 µm^2.

II. InP HBT Technology

InP double heterojunction bipolar transistors (DHBTs) offer high transistor bandwidth with high voltage handling due to the use of a wide bandgap InP collector. In this work, circuits were fabricated on 4-inch semi-insulating InP substrates with device layers grown by molecular beam epitaxy. The epitaxy utilizes a 30 nm carbon-doped base layer and a 150 nm N-InP collector region. The emitter contact is patterned using electron-beam lithography and formed using an Au-based electroplating process. In this work, the nominal emitter junction width was 0.25 µm. A thin (< 100 nm) emitter semiconductor stack minimizes undercut during the self-aligned emitter mesa etch. Dielectric sidewall spacers are formed that passivate the base-emitter junction and permit the formation of a self-aligned base contact. After base-contact deposition, the remaining HBT process flow follows that of a standard mesa-HBT process. The transistors are passivated with a spin-on-dielectric (Benzocyclobutene, BCB), and a planarization etch is used to expose the emitter post. Device vias are opened to the remaining HBT contacts and first-level interconnects are formed using electroplated gold.

The HBT IC process includes thin-film resistors (50 Ohm/sq), MIM capacitors, and 3-levels of interconnect (M1-M3). A 7 µm thick BCB layer is used between M2 and M3 to facilitate the formation of low-loss thin-film microstrip lines.

Extrinsic emitter resistance and extrinsic base-collector capacitance was reduced by a factor of ~2 compared to the previous generation of the technology, resulting in higher device bandwidths. S-parameter measurements of transistors were performed from 1-110 GHz and RF figures-of-merit

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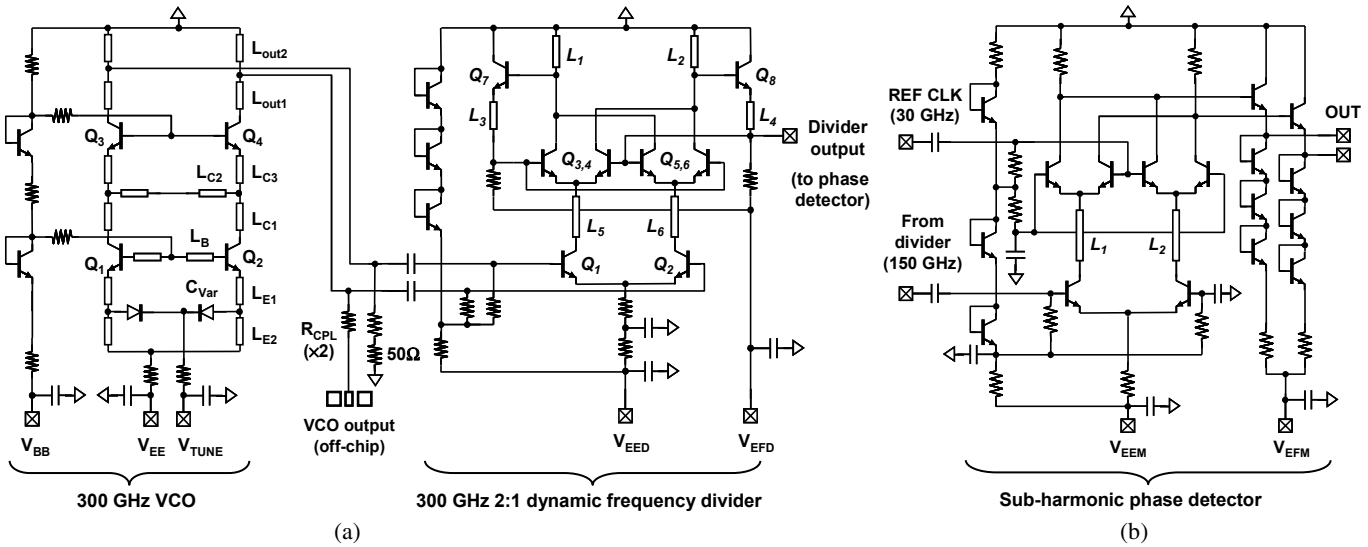

Fig. 2. Simplified schematic of the (a) VCO-divider chain and (b) phase detector.

were extracted from these measurements. A 4×0.25 μm^2 HBT demonstrated an extrapolated current gain cutoff frequency (f_T) of > 400 GHz and an extrapolated maximum frequency of oscillation (f_{max}) of > 800 GHz, at I_C = 10 mA and V_{CE} = 1.8 V. Transistors have demonstrated common-emitter breakdown voltages (BV_{CEO}) of > 4V. Large-signal Agilent HBT models have been extracted. Compared to standard silicon BJT model (i.e. Gummel-Poon or VBIC), the Agilent model is better suited to capture some characteristics that are unique to III-V DHBTs such as collector current blocking and collector velocity modulation.

III. PLL Design

The PLL consists of a 300 GHz VCO, 2:1 dynamic frequency divider, sub-harmonic phase detector, and active loop filter, as shown in Fig.1.

A. VCO

In this work, a series-tuned differential VCO is used [6], as shown in Fig.2 (a). Q_1-Q_2 form an oscillator core, and a common-base amplifier (Q_3-Q_4) provides power gain and isolation from load perturbation, while re-using the same bias current. C_{VAR} is a single finger base-collector (*B*-*C*) junction at reverse bias with expected *Q*~10 at 300 GHz. Differential topology makes oscillator operation insensitive to common-mode impedances, e.g. bias lines and grounding via inductance, thus tolerant to modeling uncertainties and errors. The VCO provides -6 dBm of single-ended power, and tunes across > 6 GHz, while consuming 95 mW. The VCO output is tapped by a simple 18 dB resistive coupler (R_{CPL}) for off-chip spectrum measurement.

B. Dynamic Frequency Divider

Due to the bandwidth limitation of static frequency dividers, dynamic frequency dividers have been used for millimeter-wave PLLs up to 100 GHz, e.g. regenerative ("Miller") frequency dividers [1-2] or injection-locked frequency dividers [3][5]. In this work, a regenerative 2:1 dynamic frequency divider is employed [7], as shown in Fig.2 (a). The use of inductive loading (L_1-L_2) enables higher frequency operation than is possible with traditional resistive or transimpedance-stage loading. According to simulation, the divider operates from 270 GHz to 330 GHz, with -25 to -15 dBm of output power, while consuming 91 mW.

C. Phase Detector

In order to perform phase comparison at a reasonably low frequency, a 5th-order (N = 5) sub-harmonic phase detector is used in this work, in favor of its simpler construction and lower power consumption compared to a chain of static frequency dividers. Fig. 2 (b) shows schematic of the sub-harmonic phase detector based on a double-balanced mixer, where the 30 GHz reference clock and 150 GHz divider output is applied to the upper and lower differential pairs, respectively. Transmission lines L_1 and L_3 improve impedance matching between the upper and lower differential pairs at 150 GHz, thus enhancing phase detector gain. Simulation shows that the phase detector provides useful detection gain up to N = 5 sub-harmonic operation with -20 dBm of RF power at 150 GHz. Simulated detector gain is K_{PD} = 35, 18, 7, and 1.6 mV/2π, for N = 3, 5, 7, and 9, respectively. Detector operation at N > 5 may suffer from increased sensitivity to detector offset voltages and may degrade PLL phase noise.

C. Active Loop Filter

A conventional lag-lead filter is used (Fig.1), which results in a 2nd-order PLL. The loop bandwidth is 150 MHz,

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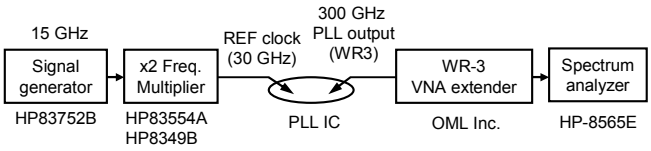

Fig. 3. PLL test setup.

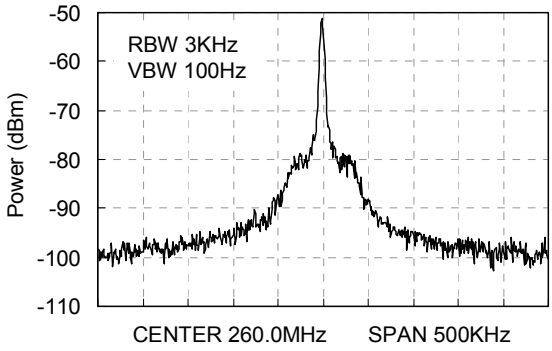

Fig. 4. Measured PLL output spectrum after down-conversion by a WR-3 VNA extender.

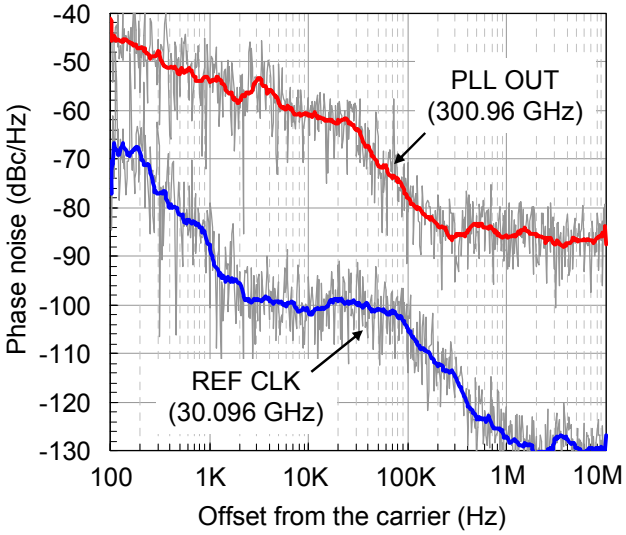

Fig. 5. Measured phase noise of the reference clock (30.096 GHz) and down-converted PLL output (300.96 GHz).

determined from the intersection of VCO phase noise and frequency-multiplied reference clock (30 GHz) phase noise skirts. This approach results a low phase noise PLL, since the PLL output phase noise will follow the lower of the two. The loop is designed with a sufficient phase margin to ensure stability in the presence of process variations. Accounting for extra phase shifts from higher-order poles, which include interconnect delays and *RC* time-constant from varactor bias circuit, the loop phase margin is 80 deg, with approximately 10 deg of contribution from extra phase shifts.

Chip photograph of the PLL IC is shown in Fig. 1. All the circuits on the PLL IC are implemented using inverted microstrip lines to utilize a continuous ground plane on a top metal layer.

IV. Measurement Results

The fabricated PLL IC was characterized on-wafer using the test setup in Fig. 3. The 300 GHz PLL output was down-converted by a WR3 VNA extender (OML Inc.), and the extender's IF output was measured by a spectrum analyzer.

Typical IF spectrum is shown in Fig. 4. The measured PLL locking range was from 300.76 GHz to 301.12 GHz. Phase noise of the PLL at 300.96 GHz was measured to be -45dBc, -54 dBc, and -78 dBc at 100 Hz, 1 KHz, and 100 KHz of offset frequencies, respectively (Fig. 5). The measured output power was -23 dBm after correcting for the down-converter loss. Beyond 300 KHz of offset frequencies, phase noise measurement is limited by IF noise floor of the WR3 VNA extender. Difference between the reference clock and PLL phase noise is greater than the frequency multiplication factor, i.e. $f_{VCO}/f_{REF} = 20 \log_{10} 10 = 20$ dB, between 1 KHz and 50 KHz of offset frequencies, suggesting noise enhancement from PLL building blocks. The PLL consumes 301.6 mW of dc power. Measurement from separate breakout circuits for the VCO-divider chain shows that the VCO has 6 GHz of tuning range, and that the dynamic frequency divider has > 40 GHz of operating bandwidth, all centered at 300 GHz. Table. 1 compares recently published mm-wave PLL ICs.

V. Conclusion

A 300 GHz single-chip PLL in InP HBT technology is presented. To the best of authors' knowledge, this work represents the highest frequency PLL, operating at 2× to 3× higher frequencies than previous fundamental or harmonic-based PLLs.

Acknowledgement

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Table 1. Comparison of recently reported millimeter-wave PLLs

	This work	[1]	[2]	[3]	[4]	[5]
Frequency [GHz]	**300.76–301.12**	162–164* 86–92 81–82	91.8–101* 45.9–50.5	95.1–96.5	79.4	73.4–73.72
Technology	**InP HBT**	0.13µm BiCMOS	0.13µm CMOS	65nm CMOS	SiGe	90nm CMOS
Divide ratio [f_{VCO}/f_{REF}]	**10**	16,32, 64,128	512	256	64	32
Phase noise @100KHz [dBc/Hz]	**-78**	-78.9 @163GHz -93.8 @90GHz	-63.5 (50KHz offset)	-75.2 to -75.86 (1MHz offset)	-81	-88
Supply voltage [V]	**-4.3, -5.0**	1.8, 2.5, 3.3	1.5, 0.8	1.2, 1.3	5.5	1.45
P_{OUT} [dBm]	**-23**	-25 @163GHz -3 @90GHz	-10 @50GHz -31 to -22 @100GHz	-	-	-
P_{DC} [mW]	**301.6**	1,150 to 1,250	57	43.7	-	88#
Chip area [mm^2]	**1.38×0.61**	1.1×1.7	1.16× 0.75	1× 0.7	-	1×0.8

* Second-order harmonic # Excluding output buffers

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