Influence of gate metallization processes on the electrical characteristics of high-k/$In_{0.53}Ga_{0.47}As$ interfaces

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The influence of different gate metal deposition processes on the electrical characteristics of dielectric/III-V interfaces is investigated. Al_2O_3 and HfO_2 dielectrics are grown on $In_{0.53}Ga_{0.47}As$ channels and top metal electrodes are deposited by either thermal evaporation or electron beam deposition. It is shown that metal-oxide-semiconductor capacitors with electron beam evaporated electrodes exhibit substantially larger midgap interface trap densities than those with thermally evaporated electrodes. The damage caused by electron beam metallization can be mitigated by subsequent, long anneals in forming gas. *© 2011 American Vacuum Society.*
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I. INTRODUCTION

The development of metal-oxide-semiconductor field effect transistors with high-mobility, compound (III-V) semiconductor channels and high-permittivity (k) gate dielectrics critically depends on further reducing the typically very high density of interface traps (D_{it}) at the dielectric/semiconductor interface.[1,2] Although numerous studies have investigated the influence of III-V surface preparation and high-k deposition parameters on the electrical quality of these interfaces, the nature of the interface defects, their spatial location, and energy distribution in the semiconductor band gap remain poorly understood. Fewer studies have focused on the role of post-high-k-deposition device processing steps in determining the interface quality. For example, energetic species (ions, electrons, and x-rays) generated during gate metal deposition may cause significant damage to the III-V semiconductor far below the surface.[3] In this context, several recent studies have reported significant improvements of the interface electrical characteristics after postmetallization anneals in forming gas, which contains a few percent of hydrogen.[4–7] Among the mechanisms that have been suggested to cause the reduction in D_{it} are hydrogen passivation of border traps in the oxide[4] and reduction of native oxides of the III-V semiconductor.[8] A third possibility, namely, that the forming gas anneals serve to recover the damage from gate metal deposition, has not yet been considered. In this article, we investigate the influence of two different gate metal deposition processes, electron beam and thermal evaporation, on the D_{it} of high-k/$In_{0.53}Ga_{0.47}As$ interfaces. We show that gate metallization can cause substantial increases in the D_{it} and that the main effect of postmetallization forming gas treatments is to anneal out this damage.

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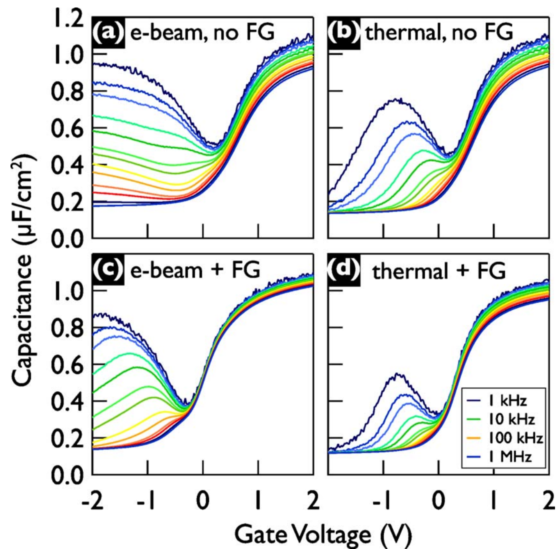

FIG. 1. (Color online) Capacitance-voltage curves measured as a function of frequency (from 1 kHz to 1 MHz) at room temperature for MOSCAPs with Al_2O_3 dielectrics grown by ALD and (a) Ni top electrode deposited by electron beam evaporation, (b) Ni top electrode deposited by thermal evaporation, and [(c)–(d)] same samples as in (a) and (b) after forming gas annealing.

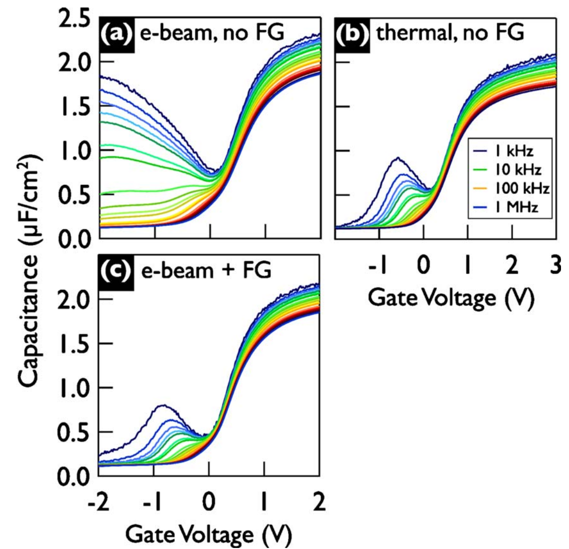

FIG. 2. (Color online) Capacitance-voltage curves measured as a function of frequency (from 1 kHz to 1 MHz) at room temperature for MOSCAPs with HfO_2 dielectrics and (a) Pt electrode deposited by electron beam evaporation, (b) Ni electrode deposited by thermal evaporation, and (c) same sample as in (a) after forming gas annealing.

II. EXPERIMENT

High-*k* dielectrics were deposited on 300 nm thick n-$In_{0.53}Ga_{0.47}As$ layers (Si: 1×10^{17} cm^{-3}) grown by molecular beam epitaxy on (001) n^+-InP. The deposition process for the HfO_2 dielectric, which was alloyed with a few percent of Al, has been described elsewhere.[9,10] Al_2O_3 was deposited by atomic layer deposition (ALD) after cleaning the wafer in a de-ionized water:HCl solution (1:10) for 20 s, followed by 45 cycles of sequential trimethylaluminum (TMA) and H_2O pulses at 300 °C. Both dielectrics were about 5 nm thick. Metal-oxide-semiconductor capacitor (MOSCAP) structures were fabricated with either Ni or Pt top electrodes. Pt electrodes were deposited by electron beam evaporation, whereas for the Ni electrodes either electron beam or thermal evaporation were used. In all cases, the top electrodes were about 50 nm thick and deposition was through a shadow mask. Back contacts were Ti (20 nm)/Pt (20 nm)/Au (250 nm) or Cr (10 nm)/Au(100 nm). For selected samples, a postmetal deposition anneal was carried out at 400 °C for 50 min in forming gas (95% of N_2 and 5% of H_2). Frequency-dependent capacitance-voltage (CV) and conductance-voltage (GV) measurements were performed from 1 kHz to 1 MHz at room temperature using an impedance analyzer (Agilent 4294) in the dark. The midgap D_{it} was quantified using conductance maps after series resistance correction, as described in Ref. 2.

III. RESULTS AND DISCUSSION

Figures 1(a) and 1(b) show the CV characteristics of MOSCAPs with Al_2O_3 dielectrics and Ni electrodes at frequencies between 1 kHz and 1 MHz measured without aNY postelectrode deposition anneal. The frequency dispersion in the capacitance at negative bias is due to midgap D_{it} response,[2] which is much more pronounced when the gate metal is deposited by electron beam deposition [Fig. 1(a)] rather than by thermal evaporation [Fig. 1(b)]. A measure of the efficiency of Fermi level response is whether the capacitance reaches the minimum capacitance given by the doping level of the semiconductor, i.e., if the applied bias is sufficient to fully deplete the semiconductor. For the MOSCAPs investigated here, the ideal depletion capacitance is about 0.119 $\mu F/cm^2$.[11] The minimum capacitance values at 1 MHz are 0.174 $\mu F/cm^2$ (electron beam deposited gate) and 0.135 $\mu F/cm^2$ (thermal gate). This indicates that for both MOSCAPs, the Fermi level movement is not quite sufficient to fully deplete the semiconductor and that the MOSCAP with the electron beam deposited gate has a less efficient Fermi level movement, caused by a higher D_{it}. Because of the otherwise identical processing of the MOSCAPs, the results show that electron beam deposition of the gate metal causes a much higher D_{it} than thermal deposition, most likely due to damage to the III-V semiconductor by x-rays and/or secondary electrons. For both MOSCAPs, the electrical characteristics improve after forming gas annealing [Figs. 1(c) and 1(d)]. The frequency dispersion at negative bias decreases, in particular, for the MOSCAP with the thermal electrode [Fig. 1(d)], which now has a depletion capacitance of 0.118 $\mu F/cm^2$, i.e., the ideal value (note that errors in determining the capacitor area correspond to about ±0.007 $\mu F/cm^2$). The depletion capacitance for the MOSCAP with the electron beam deposited electrode is 0.137 $\mu F/cm^2$, which, although reduced, indicates that the forming gas annealing was insufficient to anneal out all the damage. In addition, the frequency dispersion in accumula-

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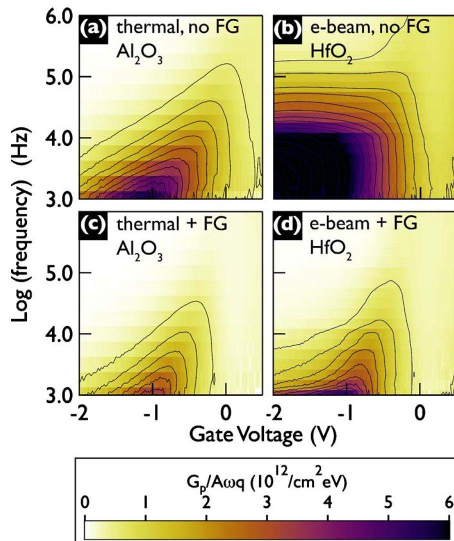

FIG. 3. (Color online) Normalized parallel conductance, $(G_p/\omega)/Aq$, as a function of gate voltage and frequency f for MOSCAPs with (a) the Al_2O_3 dielectric with a Ni electrode deposited by thermal evaporation (b) a HfO_2 dielectric with a Pt electrode deposited by electron beam evaporation. [(c)–(d)] Same samples as in (a) and (b) after forming gas annealing.

tion is also reduced after the forming gas annealing, to 2%–3% per decade from ~5% per decade for both MOSCAPs.

Figure 2 shows a comparison of the frequency-dependent CV of MOSCAPs with HfO_2 gate dielectrics and with Pt electrodes deposited by electron beam deposition and Ni electrodes by thermal evaporation, respectively. These capacitors have a higher accumulation capacitance density because of the higher dielectric constant of HfO_2. MOSCAPs with Ni electrodes have a slightly lower accumulation capacitance density, most likely because of some degree of oxidation of the Ni. Without forming gas annealing, the MOSCAP with the electron beam deposited electrode [Fig. 2(a)] shows much larger midgap D_{it}, as evidenced by a large frequency dispersion at negative biases and a minimum capacitance of 0.122 $\mu F/cm^2$ that is higher than the ideal depletion capacitance. In contrast, the MOSCAP with the thermal gate electrode [Fig. 2(b)] shows only a small "hump" at negative bias and the ideal minimum capacitance (0.119 $\mu F/cm^2$), even without the forming gas anneal. After forming gas annealing, the damage from electron beam metallization is largely recovered, see Fig. 2(c).

For a more quantitative measure of the midgap D_{it}, Fig. 3 shows maps of the normalized parallel conductance, $[(G_p/\omega)/Aq]$, as a function of frequency and gate bias for the MOSCAPs with Al_2O_3 gate dielectrics and thermal electrodes [Figs. 3(a) and 3(c)] and with HfO_2 gate dielectrics and electron beam deposited electrodes [Figs. 3(b) and 3(d)], before and after forming gas annealings. Here, G_p is the parallel conductance, ω is the angular frequency, A is the MOSCAP area, and q is the elemental charge. For the analysis, an oxide capacitance of 1.57 $\mu F/cm^2$ for the Al_2O_3 MOSCAP and 3.1 $\mu F/cm^2$ for the HfO_2 MOSCAP were used, which were determined independently through a thickness series and the Terman method, respectively.[9] The D_{it} at about 0.3 eV below the conduction band edge can be estimated by multiplying $[(G_p/\omega)/Aq]_{max}$ with a factor of 2.5.[2] For the MOSCAP with Al_2O_3 and thermally evaporated electrode, $[(G_p/\omega)/Aq]_{max}$ is 5.7×10^{12} cm^{-2} eV^{-1} which decreases to 3.4×10^{12} cm^{-2} eV^{-1} after the forming gas annealing. A much larger change is detected for the HfO_2 MOSCAP with the electron beam evaporated gate electrode. Before the forming gas annealing, $[(G_p/\omega)/Aq]_{max}$ is 10.8×10^{12} cm^{-2} eV^{-1} and the peak does not move in frequency for gate biases below −1 V. This indicates that the Fermi level is essentially pinned near midgap.[2,12] After the forming gas anneal, $[(G_p/\omega)/Aq]_{max}$ moves efficiently as a function of bias. The highest $[(G_p/\omega)/Aq]_{max}$ value is 5.2×10^{12} cm^{-2} eV^{-1}.

SUMMARY AND CONCLUSIONS

In summary, we have shown that deposition of gate electrodes using electron beam evaporation causes a significant degradation of high-*k*/III-V interfacial electrical characteristics, as exhibited by a large midgap D_{it}. Comparison with MOSCAPs with electrodes deposited by thermal evaporation and processed under otherwise identical conditions demonstrates that the very large midgap D_{it} is indeed caused by the electron beam deposition process and is not intrinsic to the as-deposited high-*k*/III-V interface. The results further demonstrate that the reason for D_{it} reduction by forming gas treatments consists of annealing out of damage in the III-V semiconductor and is not due to the passivation of defects by hydrogen, i.e., as for SiO_2/Si interfaces. This also explains the fairly long annealing times that are required to restore the interface electrical properties. As shown in the literature for III-V quantum wells,[3] even the thermal electrode deposition process is likely to cause some damage. In particular, for MOSCAPs with Al_2O_3 dielectrics and thermally deposited electrodes, reduction in D_{it} was seen after forming gas anneals. Future studies should investigate electrodes deposited by chemical vapor deposition or ALD, which may allow for even lower D_{it}.

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