40Gbit/s coherent optical receiver using a Costas loop

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Abstract: A highly integrated 40Gbit/s coherent optical receiver is reported using a Costas loop as a homodyne optical phase locked loop (OPLL). A photonic IC, an electrical IC, and a hybrid loop filter are characterized, and the feedback loop system is fully analyzed to build a stable homodyne OPLL. All components are integrated on a single substrate within the compact size of 10 × 10mm^2, and a 1.1GHz loop bandwidth and a 120psloop delay are achieved. The binary phase-shift keying receiver exhibits error-free (BER<10^{-12}) up to 35Gbit/s and BER<10^{-7} for 40Gbit/s with no latency, and consumes less than 3W power.

OCIS codes: (060.1660) Coherent communications; (250.5300) Photonic integrated circuits; (350.4010) Microwaves.

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1. Introduction

Digital coherent optical communication has been revived due to demand for increasing data-rates with high spectral efficiency and its superior sensitivity [1,2]. Recently, the majority of optical receivers use coherent detection based on high speed digital signal processing (DSP), because high data-rate signals can reach long distances even more than 1000km by compensating dispersion and other non-linear effects in the presence of DSPs [1–3].On the other hand, short distance Ethernet networks for metro and access networks use intensity-modulation and direct-detection, because it might be redundant to use complicated analog-to-digital convertors (ADCs) and DSPs, and power consumption and product cost issues should also be considered [4]. The Costas loop by simple feedback loop configuration could be a promising solution for high speed optical receivers with energy efficiency and low cost.

However, the Costas loop as a homodyne optical phase locked loop (OPLL) has been regarded challenging because of long delay in the feedback loop due to the bulk size of photonic, electrical, and loop filter components [1,5]. This long loop delay limits the loop bandwidth which determines phase-noise suppression range for the local oscillator (LO) laser and track / hold ranges against received carrier signals. In this case, the OPLL requires stable and narrow linewidth reference sources for both the LO and transmitting lasers to keep a proper receiver system operation within a stable phase lock [6–9].

Recently, many OPLL researches have reported a relatively stable feedback loop using integration technology. A homodyne OPLL using a high speed HEMT for a small delay loop filter with a loop bandwidth of 300MHz [10], a heterodyne OPLL using an RF exclusive-OR (XOR) as a phase detector with loop delay of 1.8ns [11], and a highly integrated heterodyne OPLL using an integrated single side band mixer and a phase frequency detector (PFD) with delay of 0.2ns and closed loop bandwidth of 550MHz [12] have been published. OPLL based coherent optical receivers have been also developed. Costas receivers using homodyne OPLLs with below 10Gbit/s [13,14], decision-driven loops including sub-carrier modulation scheme [15,16], and a digital OPLL using a sampled I-Q signals with slow DSP for homodyne reception of PSK 40Gbit/s [5] have been published. However, the receivers still require a narrow linewidth on LO and transmitting lasers due to a narrow loop bandwidth, and they may need additional blocks such as voltage controlled oscillators, a Mach–Zehnder modulator, an optical filter, and even ADCs and DSPs to recover the carrier signal.

In this paper, as an extension of [17], a 40Gbit/s coherent optical receiver using a Costas loop is demonstrated. The characteristics of each components and feedback loop are fully analyzed to optimize the OPLL system with a novel loop filter design topology. The receiver is realized within a compact size of $10 \times 10\text{mm}^2$, and it exhibits a closed loop bandwidth of 1.1GHz and loop delays of 120ps. In addition, the digitally operating electrical circuits make the OPLL more robust against photocurrent fluctuations, and the PFD extends phase-lock and frequency pull-in ranges. As a result, a stable OPLL and binary phase-shift keying (BPSK)

coherent receiver error-free (BER < 10^{-12}) up to 35Gbit/s and BER<10^{-7} for 40Gbit/s are achieved. The BPSK receiver consumes less than 3W power.

2. A homodyne OPLL and loop analysis

A homodyne OPLL is designed with the concept of the schematics shown in Fig. 1. It mainly consists of a photonic integrated circuit (PIC), an electrical integrated circuit (EIC), and a hybrid loop filter.

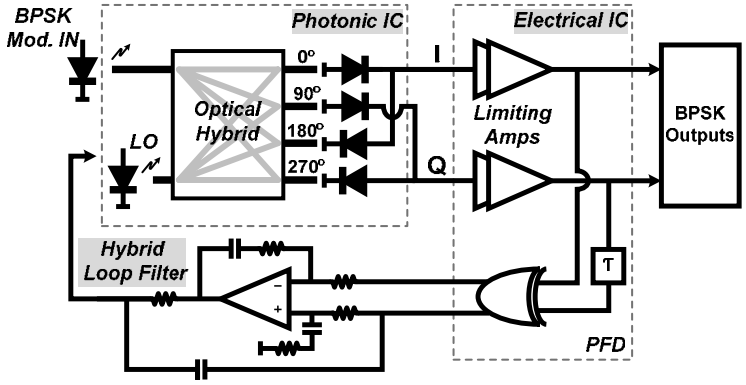

Fig. 1. A concept schematic for a homodyne OPLL structure using a Costas loop.

2.1 Photonic integrated circuit (PIC)

The fabricated PIC is based on the InGaAsP/InP platform. The PIC includes a widely tunable sampled grating distribute Bragg reflector (SG-DBR) laser which can be tuned over a 40nm wavelength span by current injection into front / back mirrors and a phase tuning section diode. The received signal and LO laser are mixed by an integrated 90° optical hybrid and down-converted by four uni-traveling carrier PDs for I-Q electrical outputs. The fabricated optical hybrid has ± 2% imbalanced outputs and the PDs exhibit a 3-dB bandwidth of 30GHz and 18mA saturation current at −5V. The PIC chip size is 4.30 × 0.56mm^2 and has 40ps propagation delay. The details about this PIC can be found in [18].

2.2 Electrical integrated circuit (EIC)

The EIC has been designed using Teledyne's 500nm HBT process which has 300GHz f_t and f_{max} [19]. It includes input biasing circuits to supply −2V bias on PIC PDs with 50Ω interface. Limiting amplifiers (LIAs) limit the PD outputs to 0.3Vp-p digitized signals containing only phase and frequency error information. Due to digital operations in the feedback system by LIAs, the OPLL system becomes less sensitive to the PIC's intensity variations. A PFD is composed of an XOR with a 10ps delay-line, which is called the quadricorrelator type, to cover a 50GHz frequency pull-in range [20]. The EIC chip size is 1.30 × 1.20mm^2 and has a 50ps propagation delay. The details about this EIC can be found in [21].

2.3 Hybrid loop filter

The hybrid loop filter has been implemented using a feed-forward technique consisting of an integrator for a main path and a differentiator for a feed-forward path. A bulk operational amplifier (OPA) is used to obtain high gain at DC and low frequencies, but the OPA has long delay which could limit the bandwidth of OPLLs. In order to minimize the delay effect, a passive capacitor is added on the feed forward path for only high frequencies. As a result, the effective loop delay by the loop filter becomes negligible, and the loop bandwidth is only limited by the delay from PIC, EIC, and interconnections (30ps) [17].

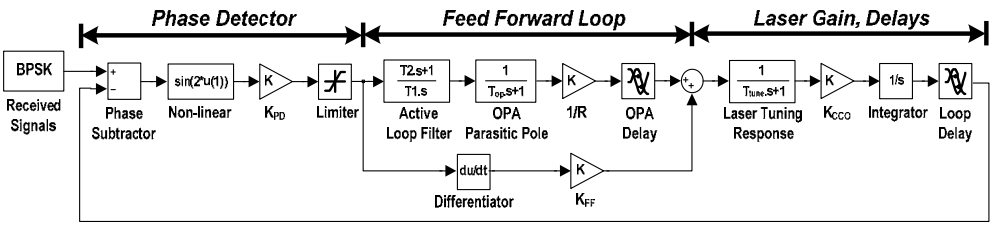

Fig. 2. Modeling for the OPLL analysis.

2.4 Feedback loop analysis

A phase based feedback loop analysis has been conducted using Matlab Simulinkas shown in Fig. 2. A phase detector is modeled by sinusoidal and hard limiting non-linear function for the LIA chain and XOR-type binary phase detection [22]. The feed-forward loop is modeled with two independent paths. The integrator path includes a first order active loop filter, OPA's second order pole, a resistor, and the OPA delay. The differentiator path has a zero, and a coupling gain determined by a capacitor value. The feed-forward loop must avoid 180° phase difference between two paths to prevent an amplitude notch at the crossover frequency. In addition, a laser slow tuning response, laser tuning sensitivity, an integrator for frequency to phase transform, and total effective loop delay are modeled as shown in Fig. 2. Based on the model parameters, the open loop response *T(s)*is expressed as

$$T(s) = K_{PD} \cdot K_{CCO} \cdot \frac{1}{\tau_{tune} s + 1} \cdot \left(\frac{\tau_2 s + 1}{\tau_1 s^2} \cdot \frac{1}{\tau_{OP} s + 1} \cdot \frac{1}{R} \cdot e^{-\tau_{d\_OP} s} + \frac{C_{FF}}{2} \right) \cdot e^{-\tau_d s}, \qquad (1)$$

where a linear equivalent phase detection gain K_{PD} = 0.2~0.4V/rad, a laser tuning sensitivity K_{CCO} = 5.0 × 10^{13}rad/sec/A, a laser slow tuning response τ_{tune} as a pole at 100MHz, active loop filter pole $\tau_1$and zero $\tau_2$determined at 0.17MHz and 2.2MHz, respectively, an OPA's second pole τ_{OP} at 200MHz, a resistor R of 500Ω, an OPA's delay τ_{d_OP} of 200ps, a coupling capacitor on feed-forward path C_{FF} of 1.0pF, and a total effective loop delay τ_d of 120ps are characterized. Especially, non-linear phase detector gain K_{PD} is approximated and optimized with a linear equivalent gain [23]. The open loop response *T(s)* for the OPLL is obtained as shown in Fig. 3, and it shows that the total loop response follows the main path at low frequencies and the feed-forward path at high frequencies. From the response, the feedback loop response shows a natural frequency ω_n of 4.4 × 10^9rad/sec (700MHz) and 65° phase margin.

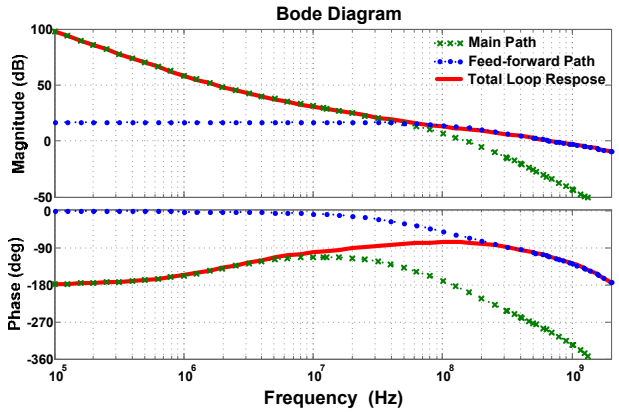

Fig. 3. A Bode diagram for the OPLL open loop response *T(s)*.

3. Implementation and experiment results

3.1 Integration for the OPLL

The OPLL for Costas loop receiver is realized as shown in Fig. 4. The fabricated PIC on the top, the EIC on the bottom left, and the hybrid loop filter on the bottom right are mounted on a single AlN substrate (ε_r = 9 and thermal conductivity = 140~180W/m/K) within the total size of 10 × 10mm^2. They are connected by wire-bonds and transmission lines, and the feed-forward path (red arrow shown in Fig. 4) is minimized to decrease their interconnection delay. The loop filter uses a commercial voltage feedback OPA, Texas Instruments' LMH6609, which has 70dB open loop gain and 200MHz unity gain bandwidth. Together with discrete chip capacitors and resistors, the active loop transfer function has been realized.

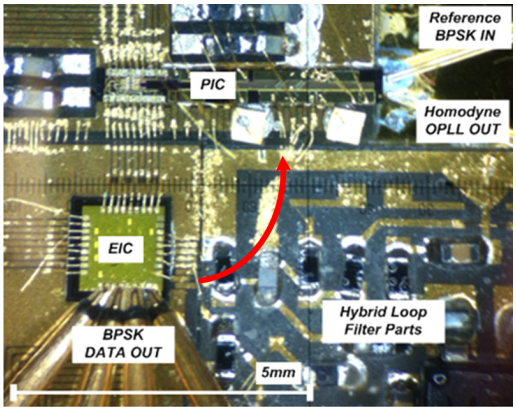

Fig. 4. A photograph of the Costas loop based on a homodyne OPLL receiver (Red arrow: feed-forward path).

3.2 Homodyne OPLL experiments

The homodyne OPLL has been tested to measure the closed loop bandwidth and locked SG-DBR laser linewidth performance. The test setup for the OPLL is explained in [17], and the OPLL has a 1.1GHz closed loop bandwidth as shown in Fig. 5(a), which is the widest loop bandwidth to the best of our knowledge. Peak beat tone is shown at 100MHz, and two side peak tones represent the closed loop bandwidth because of under damping shown at 1GHz – left peak as an image frequency and 1.2GHz – right peak as a real frequency. The linewidths for the un-locked SG-DBR laser, locked SG-DBR laser, and reference laser are measured and compared, as shown in Fig. 5(b), using a self-heterodyne linewidth measurement technique. The un-locked SG-DBR laser shows a broad linewidth of 10MHz, but the locked SG-DBR laser exhibits a linewidth of 100kHz which is the same as the reference laser linewidth. As a result, the wide loop bandwidth suppresses the SG-DBR laser's phase noise for broad frequency range, extends track and hold range against the received laser's carrier frequency drifts, and the Costas loop can catch the received laser carrier phase.

3.3 BPSK receiver experiments

To prove the Costas loop receiver performance, eye outputs and bit-error-ratio (BER) performance are measured. This test setup for the BPSK demodulation is explained in [17], and Figs. 6(a) and 6(b) show received open eye patterns for 25Gbit/s and 40Gbit/s, respectively. BER vs. optical signal-to-noise ratio (OSNR) is shown in Fig. 6(c), and it exhibits superior performance of error-free (BER < 10^{-12}) up to 35Gbit/s and BER <10^{-7} performance for 40Gbit/s. In addition, as shown in Fig. 5(b), the linewidth of the locked SG-DBR laser with 25Gbit/s BPSK data shows the same linewidth performance as the locked SG-DBR laser and the reference laser. This means that the Costas loop with a 25Gbit/s BPSK

data modulation can restore the carrier phase without degrading the linewidth and data reception performance.

This receiver system consumes less than 3W power (PIC < 0.5W, EIC < 2.2W, and loop filter < 0.1W), not including a thermoelectric controller power.

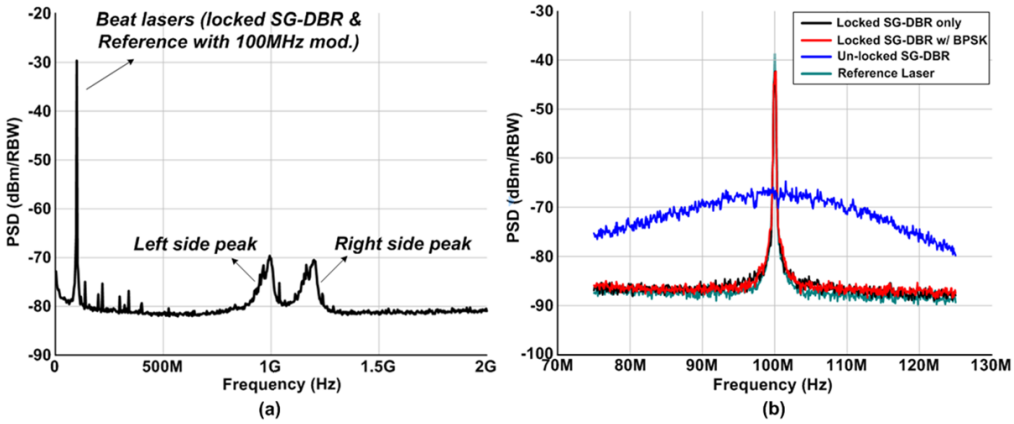

Fig. 5. Homodyne OPLL measurement results (a) Beat spectrum between the reference laser and locked SG-DBR laser, and (b) Measured linewidths: locked SG-DBR laser without BPSK modulation, locked SG-DBR laser with BPSK modulation, un-locked SG-DBR laser, and reference laser.

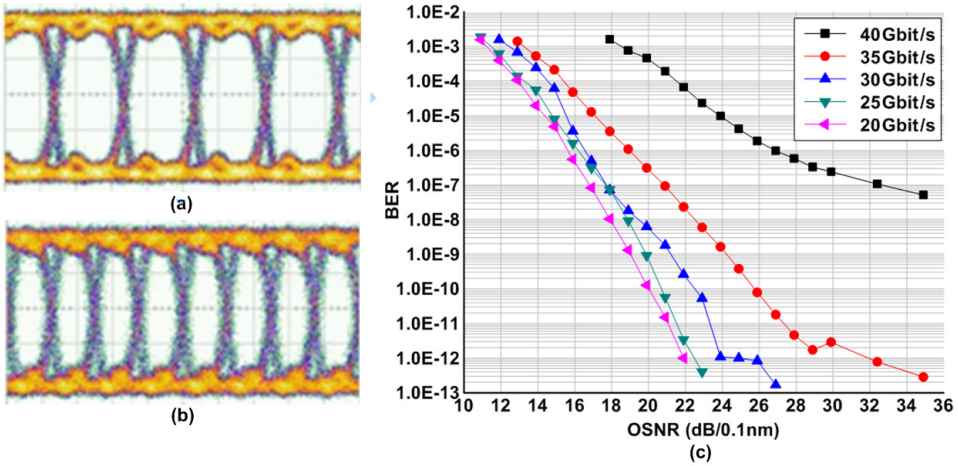

Fig. 6. BPSK data reception tests: (a) Received eye output for 25Gbit/s, (b) Received eye output for 40Gbit/s, and (c) BER vs. OSNR from 20Gbit/s to 40Gbit/s.

4. Conclusion

For the first time, a highly integrated homodyne OPLL based coherent optical receiver has been demonstrated using a Costas loop. A stable OPLL has been achieved within the compact size of 10 × 10mm^2, closed loop bandwidth of 1.1GHz, and 120ps loop propagation delay. The BPSK receiver based on the Costas loop exhibits error-free (BER < 10^{-12}) up to 35Gbit/s and BER < 10^{-7} for 40Gbit/s. The receiver consumes less than 3W power. It might be a promising option for coherent optical receivers in short or mid distance optical communication with low power and low cost.

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