Contact Resistance Limits of Ohmic Contacts to Thin Semiconductor Channels

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Introduction

- III-V transistors are being developed for use in large scale integrated circuits[1]
- Scaling requirements dictate that as device areas scale by 1:2, absolute resistance must remain constant, requiring a 1:2 decrease in resistivities
- ~ 9 nm L_g MOSFETs would need access resistivities of less than 10 Ω µm to suffer a 10 % degredation in perfomance[2]
- HBTs and optoelectronic devices also require lower parasitic resistivities in order to operate at increasing frequency[3]
- MBE can be used to regrow low-resistance, highly doped ohmic contact to InGaAs with careful control of growth conditions[4]
- We present MBE regrown contacts on channels with varying sheet carrier density
- We give an expression dictating the minimum measurable resistance of a TLM structure

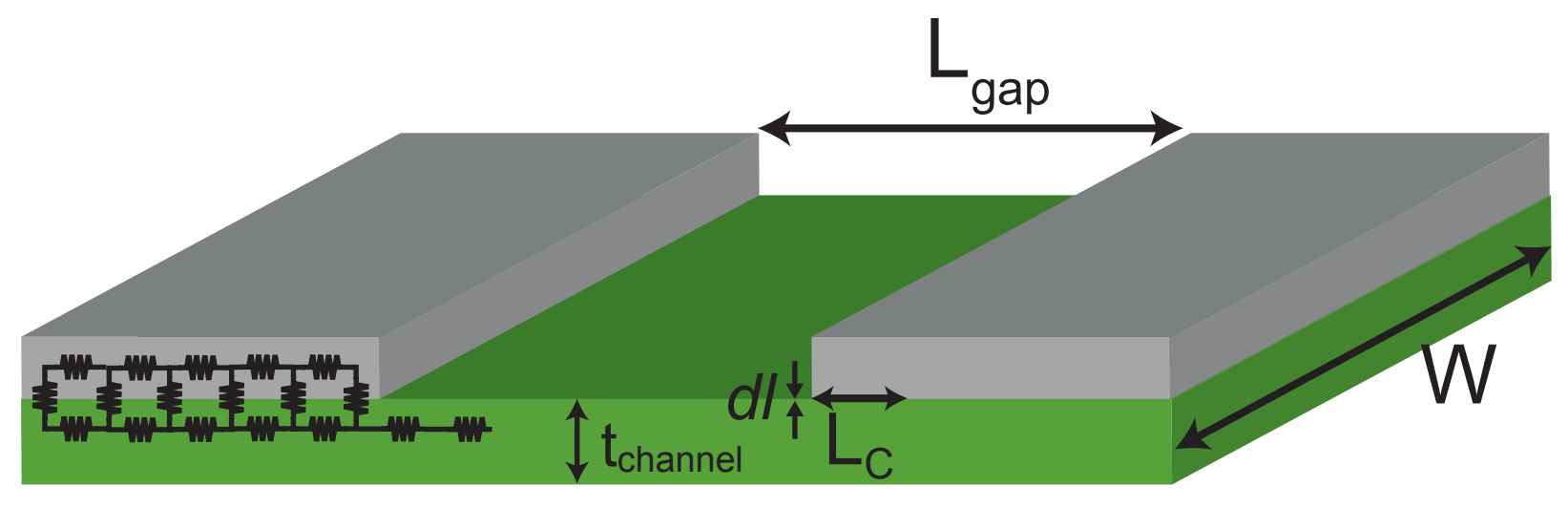

Figure 1: TLM contact measurement structure.

- TLM measurements of total resistance versus gap spacing allow extraction of contact resistance from the formula below:

$$R = 2\frac{\rho_1 \cdot dl}{W \cdot L_C} + \frac{\rho_2 \cdot L_{gap}}{W \cdot t_{channel}} R = 2\frac{\rho_{contact}}{W} + \frac{R_{sheet} \cdot L_{gap}}{W} \text{ where } \rho_{contact} = \frac{\rho_1 \cdot dl}{L_C} \text{ and } R_{sheet} = \frac{\rho_2}{t_{channel}}$$

Experiment

- Samples were growth by solid source MBE lattice matched to semi-insulating InP and strained relaxed on semi-insulating GaAs
- Layer structure on InP:
  - 100 nm n^+ $In_{0.53}Ga_{0.47}As$ Si doped 5×10^{19} cm^{-3}, 150 nm $In_{0.52}Al_{0.48}As$, S. I. InP substrate
- Layer structure metamorphic on GaAs:
  - 15 nm InAs, 3 nm n $Al_{0.76}Ga_{0.24}Sb$ Te doped 3×10^{18} cm^{-3}, 500 nm $Al_{0.76}Ga_{0.24}Sb$, a superlattice with 20 periods of 2.5 nm GaSb and 2.5 nm AlSb, 5.0 nm AlSb, 1 µm GaSb, 300 nm GaAs
- Dummy pillar definition:
  - 300 nm PECVD SiO_2, optical lithography, SF_6 and Ar ICP dry etch
- Regrowth Surface Preparation:
  - UV ozone oxidation, 10 H_2O:1 HCL dip, 3 hour 200 °C and 1 hour 325 °C, 40 min. H-clean at 420 °C at 1×10^{-6} Torr
- Quasi-migration enhanced epitaxy (MEE) regrowth:
  - 500 °C, V:III BEP ratio of ~ 5
  - 60 nm n^+ InAs regrowth on InAs channel
  - 5.0 nm n^+ $In_{0.53}Ga_{0.47}As$, ~ 35 nm grade from n^+ $In_{0.53}Ga_{0.47}As$ to n^+ InAs, 20 nm n^+ InAs on n^+ $In_{0.53}Ga_{0.47}As$ channel
- Mesa isolation and Ti/Pd/Au metalization

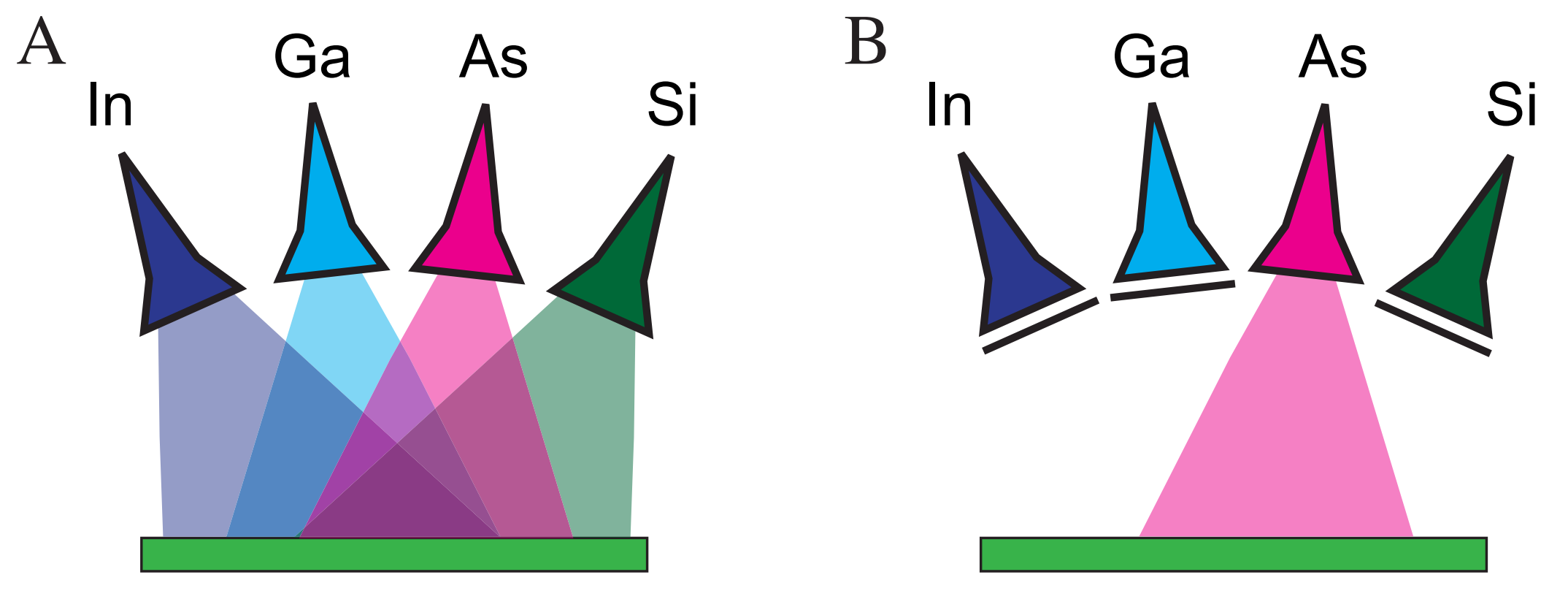

Figure 2: An illustration of quasi-MEE technique showing alternating openings of (A) group III and group V shutters followed by (B) a pause with only group V shutters open.

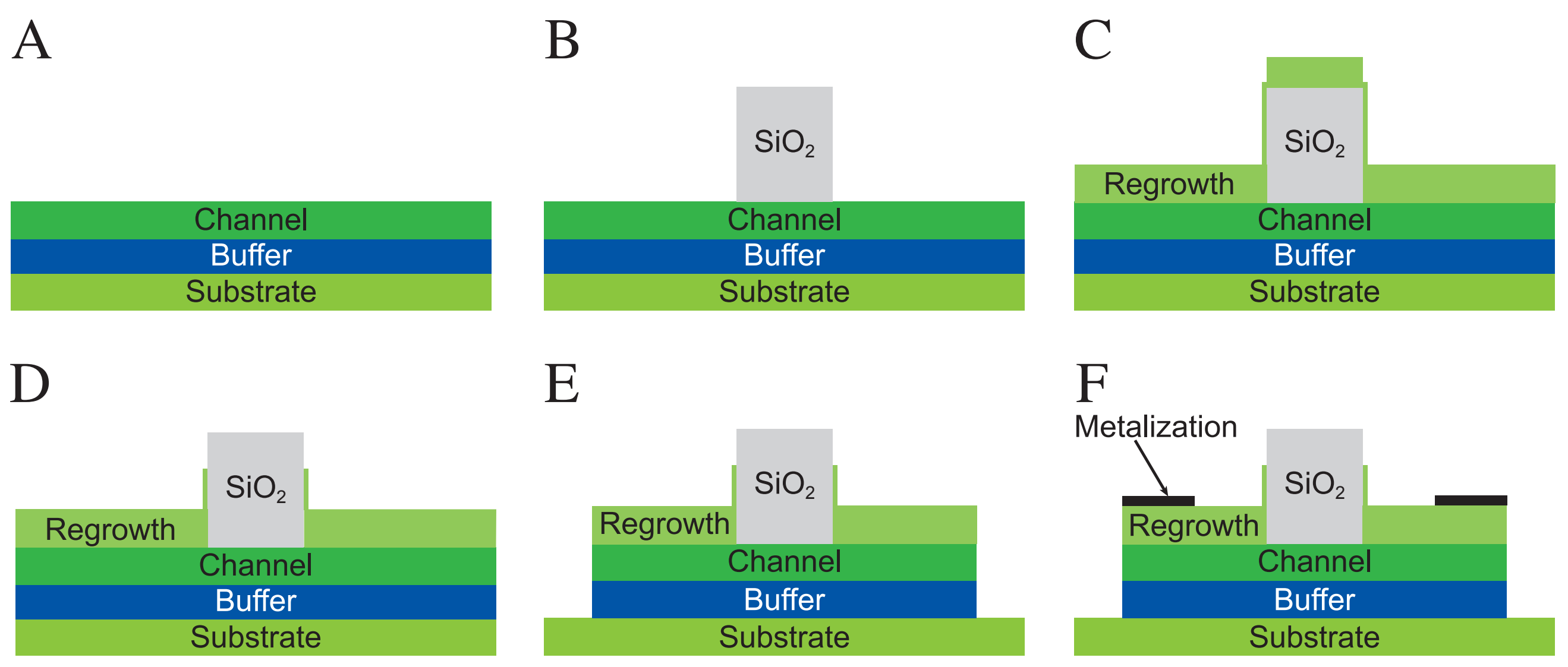

Figure 3: An illustration of the process flow: (A) epi growth, (B) dummy pillar deposition and definition, (C) regrowth, (D) planarization, (E), isolation, and (F) metalization.

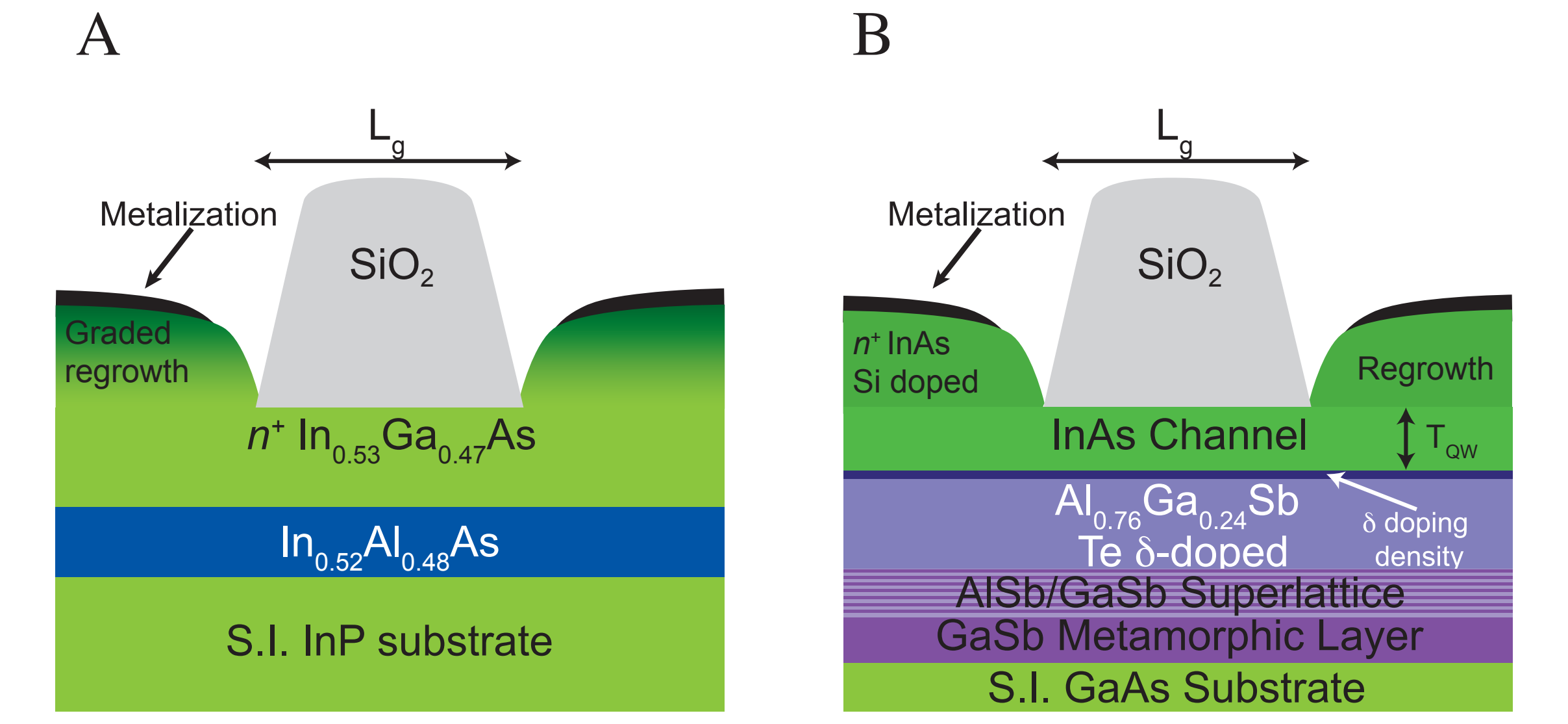

Figure 4: An illustration of the two device structures made to measure contact resistance between channel and regrowth. (A) Graded n^+ $In_{0.53}Ga_{0.47}As$ to n^+ InAs regrowth on 100 nm n^+ $In_{0.53}Ga_{0.47}As$ channel and (B) homoepitaxial n^+ InAs regrowth on 15 nm InAs channel.

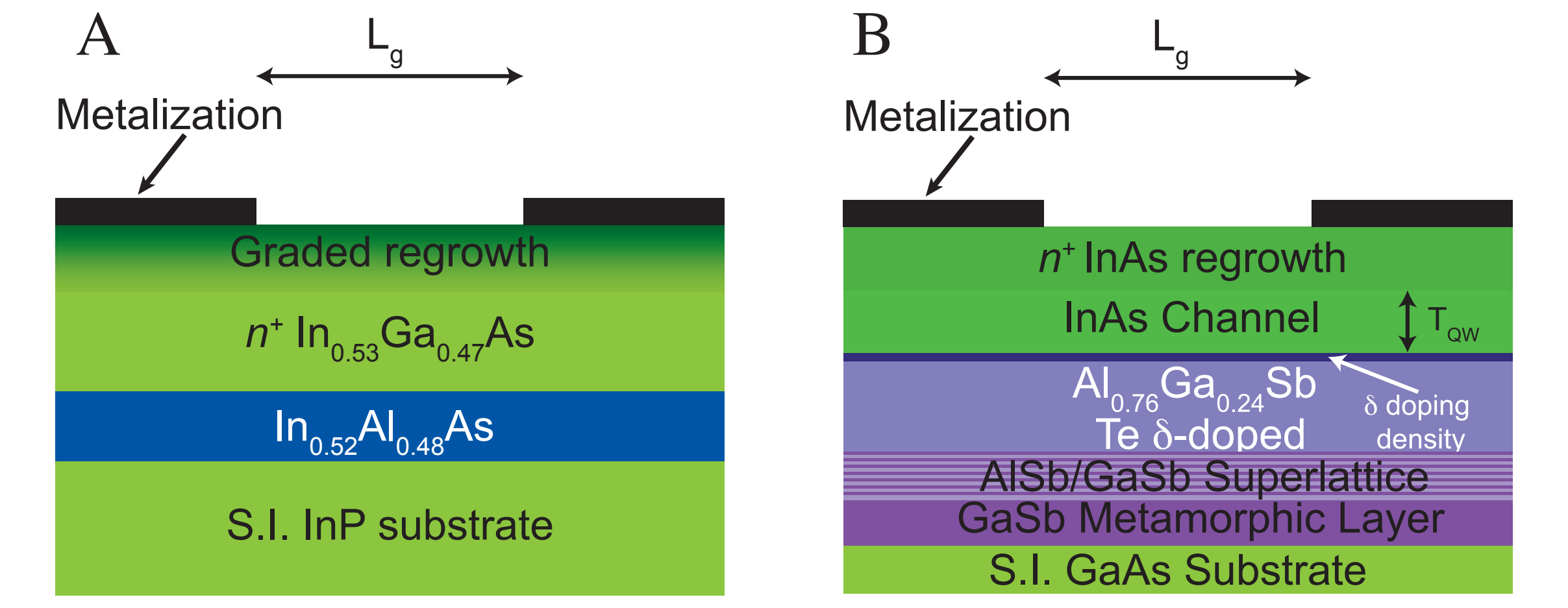

Figure 5: An illustration of the two device structures made to measure contact resistance between regrowth and metal. (A) Graded n^+ $In_{0.53}Ga_{0.47}As$ to n^+ InAs regrowth on 100 nm n^+ $In_{0.53}Ga_{0.47}As$ channel and (B) homoepitaxial n^+ InAs regrowth on 15 nm InAs channel.

Results

- For InAs regrowth, RHEED showed 4x2 surface reconstruction
- For graded regrowth, RHEED showed 4x2 during group III/V shutter openings and 2x4 during group V shutter openings
- SEM of both samples (not shown) demonstrates good fill-in near SiO_2 pillar
- TEM of graded regrowth shows faults begin ~ 5 nm above regrowth interface

Figure 6: Representative RHEED images of InAs regrowth (A) at the beginning of the regrowth and (B) at the end of the regrowth.

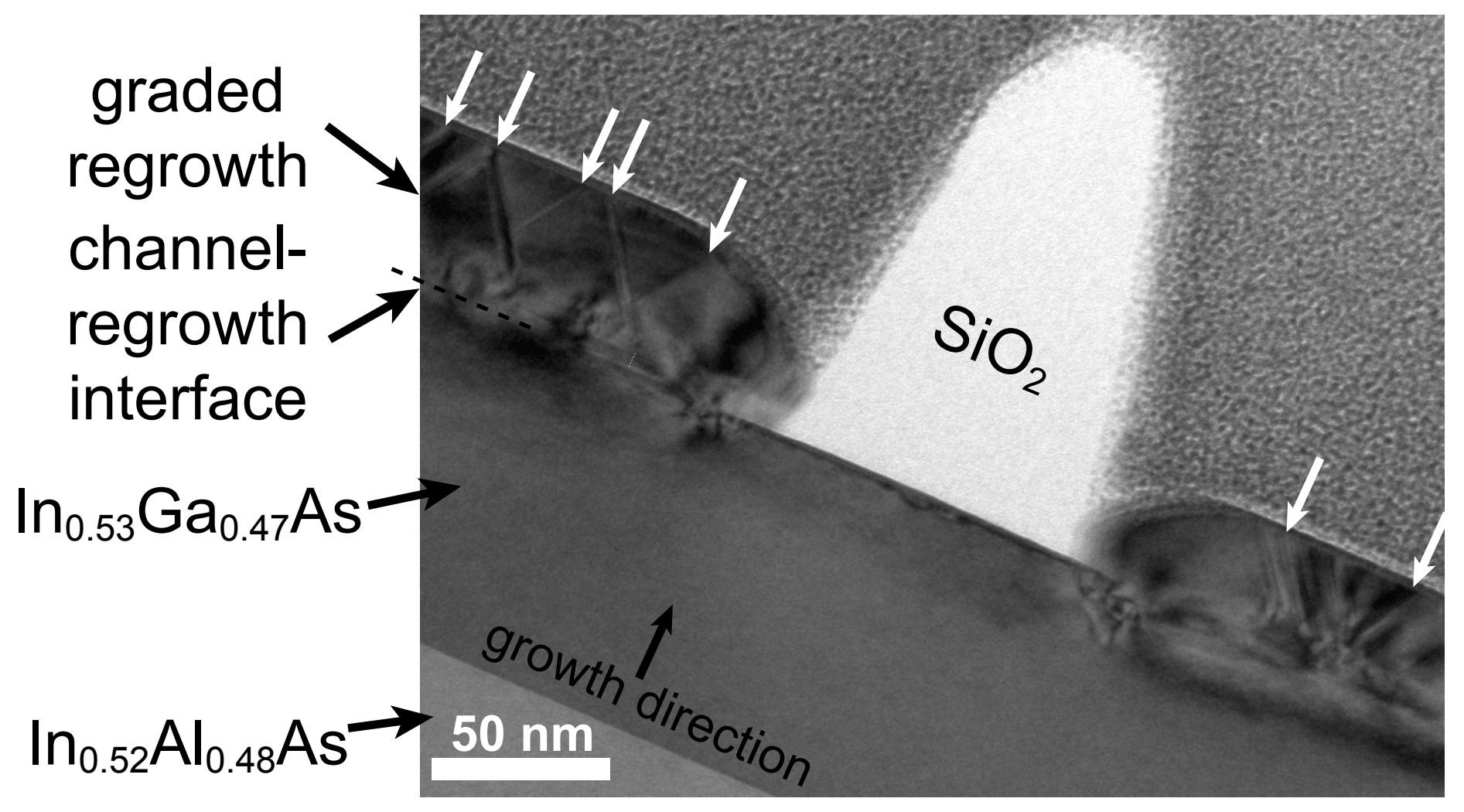

Figure 7: TEM image of the graded regrowth along the <110> showing defects nucleating ~ 5 nm above the channel/regrowth interface with white arrows indicating defects.

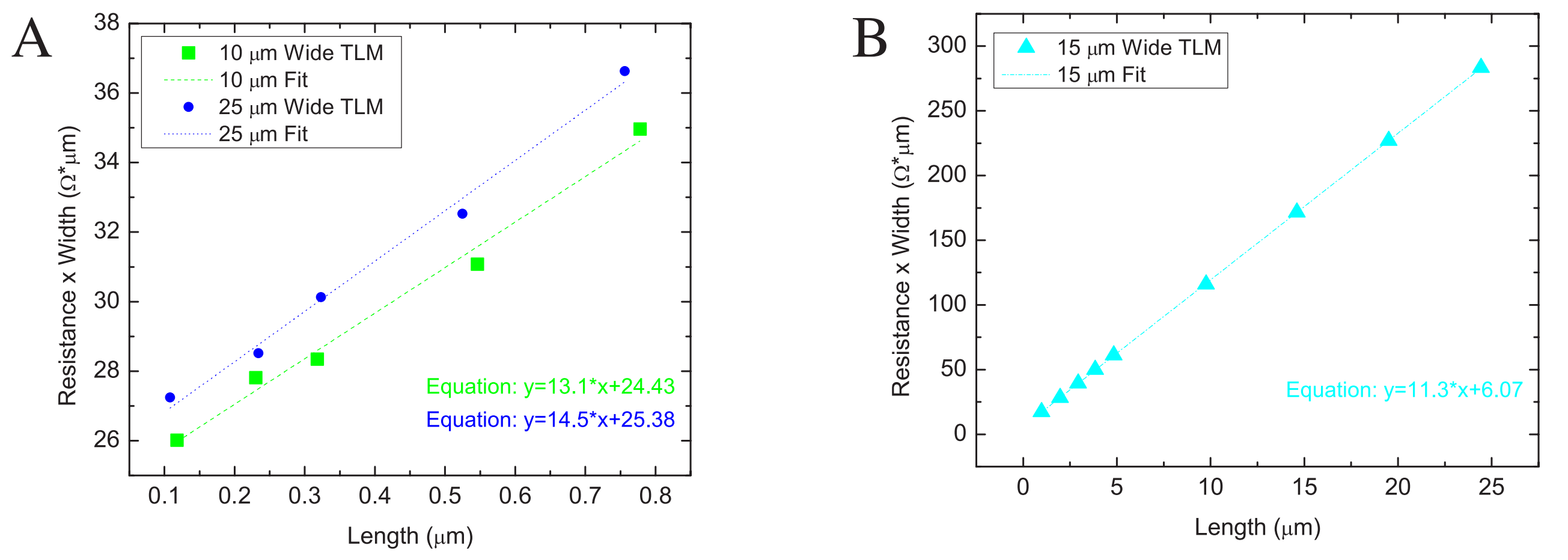

Figure 8: Resistance versus gap spacing for (A) 10 and 25 µm wide TLMs of graded regrowth on top of 100 nm n^+ $In_{0.53}Ga_{0.47}As$ channel (Figure 4 (A)) and (B) 15 µm wide TLMs of metal on top of graded regrowth (Figure 5 (A)).

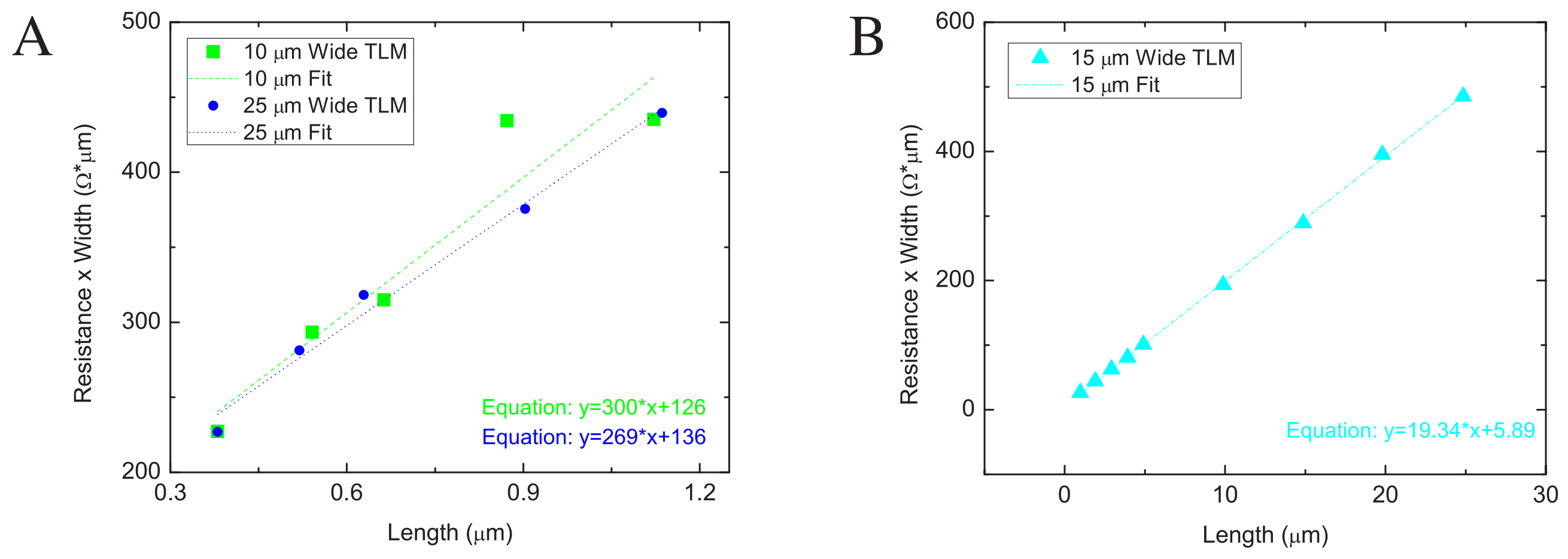

Figure 9: Resistance versus gap spacing for (A) 10 and 25 µm wide TLMs of n^+ InAs regrowth on top of 15 nm InAs channel (Figure 4 (B)) and (B) 15 µm wide TLMs of metal on top of n^+ InAs regrowth (Figure 5 (B)).

- Graded regrowth shows total single-sided contact resistance of ~ 12.5 Ω µm
- Graded regrowth shows metal-regrowth contact resistance of ~ 3 Ω µm
- n^+ InAs regrowth shows total single-sided contact resistance of 65 Ω µm (130 Ω µm double sided)
- n^+ InAs regrowth shows metal-regrowth contact resistance of ~ 3 Ω µm

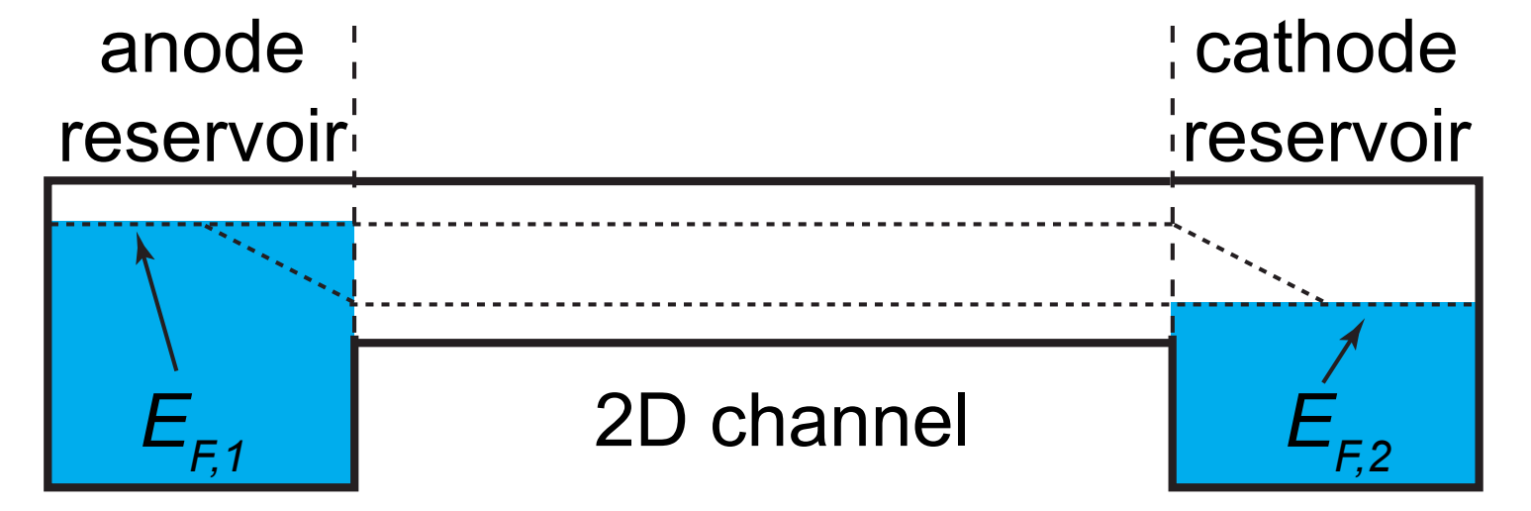

Figure 10: Illustration of TLM device in ballistic, degenerate limit with no scattering and thus two quasi Fermi levels in the channel.

- Considering the structure in Figure 10 yields the relationship for maximum conductivity below
- 15 nm InAs channel has a theoretical minimum resistance of 80 Ω µm and our regrowth is within a factor of two of this at 130 Ω µm

$$G = \frac{q^2 2^{1/2}}{\hbar \pi^{3/2}} \sum_i n_{s,i}^{1/2}$$

Conclusion

- Regrown contacts by MBE can yield contact resistivities as low as 12.5 Ω µm
- There is a maximum measurable conductivity for a TLM structure of given sheet carrier density
- Our results are within a factor of 2 of our theoretical predictions
- This maximum conductivity may obscure true contact resistivity in any material system
- This limit must be considered when extracting accurate contact resistance in any materials system or TLM-like structure

References

1. M. J. W. Rodwell, U. Singisetti, M. Wistey, G. Burek, A C. Gossard, C. J. Palmstrom, E. Arkun, P. Simmonds, S. Stemmer, R. Engel-Herbert, Y. Hwang, Y. Zheng, P. Asbeck, Y. Taur, C. Sachs, A. Kummel, P. McIntyre, C. Van de Walle, and J. Harris, "Technology Development and Design for 22 nm InGaAs/InP-Channel MOSFETs," **2008 IEEE Indium Phosphide and Related Materials Conference**, Versailles, France, 2008.
2. M. J. W. Rodwell, M. A. Wistey, U. Singisetti, G. J. Burek, E. Kim, A. Baraskar, J. Cagnon, Y. -J. Lee, S. Stemmer, P. C. McIntyre, A. C. Gossard, B. Yu, P. Asbeck, and Y. Taur, "Process Technologies for Sub-100 nm InP HBTs and InGaAs MOSFETs," **8th Topical Workshop on Herosctructure Microelectronics**, Nagano, Japan, 2009.
3. M. J. W. Rodwell, E. Loisser, M. Wistey, V. Jain, A. Baraskar, E. Lind, J. Koo, Z. Griffith, J. Hacker, M. Urteaga, D. Mensa, R. Pierson, and B. Brar, "THz Bipolar Transistor Circuits: Technical Feasibility, Technology Development, Integrated Circuit Results," **2008 IEEE Compound Semiconductor IC Symposium**, Monterey, CA, 2008.
4. M. A. Wistey, G. J. Burek, U. Singisetti, A. Nelson, B. J. Thibeault, S. R. Bank, M. J. W. Rodwell, and A. C. Gossard, "Regrowth of Self-Aligned, Ultra Low Resistance Ohmic Contact on InGaAs," **5th International Conference on Molecular Beam Epitaxy**, Vancouver, Canada, 2008.

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