A 58.4mW Solid-State Power Amplifier at 220 GHz using InP HBTs

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***Abstract* — A 220 GHz solid state power amplifier MMIC is presented demonstrating 58.4 mW of output power with 5.4dB compressed gain. The 8-cell amplifier has a small signal gain of 8.9 dB at 220 GHz, and 3-dB bandwidth from 206 to 242GHz. Amplifier cells are formed using a 250nm InP HBT technology and a 5um BCB thin-film, non-inverted microstrip wiring environment. Power division and combining of the eight amplifier cells is done by a 2-1 quarter wave combiner series connected to a 4-1 Dolph-Chebyshev combiner. More than 50mW of output power was observed from 215 to 225GHz.**

***Index Terms* — Millimeter wave integrated circuits, MMICs, Power amplifier, Solid State Power Amplifier (SSPA).**

I. Introduction

Future high resolution imaging systems and high bandwidth communications systems will benefit from the continued development of solid-state power amplifiers (SSPA), where there has been active interest to increase the saturated output power at 220GHz. These high power signals may be used to drive multiplier chains for THz applications, or to drive power vacuum tube amplifiers within the 220GHz low-loss free space propagation window. For other prospective applications, significant output power is necessary at 220GHz and above to overcome attenuation due to weather events.

The highest output power reported for a solid-state G-band (140-220GHz) power amplifier is from an InP HEMT technology having 75mW of saturated output power at 210GHz, in a waveguide-block package [1]. An early G-band medium power amplifier using InP HBT produced greater than 8 mW saturated P_{out} at 190GHz [2]. Recently, advances in InP HBT gain and bandwidth at the 250nm node have made it a viable candidate for much higher power amplification at high mm-, sub-mm-wave frequencies [3]. From these technology advancements, InP HBT SSPA amplifiers have been reported with 47.9mW P_{out} from 210 to 220GHz [4].

For a PA cell to have appreciable gain and P_{out} at 220GHz, the transistor finger count and length will be limited by issues associated with device self-heating and interconnect parasitics forming the multi-finger device. At these frequencies, higher P_{out} is achieved through power combining PA cells using combiner structures. Careful design of the combiner is necessary to avoid excessive skin-effect loss; if the insertion loss exceeds ~ 1.0–1.5dB, no significant increase in P_{out} can come from on-chip combining. InP HEMT SSPA's using 4-1 combiners at 220GHz have been realized with Dolph-Chebyshev structures formed in G-CPW [1]. InP HBT 220GHz SSPA's have separately made use of similar 4:1 Dolph-Chebyshev structures, as well as λ/4-wave 2:1 combiners, but in low-loss thin-film microstrip form [4].

In this paper, an 8-cell InP HBT SSPA is reported using both 2-1 and 4-1 low-loss on-chip power division and combining. The SSPA exhibits 8.9dB small signal gain at 220GHz, and 3-dB bandwidth from 206 to 242GHz. Power measurements show 58.4 mW P_{out} with simultaneous 5.4dB gain at 220GHz. The measured loss of the 2-1 and 4-1 combiners in the 5-μm BCB ($\varepsilon_r = 2.7$) non-inverted thin-film microstrip wiring is 0.7dB per structure. To the authors' knowledge, this is the highest RF output power for an InP HBT SSPA in this band to date.

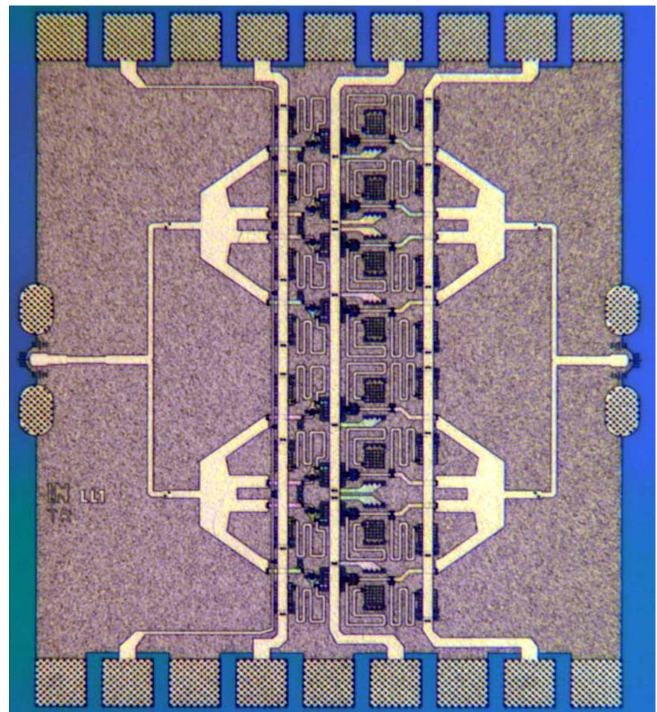

Fig. 1. An IC micrograph of the 220GHz, 8-cell InP HBT solid state power amplifier (SSPA). Dimensions: 0.90x1.1mm^2.

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II. 250NM INDIUM PHOSPHIDE HBT PROCESS

A 250nm InP HBT technology having ~4.5V breakdown voltage was used for amplifier design. The peak bandwidth of a single HBT was f_{max} = 700GHz and f = 400GHz. At the amplifier's quiescent bias of I_c = 5.5mA/μm^2 and V_{ce} = 2V, a single HBT showed f_{max} = 590GHz and f = 350GHz. HBT amplifier cells used 4-emitter fingers, each with L_e = 6-μm. The physical sizes of device footprints were 18x7.5μm^2 for common emitter and 16x9μm^2 for common base configuration. At the quiescent amplifier bias, the PA cells exhibit f_{max} = 530GHz and f = 333GHz, showing that the parasitics associated with the multi-finger devices have little effect on the available gain and bandwidth of the amplifier cell at 220GHz.

MMIC fabrication included 4-levels of interconnect metal. 1.0 μm-thick metal layers were separated by 1.0 μm BCB (ε_r = 2.7). The process supported the use of compact, stacked interconnect vias for the first, second, and third interconnect levels. MIM capacitors (SiN_x, 0.3fF/μm^2) were formed between the first and second level of interconnect metal, and 50Ω/square thin-film resistors were available.

III. MMIC POWER AMPLIFIER DESIGN

The amplifier circuits were simulated in Advanced Design System (ADS) using an Agilent-HBT model for the 250nm HBT technology. All interconnects, MIM capacitors, device feed structures, and probe pads were simulated using the ADS Momentum 2.5-D electromagnetic simulator.

Thin-film microstrip was formed by using the lowest metal interconnect (MET-1) as ground and higher interconnects (MET-3, MET-4) for signal. A non-inverted thin-film microstrip wiring environment was selected to minimize interconnect inductance between the emitter terminal and ground plane for the common emitter (CE) HBT and between the base terminal and ground plane for the common base (CB) HBT. This is particularly important for the common-base device as small amounts of added inductance at the base node often causes a significant reduction to the amplifier stability margin. The minimal ground-return inductance of a large, continuous ground plane also helps to make the amplifier

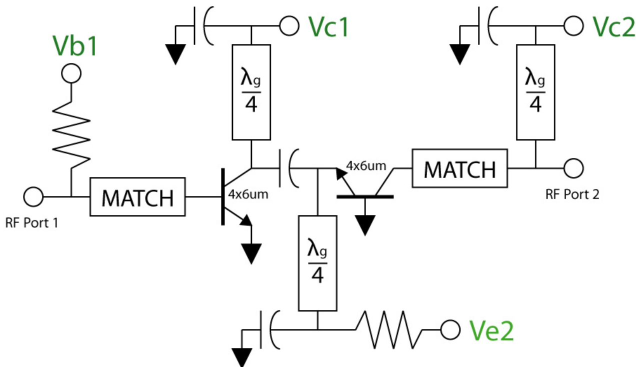

Fig. 2. Schematic of a cascode HBT amplifier cell.

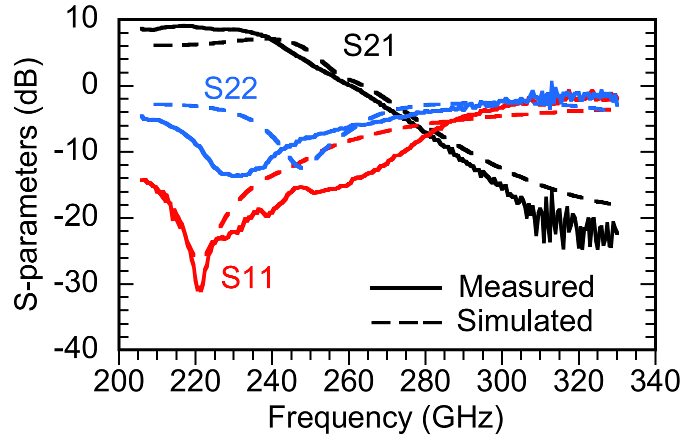

Fig. 3. S-parameters of the 8-cell InP HBT SSPA. 3-dB bandwidth extends from 206 to 242GHz.

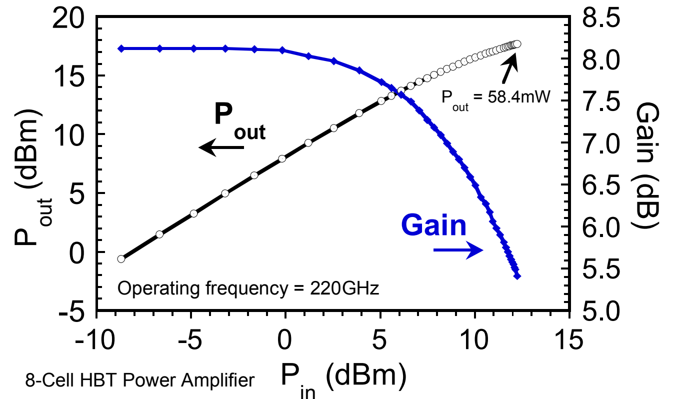

Fig. 4. A 220GHz power sweep of the 8-cell SSPA. 58.4mW P_{out} was measured with 5.4dB gain.

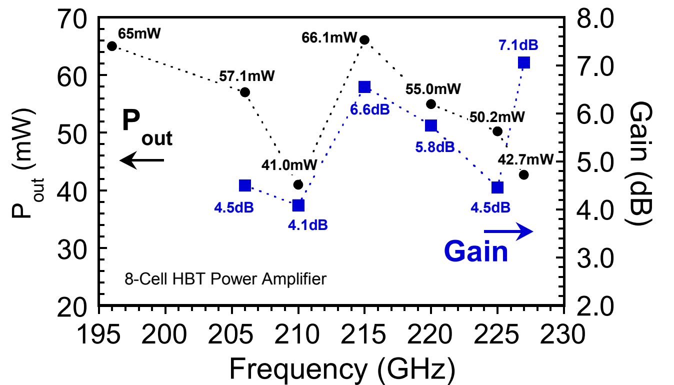

Fig. 5. Power sweep versus frequency. of the 8-cell SSPA. More than 50mW of output power was observed at points from 215 to 225GHz. Limited source power prevented observation of higher SSPA saturated output power.

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broadband, since additional reactive cancellation is not needed as part of the matching networks.

A single power amplifier cell was designed using a cascode cell constructed with one 4-finger CE and one 4-finger CB HBT, shown in figure 2. DC bias is fed into the HBTs with quarter-wave chokes. High cell gain was achieved by matching the input of the cascode to 50-Ω Z_o. High output power was achieved by matching the output impedance to a load line within the high performance operating area of the device. This operating area is the region of the I_c vs. V_{cb} curve defined by the HBT's saturation voltage, maximum current density, safe operating power density, common base breakdown voltage, and variation of f with DC bias. The quiescent DC bias chosen was J_e =5mA/μm^2 and V_{cb}=1.5V.

On-wafer power splitting and combining was used to create the 8-cell amplifier. A 2-1 $\lambda_g/4$ combiner used two 70-Ω Z_o impedance transformers to match all three ports to 50-Ω Z_o. The measured insertion loss per 2-1 combiner stage was 0.6dB. A 4-1 combiner uses high Z_o transmission lines to feed a central point. A small MIM capacitor is added to tune the EM structure for low loss at 220GHz. The measured insertion loss of one 4-1 combiner stage was 0.75dB.

IV. Experimental Results

SSPA MMIC on-wafer S-parameters were measured using an Agilent 8510C VNA with WR-03 OML frequency extender modules after an LRRM probe tip calibration [5]. The DC bias conditions of the cascade cell are: V_{b1} = 2.1V, V_{c1} = 2.1V, I_{c1} = 260mA, V_{e2} = -4.2V, V_{c2} = 1.8V, I_{c2} = 262mA. Figure 3 shows the S-parameters of the 8-cell SSPA. At 220 GHz, the gain is 8.9dB, and at 217GHz the peak gain is 9.1dB. The 3-dB bandwidth extends from 206GHz to 242GHz.

For large signal power measurements, a 210-227GHz VDI amplifier multiplier chain (AMC) is used (see figure 6), where waveguide transitions are necessary to adapt the WR-04 output to WR-03 for on-wafer probing. Output power was measured by an Erickson PM4 sub-mm wave power meter. Power data was corrected for measured insertion loss of components between the probe tips and power meter. Source power was insufficient to drive the amplifier into saturation at the source boundaries.

Under the aforementioned DC bias conditions, the 8-cell SSPA demonstrated 58.4mW output power with 5.4dB compressed gain at 220GHz (see figure 4). At 215GHz, 66.1mW was measured with 6.6dB gain. Figure 5 shows the SSPA P_{out} and gain from 210-227GHz, where at least 50mW of output power is measured from 215-225GHz.

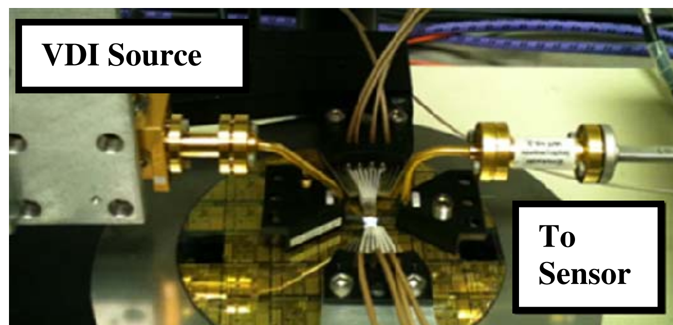

Fig. 6. Photograph of the power measurement setup. The VDI source drives the amplifier through a WR-03 GSG probe. Output power of the SSPA is measured with a sub-mm wave calorimeter.

VII. Conclusion

A 220GHz 8-cell SSPA is reported using a 250nm InP HBT technology. The eight amplifier cells were combined using 2-1 and 4-1 on-wafer microstrip combiners. The total transistor output periphery was 192μm and the SSPA showed an output power of 58.4mW at 220GHz with 5.4dB power gain (using a probe tip calibration).

This amplifier represents a first-pass design success, as challenges associated with G-band SSPA design were thoroughly identified and then mitigated with a customized design kit and layout library. Future SSPA designs employing more gain stages are under development—this will relax the demands of the source and higher SSPA P_{out} is expected as the amplifier may be driven further into compression.

Acknowledgement

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