A Single-Chip 630 GHz Transmitter with 210 GHz Sub-Harmonic PLL Local Oscillator in 130 nm InP HBT

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***Abstract* — We present a 630 GHz transmitter IC based on a 210 GHz PLL and 3rd-order sub-harmonic transmit mixer in an 130nm InP HBT process. The transmitter output can be tuned across 15 GHz with -51 dBc and -74 dBc of phase noise at 100 Hz and 10 KHz offset, respectively. Measured saturated RF power was -30 to -33 dBm, while consuming 650 mW. The transmitter IC occupies 1.37 mm^2. To the authors' knowledge, this work represents the first terahertz transmitter with on-chip (phase-locked) frequency generation.**

***Index Terms* — Terahertz, transmitter, phase-locked loops, hetero-junction bipolar transistors, dynamic frequency dividers.**

I. Introduction

Sub-millimeter-wave and terahertz (THz) frequency bands covering 300 GHz to 3 THz have applications in security/medical imaging systems, radar, chemical/bio sensors, and high-rate data communications. Various THz transceiver building blocks up to 670 GHz have been reported in indium phosphide-based (InP) high electron mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs) [1-4]. For compact, low-power THz radio systems, single-chip integration of such THz building blocks is necessary, while obviating lossy waveguide transitions and enabling the implementation of dense arrays of THz imager/sensor. In this paper, a 630 GHz transmitter IC with integrated sub-harmonic PLL local oscillator in InP HBT technology is presented.

II. InP HBT Technology

In this work, a 130 nm emitter width InP HBT technology was used. Details of the device technology can be found in [5]. Key features of the process technology are the use of electron-beam lithography and electroplating to form the emitter contact, and the use of dielectric sidewall spacers to form a self-aligned base-emitter junction. Circuits were fabricated on 4-inch InP substrates and the HBT IC process includes thin-film resistors (50 Ohm/sq), MIM capacitors, and 3-levels of gold interconnect (M1-M3). A 7 µm thick BCB layer is used between M2 and M3 to facilitate the formation of low-loss thin-film microstrip lines.

The highly-scaled HBTs support very high current (>30 mA/µm^2) and power (>50 mW/µm^2) densities. The common-emitter breakdown of the transistors is BV_{CEO} = 3.5 V (J_E = 10 µA/µm^2). Transistor *S*-parameter measurements are performed using on-wafer extended reference plane microstrip TRL calibration structures and RF figures-of-merit are extracted. A 0.13×2 µm^2 HBT exhibits a current gain cutoff frequency f_t= 520 GHz and a maximum frequency oscillation f_{max}= 1.1 THz at I_C= 6.9 mA and V_{CE}= 1.6V. Longer emitter length devices exhibit progressively smaller values of f_{max} due to distributed resistance effects along the length of the base mesa.

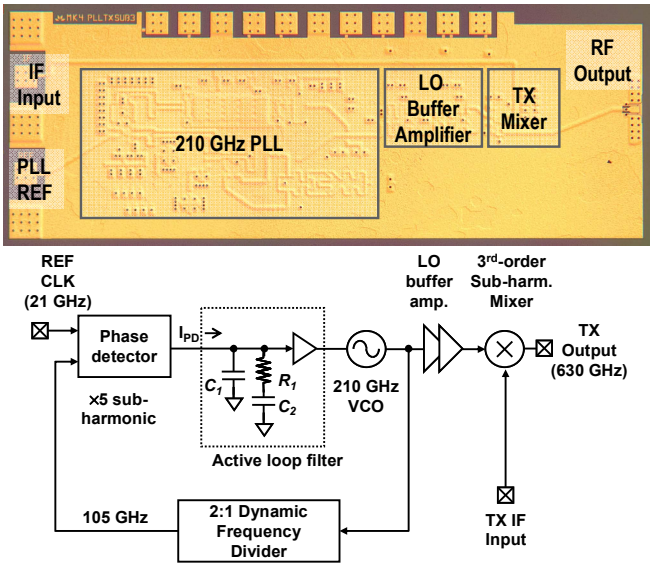

Fig. 1. 630 GHz single-chip transmitter (TX): chip photograph (top) and block diagram (bottom). Chip size: 1,950×700 µm^2.

III. PLL-Transmitter Circuit Design

The 630 GHz transmitter consists of a 210 GHz PLL, LO buffer amplifier, and a 3rd-order sub-harmonic mixer (Fig.1). Differential topology is extensively used to make circuit operation insensitive to common-mode impedances, e.g. bias circuits and via inductance, and thus more tolerant to modeling uncertainties and errors. The differential topology also eliminates circuit losses and bandwidth reduction caused by lossy *single-ended* ac-grounds and their internal inductance.

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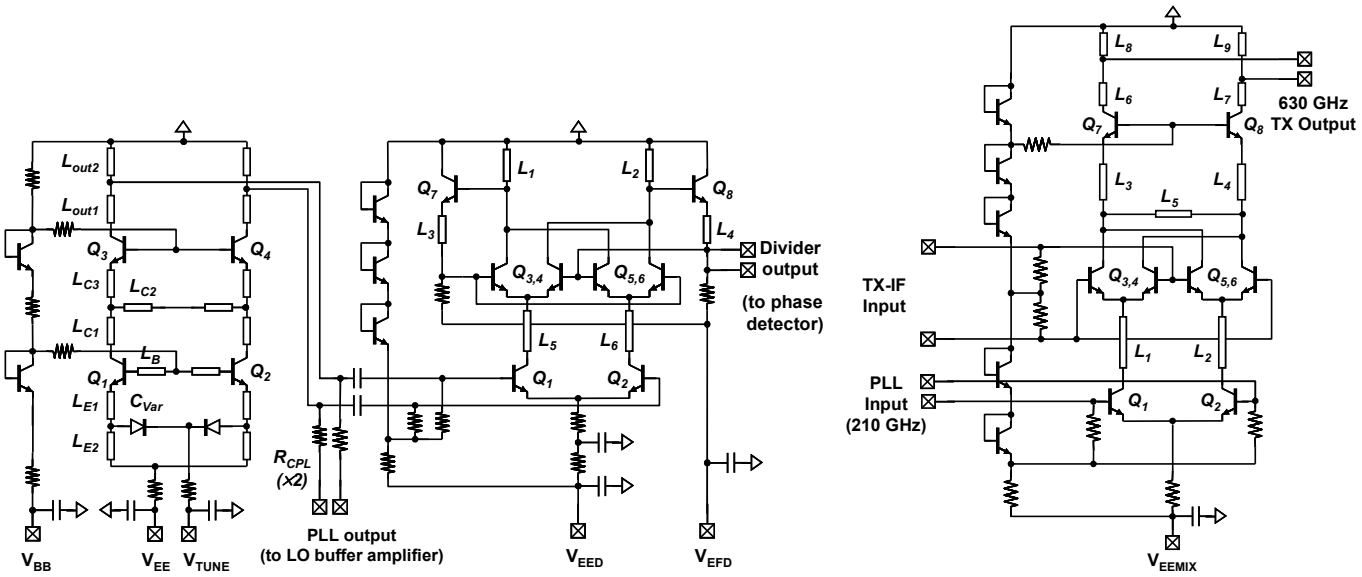

Fig. 2. Simplified schematic of the (a) 210 GHz VCO-divider chain and (b) 630 GHz 3rd-order sub-harmonic transmit mixer.

A. 210 GHz Phase-Locked Loop

In this work, a series-tuned differential VCO is used, as shown in Fig.2 (a). Q_1-Q_2 form an oscillator core, and a common-base amplifier (Q_3-Q_4) provides power gain and isolation from load perturbation. C_{VAR} is a single finger base-collector (*B-C*) junction at reverse bias with expected Q~10 at 300 GHz. The VCO provides 0 dBm of single-ended power, and tunes across 5-6 GHz, while consuming 95 mW.

The VCO output is followed by a regenerative 2:1 dynamic frequency divider (Fig. 2 (a)). The use of inductive loading (L_1-L_2) enables higher frequency operation than is possible with traditional resistive or transimpedance-stage loading (also with less voltage headroom). Simulated divider operating bandwidth is > 40 GHz centered at 210 GHz, with -20 to -10 dBm of output power, while consuming 91 mW. The VCO output is tapped by a simple 18 dB resistive coupler (R_{CPL}), and the subsequent LO buffer amplifier (2-stage differential cascode) delivers 0 dBm of LO power to the transmit mixer.

In order to perform phase comparison at a reasonably low frequency, a 5th-order sub-harmonic phase detector based on a double-balanced mixer is used, in favor of its simpler construction and lower power consumption compared to a chain of static frequency dividers. Simulation shows that the phase detector provides useful detection gain up to $N = 5$ sub-harmonic operation with -20 dBm of RF power at 105 GHz. Detector operation at $N > 5$ may suffer from increased sensitivity to detector offset voltages and may degrade PLL phase noise.

B. Sub-Harmonic Transmit Mixer

Fig.2 (b) shows the schematic of the 630 GHz transmit mixer operating in a 3rd-order sub-harmonic mode, based on a double-balanced mixer followed by a common-base (CB) stage. For the 130 nm HBT process used in this work, a CB stage exhibits higher maximum available gain than a common-emitter configuration around 600 GHz, while simplifying the biasing scheme. Transmission lines L_1 and L_2 improve impedance matching between the upper and lower differential pairs, improving conversion gain. Input and output impedance matching of the CB stage is achieved by L_3-L_5 and L_6-L_9, respectively. The mixer consumes 200 mW of dc power from a single power supply. Simulated conversion gain of the transmit mixer is -20 to -25 dB for 600-640 GHz at 0 dBm of LO power, with > 30 GHz of IF bandwidth.

All circuits are implemented using inverted microstrip lines to utilize a continuous ground plane on a top metal layer (M3).

IV. Measurement Results

The fabricated transmitter IC was characterized on-wafer using the test setup in Fig. 3. A WR-1.5 (500-750 GHz) coupler was used for simultaneous spectrum and power measurement. Its main output connects to a power meter, and the signal from the coupled output is down-converted by a WR-1.5 harmonic mixer followed by a spectrum analyzer.

Measured locking range of the 210 GHz PLL was typically 5 GHz centered around 210 GHz, yielding 15 GHz of LO tuning range (×3) at the transmitter output around 630 GHz. Typical down-converted spectrum of the transmitter output is shown in Fig. 4, where the PLL is locked at 210 GHz and f_{IF} = 100 MHz (LO feedthru is not suppressed due to single-ended testing setup). Phase noise measurement was performed by

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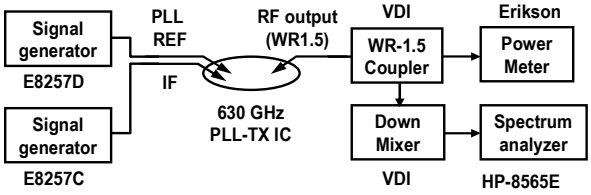

Fig. 3. PLL-Transmitter test setup.

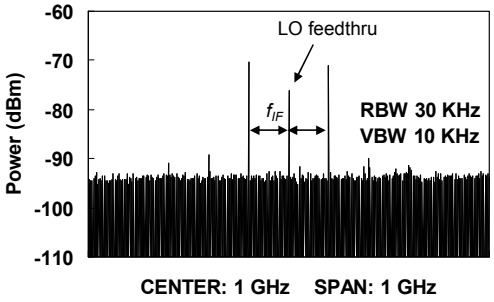

Fig. 4. Measured transmitter output spectrum after down-conversion (f_{IF} = 100 MHz).

using the spectrum analyzer built-in utility routine for offset frequencies from 10 Hz to 1 MHz (Fig. 5). Measured phase noise of the transmitter output at 630.1 GHz was -51 dBc, -65 dBc, and -74 at 100 Hz, 1 KHz, and 10 KHz of offset frequencies, respectively. Beyond a 300 KHz offset frequency, phase noise measurement is limited by additive noise from the down-conversion mixer. Transmitter IF bandwidth was measured to be > 30 GHz.

Measured transmitter saturated output power was typically between -30 to -33 dBm (Fig. 6), after de-embedding losses from the WR-1.5 probe, coupler, transition and waveguide taper (total 13.5 dB). Since the raw measured power was relative low (e.g. 20-40 nW), a modulated test setup was used to improve measurement accuracy in the presence of random measurement drifts: transmitter power supplies are periodically switched on and off, while the power meter read-out is digitized and subsequently demodulated by separately averaging on- and off-period measurements. If the modulation period is chosen sufficiently short, measurement drifts will be averaged out. Note measured output power in Fig. 6 is from a single-ended RF output.

The transmitter IC consumes 650 mW of dc power, where the PLL and transmit mixer dissipate 450 mW and 200 mW, respectively.

VII. Conclusion

A 630 GHz InP HBT transmitter with phase-locked local oscillator is presented, aimed toward highly integrated THz radio systems. Further characterization is under way, as well as design efforts to integrate amplifiers for higher output power.

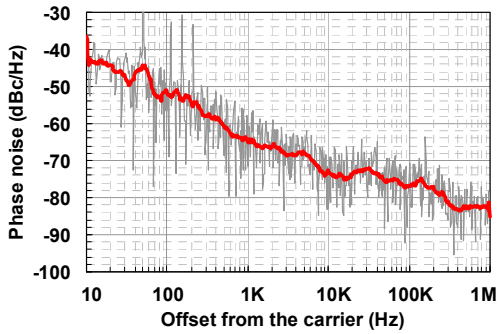

Fig. 5. Measured phase noise of the transmitter output at 630.1 GHz (f_{IF} = 100 MHz).

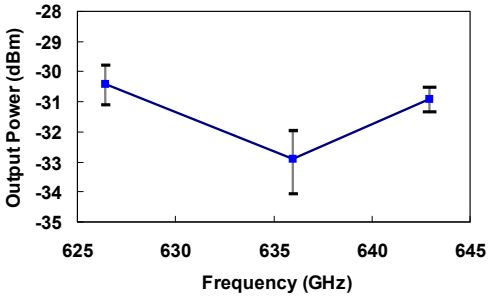

Fig. 6. Measured saturated transmitter output power with f_{IF} = 100 MHz and P_{IF} = -6 dBm (error bars with ±1 are also shown).

Acknowledgement

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