Over 200GHz Static Frequency Dividers in 250nm InP HBT

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Through appropriate latch design using a 250nm InP HBT technology, static frequency dividers operating in excess of 200GHz have been realized [1,2]. We present a static divide-by-8 frequency divider with a maximum clock frequency of 204.8GHz, utilizing 250nm InP HBTs (400GHz f_τ, 650GHz f_{max}) and a 4-metal layer interconnect, inverted thin-film microstrip wiring environment. The divider is static to 4.0GHz operation. Emitter-coupled-logic forms the divider latches to minimize gate delays for highest divider clock rates. The power dissipation is 1.82W, of which 592mW is consumed by the input-stage divider. The circuit contains 108 HBTs and its size is 0.68×0.45-mm^2.

InP based double heterojunction bipolar transistors (DHBT) have been aggressively researched and pursued because of their superior material transport properties compared to its SiGe counterpart. At a given scaling generation, InP devices have increased values of small-signal unity current gain f_τ and unity power gain f_{max}. The gate delay of a digital IC however is not determined by an algebraic function of f_τ and f_{max}, but instead by a set of time constants of which $C_{cb}\Delta V_{logic}/I_c$ and $C_{cb}R_{bb}$ are majority contributors. The parasitic voltage drop $I{\cdot}R_{ex}$ across the switching differential pairs must be considered as well, as it may consume a significant fraction of ΔV_{logic}. For a given technology, the maximum clock rate of a static frequency divider is used as a digital benchmark circuit as it reflects the highest data rate a latch may support. To increase the toggle-rates to 200GHz for this circuit, the HBT has been laterally scaled to 250nm [3,4] to reduce C_{cb} and support higher J_e (fig. 2), done simultaneously with reductions to the HBT resistances R_{ex} and R_{bb}, as well as forming the IC with reduced signal path lengths.

The circuit consists of a master-slave flip-flop with the output cross-coupled to the input to generate $f_{clk}/2$ frequency division of the clock signal (fig. 3). Two-stages of output signal buffering are used to minimize capacitive loading on the flip-flop signal bus. To form the divide-by-8 output, three dividers are cascaded together (fig. 3). All flip-flops employ single-buffered emitter-coupled-logic (ECL). Bias currents are established using pull-down resistors to avoid capacitive loading that would exist from using HBT current mirror biasing. For the input-stage divider only, the collector terminal of emitter-followers Q1-Q2 may be biased to $V_{CC} > 0V$ to minimize their base-collector capacitance C_{cb} and reduce signal delays. The first divider (stage-1) is composed of 4μm HBTs for Q1-Q4, and 6μm HBTs for Q5-Q6. The signal bus switching paths are only 50μm in length (located at the center of the IC) – doubly terminated with 50Ω and 22pH peaking inductance. The logic swing ΔV_{logic} is 300mV. Figure 4 shows the variation of HBT C_{cb} with J_e and V_{cb}, along with the operating endpoints for HBTs Q1-Q6 in the flip-flop. Figure 5 shows the current switching behavior for a differential pair, where the differential voltage is normalized to kT/q. For an HBT junction temperature increase $\Delta T \sim 60°C$ and $kT/q \sim 30mV$, to switch 95% of current I_o to one side of differential pair Q3-Q4 ($I_oR_{ex} = 3kT/q$ trace, fig. 5), $\Delta V_{logic,minimum} \sim 180mV$ is required. To account for ΔT and R_{ex} variation, 120mV of margin was designed into the logic swing. An IC micrograph of the fabricated static divide-by-8 frequency divider is shown in figure 1.

Divide-by-8 measurements for clock frequencies spanning the divider limits were performed, where the clock signal is presented single-ended (50Ω input matched) to the circuit and an input clock DC voltage offset of -450mV (Q5, fig. 4) is required. The bias voltage for all stages (dividers and buffers) is $V_{EE} = -3.8V$ ($I_{EE,total} = 463mA$). V_{CC} (Q1-Q2) for the input divider is 500mV, and the bias current for an input-stage latch $I_{EE,latch} = 70mA$. The entire divide-by-8 power dissipation is 1.82W, where 592mW is from the input divider (no output buffers). All measurements were performed at ~ 25°C and at identical biases for the frequencies tested. The divider was clocked to 4.0GHz (P_{clk} = 9.0mW) to show it is fully static. The maximum clock rate achieved was 204.8GHz (P_{clk} = 17mW). Divider input clock sensitivity measurements were performed and are summarized in figure 6. The meta-stable, source-free self-oscillation (circuit biased, no clock signal) referenced to the clock input was 143GHz.

A fully static divide-by-8 frequency divider having a record maximum clock frequency of 204.8GHz has been demonstrated in a 250nm InP HBT technology, supported by a low-loss, 4-metal interconnect wiring environment. The scaling of the HBT from 500nm to 250nm features, combined with reductions to the HBT parasitic contact resistances, and aggressive scaling of the circuit signal path lengths are responsible for the increased divider clock rates past 200GHz. Table-I provides a summary to date of state-of-the-art results reported for static frequency dividers.

[1] Z. Griffith et al.,*Proc. IEEE Compound Semiconductor IC Symposium*, Monterey, CA, Oct. 3-6, 2010.
[2] M. D'Amore et al., *Proc. IEEE Compound Semiconductor IC Symposium*, Greensboro, NC, Oct. 11-14, 2009.
[3] J. Hacker et al., *Proc. IEEE International Microwave Symposium*, Anaheim, CA, May 23-28, 2010.
[4] Z. Griffith et al., *Proc. IEEE/LEOS Indium Phosphide and Related Materials*, Matsue, Japan, May 14-18, 2007.

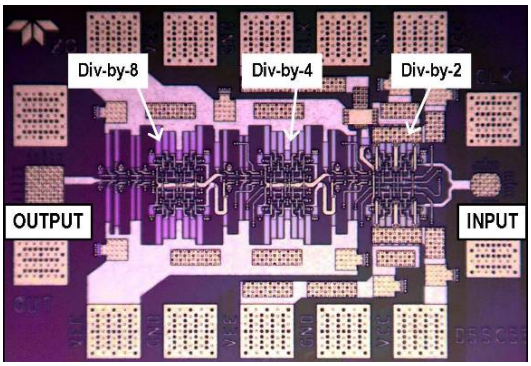

Fig. 1. IC micrograph of the static divide-by-8 frequency divider (prior to top-most metal deposition). Die area, 0.68×0.45mm^2

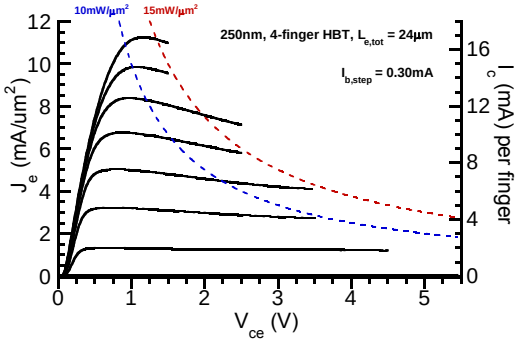

Fig. 2. Common-emitter characteristics – 4-finger, 250nm × 6um HBT.

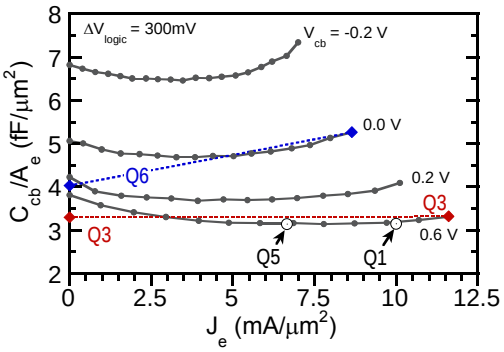

Fig. 4. Variation of C_{cb} with J_e and V_{cb} bias, labeled to show the device switching endpoints within the divider (Fig 3).

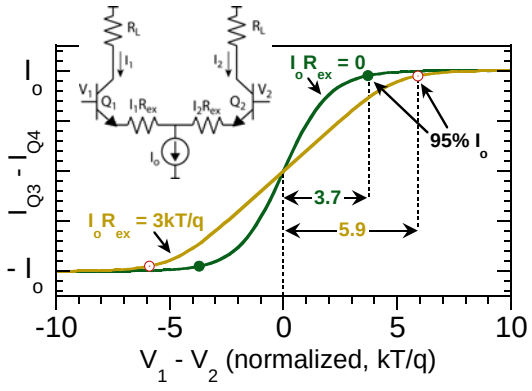

Fig. 5. Current flow of a differential-pair in the presence of emitter resistance. $V_1 - V_2$ is normalized to kT/q. The $I_oR_{ex} = 3kT/q$ trace reflects the current switching nature of HBTs Q3, Q4 in the divider (fig. 3). $\Delta T \sim 60°C$, $kT/q \sim 30mV$, $\Delta V_{logic} = 300mV$

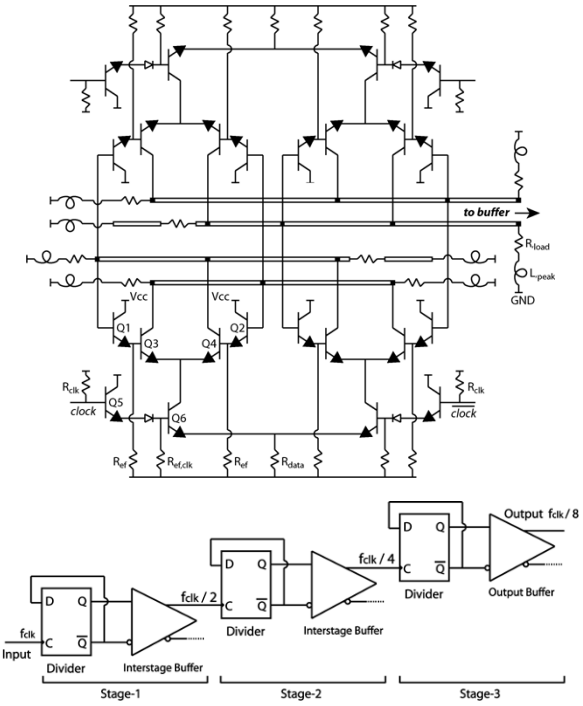

Fig. 3. Circuit schematic of the emitter-coupled-logic (ECL) flip-flop configured as a static divide-by-2, and a block diagram showing how they are configured to form a static divide-by-8.

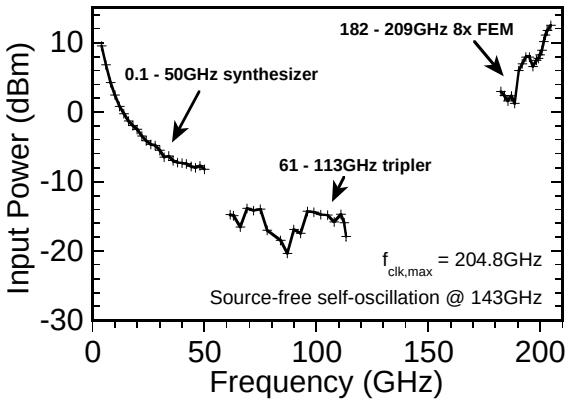

Fig. 6. Input sensitivity with frequency for the 204.8GHz static divide-by-8 frequency divider.

Max. Clock Freq. (GHz)	Division Rate	Technology	Scale (nm)	Reference
110	4	SiGe HBT	140	Infinion
151.6	4	InP HBT	400	HRL
152.0	2	InP HBT	500	Teledyne
152	4	InP HBT	500	Lucent
200.6	2	InP HBT	250	NGAS [2]
204.8	8	InP HBT	250	Teledyne [1]

Table 1. Summary of the fastest reported static frequency dividers.