High Performance Substitutional-Gate MOSFETs Using MBE Source-Drain Regrowth and Scaled Gate Oxides

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***Abstract* — We report high transconductance MOSFETs with scaled dielectric (1.2 nm EOT) fabricated using a substitutional-gate process with MBE source/drain regrowth. A 50 nm-L_g and 1.2 nm EOT device shows 0.8 mA/μm on-current at V_{gs}-V_{th} = 0.8 V and V_{ds} = 0.5 V and 1.0 mS/μm peak transconductance at V_{ds} = 0.5 V which are 25% and 40% higher than those of a 1.65 nm EOT control device, respectively. Transmission line method (TLM) measurements indicate 0.8 Ohm-μm^2 metal-semiconductor contact resistivity and 18 Ohm sheet resistance of the regrown N+ source-drain contact layer.**

I. Introduction

Due to the low transport mass in $In_{1-x}Ga_xAs$-based materials, InGaAs MOSFETs can provide higher on-state current and transconductance than reference Si channel devices [1]-[3], given low dielectric interface trap density (D_{it}) [4] and low source/drain access resistivity [5]. According to FET scaling laws [5], high on-current and integration density in scaled devices requires the following: (1) low source/drain contact and access resistivities, (2) heavily-doped source and drain regions for adequate carrier supply (3) low D_{it}, and (4) small equivalent oxide thickness (EOT) and thin channel layers for high channel charge density

Thin gate dielectrics are critical not only for proper FET electrostatics at a short gate length but also for high on-current and transconductance. Considering gate-channel capacitances (Fig. 1), given a 7.5 nm thick channel, and estimating D_{it} as $5{\cdot}10^{12}$/cm^2, we calculate from ballistic transport theory that reducing the EOT from 1.65 nm (3.3/1.5 nm Al_2O_3/HfO_2) to 1.16 nm (1.1/4.0 nm Al_2O_3/HfO_2) should increase the 2D electron density (N_s) by ~15%. In the absence of S/D resistance, the thinner dielectric should increase current density and transconductance ~25%. Here we report a high-transconductance (1.0 mS/μm peak transconductance at V_{ds} = 0.5 V) device with a scaled 1.16 nm EOT dielectric, fabricated using a substitutional-gate scheme and using MBE source-drain regrowth.

II. Device Fabrication

The epitaxial layers, grown by MBE, has a InP (100) semi-insulating (S. I.) substrate, a 400 nm unintentionally doped (UID) $In_{0.52}Al_{0.48}As$ buffer/barrier layer, a 3 nm Si-doped ($6.0{\cdot}10^{12}$ /cm^2) $In_{0.52}Al_{0.48}As$ pulse doping layer, a 1 nm UID

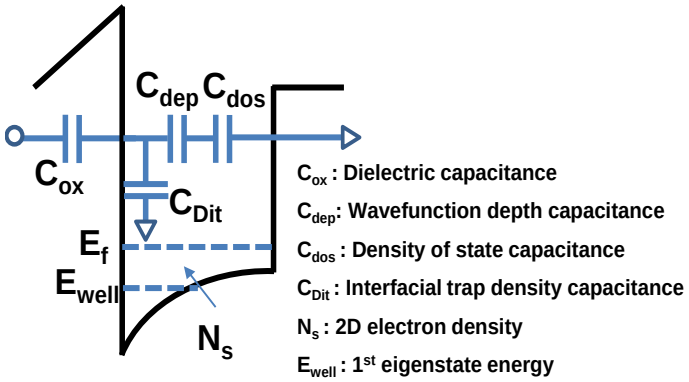

Fig. 1. Circuit model of QW-MOSFET electrostatics.

$In_{0.52}Al_{0.48}As$ setback layer, and a 2 nm $In_{0.53}Ga_{0.47}As$ / 2.5 nm InAs / 3 nm $In_{0.53}Ga_{0.47}As$ composite channel. Fig. 2 summarizes the process flow. 300 nm of SiO_2 as a dummy gate and 20 nm of Cr as a hard mask were deposited by PECVD and e-beam evaporation, respectively. A Cr hard mask was pattern by e-beam lithography and inductively coupled plasma (ICP) dry etching, and subsequently SiO_2 was dry-etched by ICP using the patterned Cr hard mask. The Cr hard mask was then removed by photo resist planarization [7]. Prior to loading into the MBE chamber, the semiconductor surface was oxidized by exposure to UV ozone and subsequently etched in 10:1 DI H_2O:HCl. Approximately 60 nm of Si doped ($5\text{-}10{\cdot}10^{19}$ /cm^3) InAs was non-selectively grown on the sample. Amorphous InAs on top of the dummy gate was then removed by photo resist planarization [7]. The sample was wet-etched to form device mesas. The SiO_2 dummy gate was then removed using a buffered oxide etch and a few drops of Tergitol as a surfactant. Prior to gate dielectric deposition, native oxide on the channel was removed in dilute HCl. Using atomic layer deposition (ALD), 3.3 nm Al_2O_3 and 1.5 nm HfO_2 (1.65 nm EOT) were deposited on the control sample and 1.1 nm Al_2O_3 and 4.0 nm HfO_2 (1.16 nm EOT) deposited on the experimental sample. The samples were then annealed at 400 ℃ for 1 hour in forming gas. Approximately 80 nm of Ni was thermally deposited as the gate electrode. Finally, 20 nm Ti / 20 nm Pd / 130 nm Au was lifted off for source/drain metallization by e-beam evaporation. The schematic cross-section of the device is shown in Fig. 3.

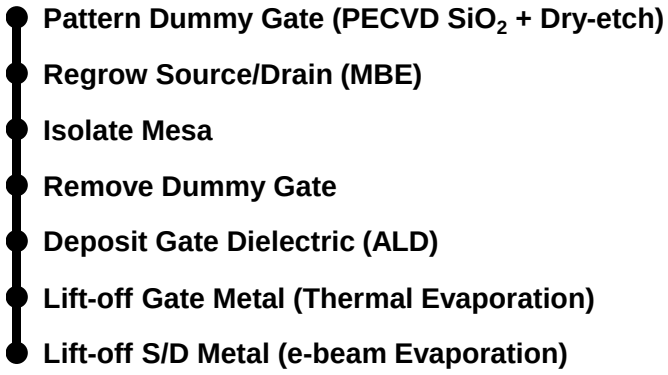

Fig. 2. Process flow.

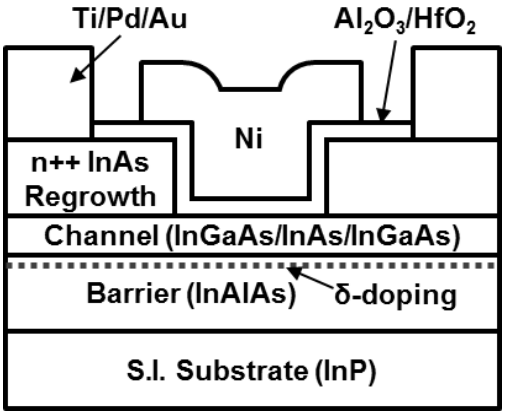

Fig. 3. Schematic cross-section of the substitutional-gate MOSFET.

III. Results and Discussion

Fig. 3 compares transfer characteristics (I_d-V_{gs} and g_m-V_{gs}) for a 50 nm-L_g (as drawn) device with 1.65 nm EOT (control sample) and a 50 nm-L_g (as drawn) device with 1.2 nm EOT (experimental sample). Threshold voltages extracted from linear extrapolation of the I_d-V_{gs} characteristics are ~0.4 V for the 1.65 nm EOT sample and ~0 V for the 1.16 nm EOT sample. The peak transconductance of the 1.16 nm EOT device is approximately 1.0 mS/μm at V_{ds} = 0.5 V which is approximately 40 % larger than that of the 1.65 nm EOT control. As shown in Fig. 4, the 1.16 nm EOT device shows approximately 0.8 mA/μm on-current at V_{gs}-V_{th} = 0.8 V and V_{ds} = 0.5 V, a bias at which impact ionization does significantly increase I_{on} , outperforming the 1.65 nm EOT control device by 25%. Fig. 5 shows log(I_d)-V_d plots of the 50 nm-L_g devices. The 1.65 nm EOT control and 1.16 nm EOT experimental samples both show ~200 mV/dec sub-threshold swing (SS) at V_{ds} = 0.1 V, which results both from short channel effects, back barrier leakage, and D_{it}. Approximately 60 mV hysteresis is observed near the V_{th}. Subthreshold characteristics of 200 nm-L_g devices are represented in Fig. 7.

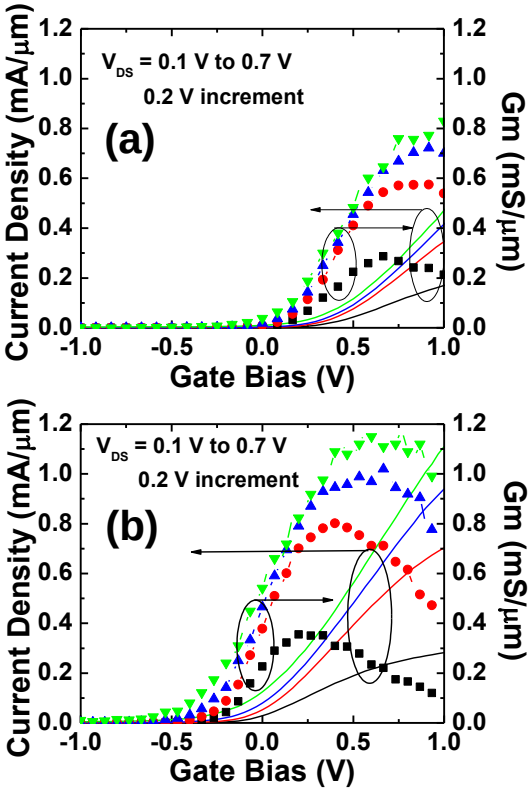

Fig. 4. Transfer (I_d-V_{gs} and g_m-V_{gs}) characteristics for a 50 nm-L_g device with 3.3/1.5 nm Al_2O_3/HfO_2 (a) and a 50 nm-L_g device with 1.1/4.0 nm Al_2O_3/HfO_2 (b)

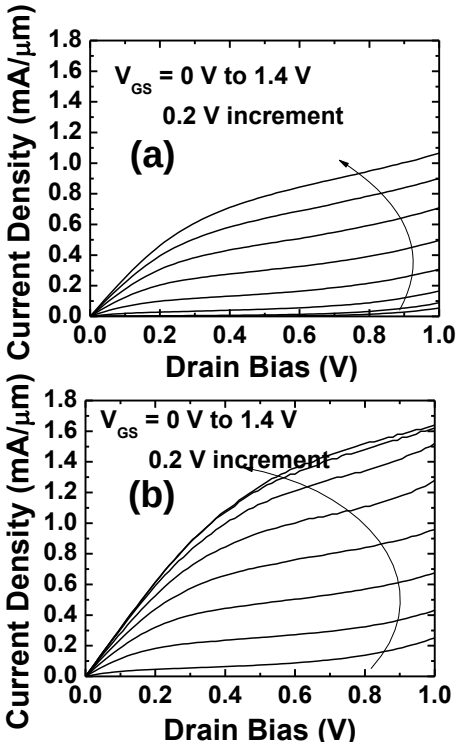

Fig. 5. Output (I_d-V_{ds}) characteristics for a 50 nm-L_g device with 3.3/1.5 nm Al_2O_3/HfO_2 (a) and a 50 nm-L_g device with 1.1/4.0 nm Al_2O_3/HfO_2 (b)

Devices show a minimum SS of ~170 mV/dec for the 1.65 nm EOT control device and ~130 mV/dec for the 1.16 nm EOT experimental device, respectively. Fig. 8 shows the gate leakage current for both cases. At gate biases larger than 0.3 Volts, the 1.16 nm EOT device shows smaller gate leakage current than the 1.65 nm EOT device. This is a consequence of the thinner dielectric. However, for both samples the gate leakage current is negligible, <10 nA/μm at all gate biases.

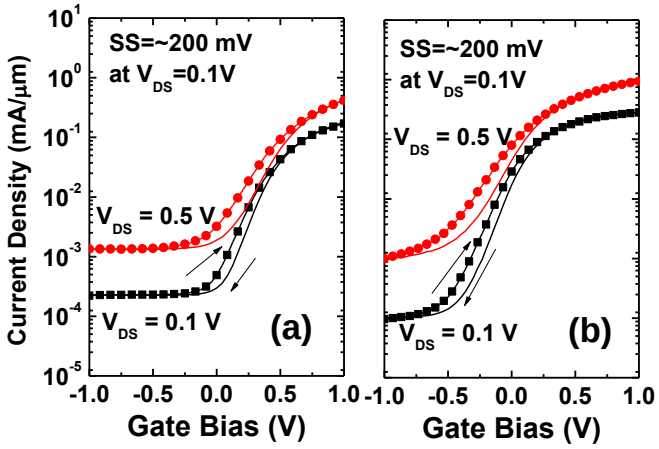

Fig. 6. Sub-threshold (log(I_d)-V_{gs}) characteristics for a 50 nm-L_g device with 3.3/1.5 nm Al_2O_3/HfO_2 (a) and a 50 nm-L_g device with 1.1/4.0 nm Al_2O_3/HfO_2 (b). Solid lines and lines with symbols represent forward and reverse sweeps, respectively.

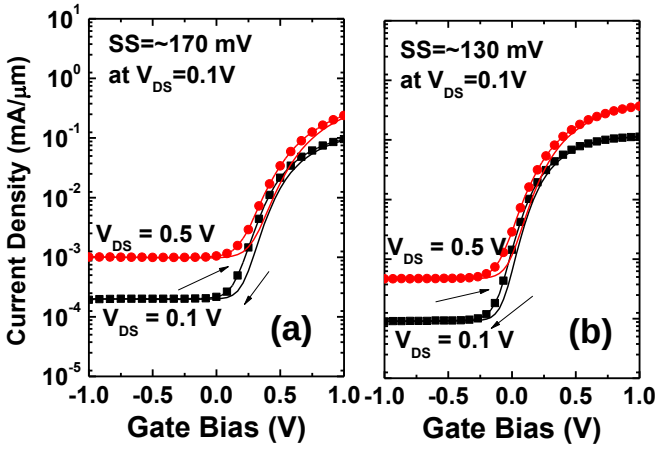

Fig. 7. Sub-threshold (log(I_d)-V_{gs}) characteristics for a 200 nm-L_g device with 3.3/1.5 nm Al_2O_3/HfO_2 (a) and a 200 nm-L_g device with 1.1/4.0 nm Al_2O_3/HfO_2 (b). Solid lines and lines with symbols represent forward and reverse sweeps, respectively.

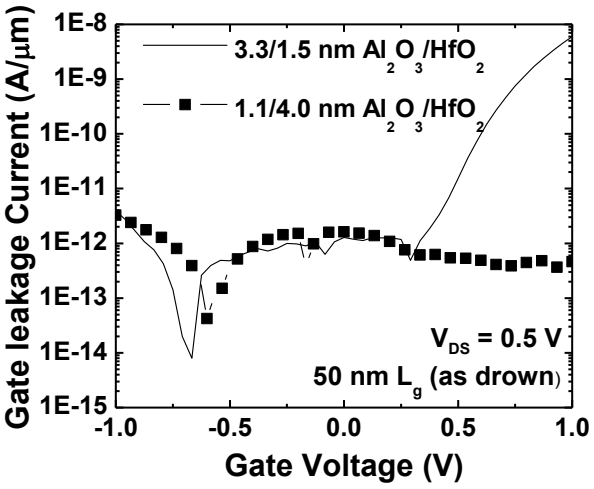

Fig. 8. Gate leakage current for both a 50 nm-*Lg* device with 3.3/1.5 nm Al_2O_3/HfO_2 (Solid line) and a 50 nm-*Lg* device with 1.1/4.0 nm Al_2O_3/HfO_2 (Square)

Fig. 9 shows transmission line method (TLM) measurement data for n++ InAs regrown source-drain, from which 0.8 Ohm-μm^2 of metal-semiconductor contact resistivity and 18 Ohm of sheet resistance are determined, respectively.

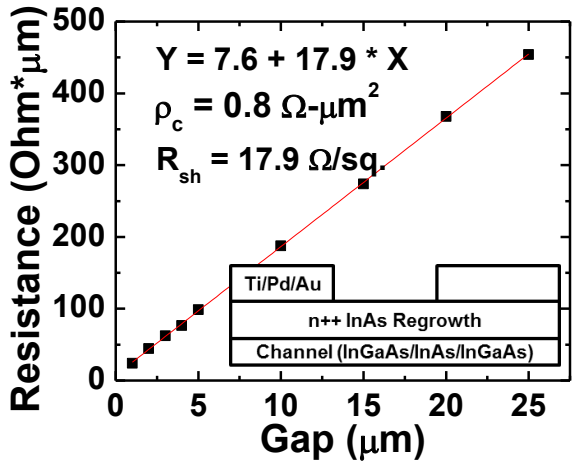

Fig. 9. Transmission line method (TLM) measurement of the n++ regrown source-drain layer. The metal-to-semiconductor contact resistivity and sheet resistance are 0.8 Ohm-μm^2 and 17.9 Ohm/square, respectively.

IV. Conclusion

We have demonstrated high transconductance III-V MOSFETs with scaled gate dielectric using substitutional–gate scheme and MBE source drain regrowth technique. An experimental sample with 1.1/4.0 nm Al_2O_3/HfO_2 shows 1.0 mS/μm peak transcondance at V_{ds} = 0.5 V and 0.8 mA/μm on-current at V_{gs}-V_{th} = 0.8 V and V_{ds} = 0.5 V.

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