High Performance Substitutional-Gate MOSFETs Using MBE Source-Drain Regrowth and Scaled Gate Oxides

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2012 Conference on Indium Phosphide and Related Materials
UCSB, Santa Barbara, CA
08/28/2012

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Outline

- Motivation: Why III-V MOSFETs?
- Key Design Considerations

  - Process : Gate-last
  - Channel Design : Composite channel
  - Gate dielectric

- Process Flow
- Measurement Results

  - I-V Characteristics
  - Gate leakage and TLM measurement

- Conclusion

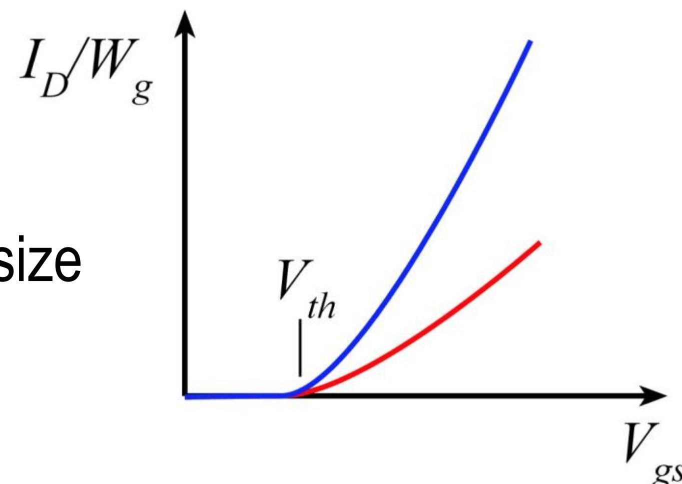
Why III-V MOSFETs in VLSI ?

more transconductance per gate width

more current→ speed

or reduced V_{dd} → reduced power

or reduced FET widths→ reduced IC size



increased transconductance from:

low mass→ high velocities

lower density of states→ less scattering

higher mobility in N+ regions → lower access resistance

Other advantages

strong heterojunctions→ carrier confinement

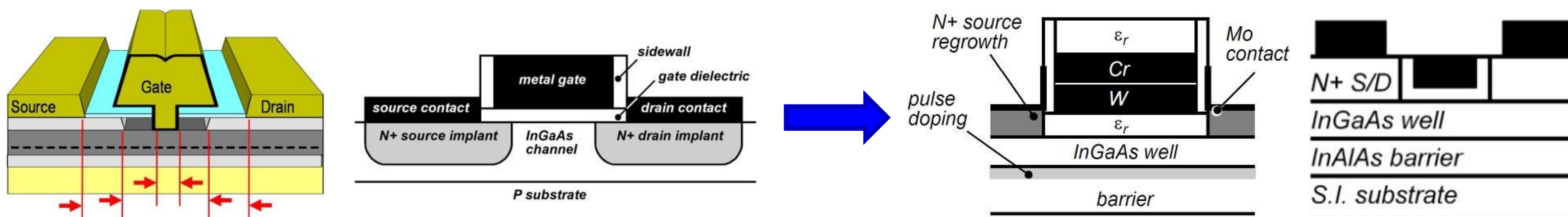
wide range of available materials

epitaxy→ atomic layer control

Key Design Considerations

Process:

Scalability (~10 nm-L_g,<30 nm contact pitch) : self-aligned S/D, very low ρ_c [2)]
Carrier supply: heavily doped N+ source region[3)]
Shallow junction: regrown S/D[3)] or Trench-gate



Channel Design:

Thinner wavefunction depth: Thin channel, less pulse doping.
More density of state: L-vally transport channel[4)]
Higher injection velocity: high In-content channel [5)]

Gate Dielectric:

Thinner EOT : scaled high-k dielectric
Low D_{it} : surface passivation[6)], reduced damage process[7)]

1) M. Wistey et al. EMC 2009; 2) A. Baraskar et al. IPRM 2010 ; 3) U. Singisetti et at. EDL 2009 ; 4) M. Rodwell et at., DRC 2010
5) S. Lee et al. EDL 2012 (accepted); 6) A. Carter et at. APEX 2011; 7) G. Burek, et al, JVST 2011.

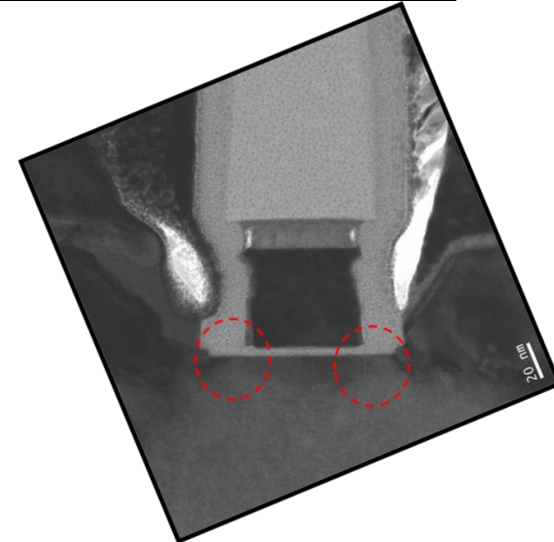
Process : Why Gate-Last process?

Gate-First

Fully self-aligned transistor at nm dimensions

Process damage during gate stack definition

Large ungated region: High pulse doing
➔ Large leakage current and Decrease C_{depth}

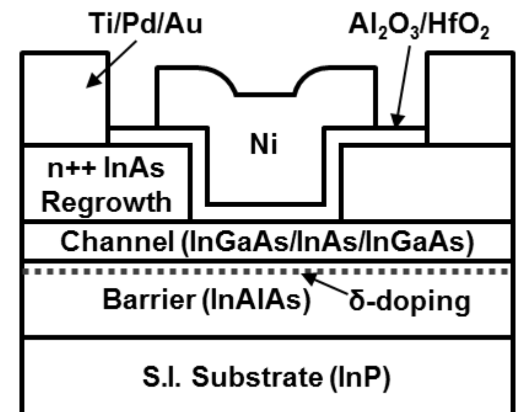


A. Carter et at., DRC 2011

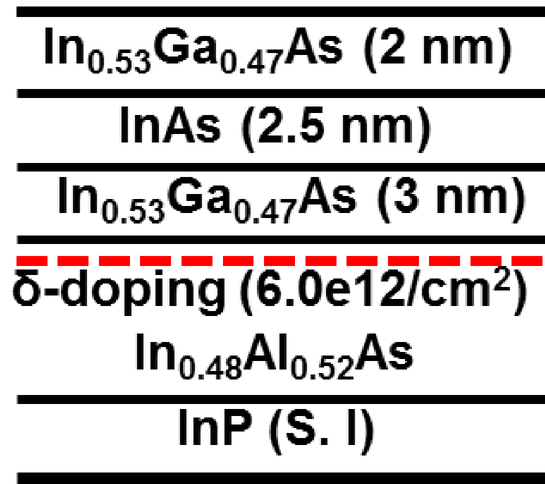
Gate-Last

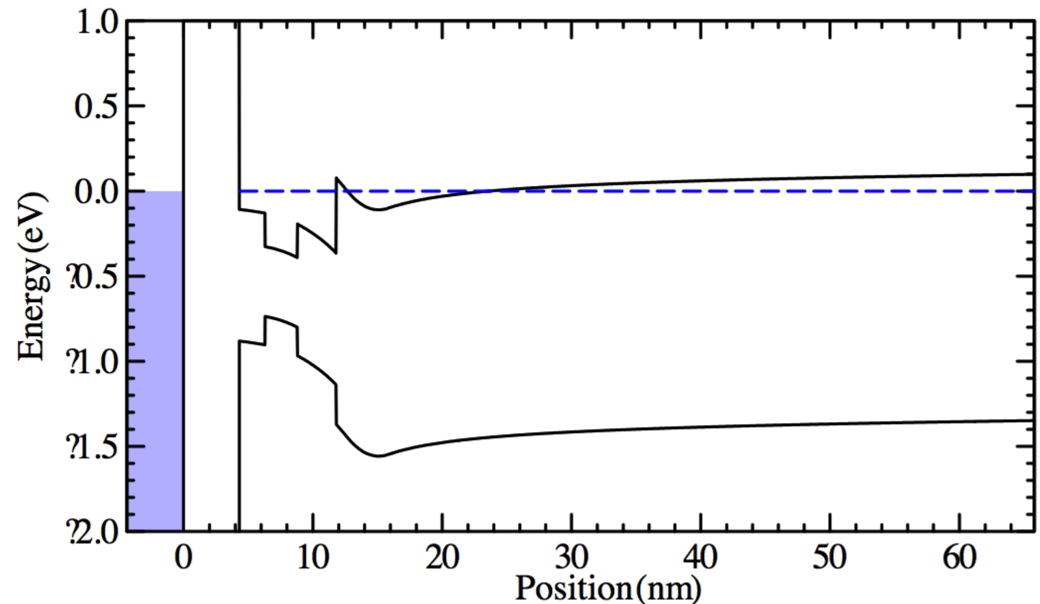
Low-damage process: Thermal gate metal,
No Plasma process after gate dielectric deposition

Rapid turn-around ➔ rapid learning.



Channel Design: Composite Channel





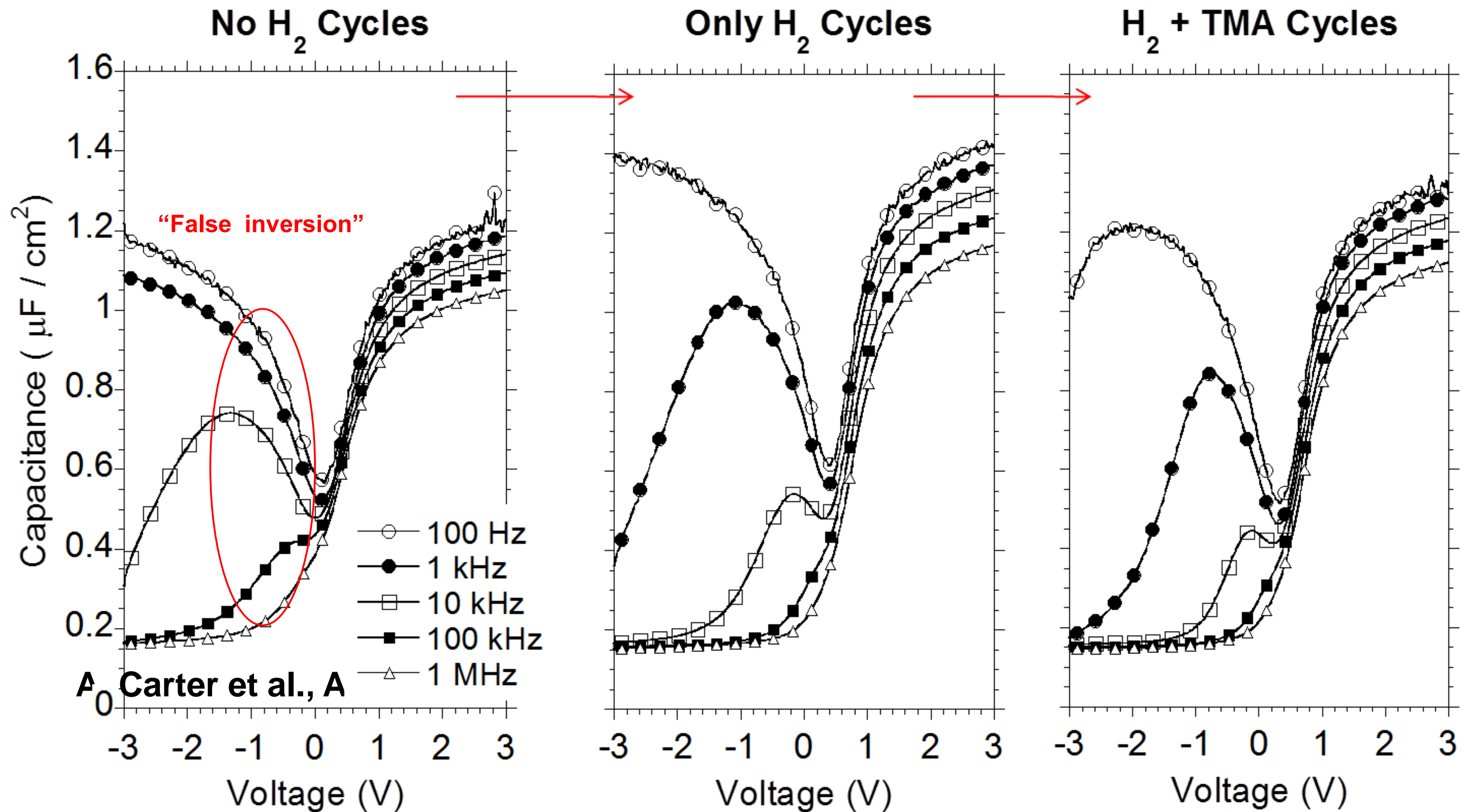
S. Lee et al. EDL 2012

Average In-content high → Source-to-channel hetero-barrier suppressed

Mean depth of wave function → reduce surface scattering

Lower bound state m* → higher injection velocity

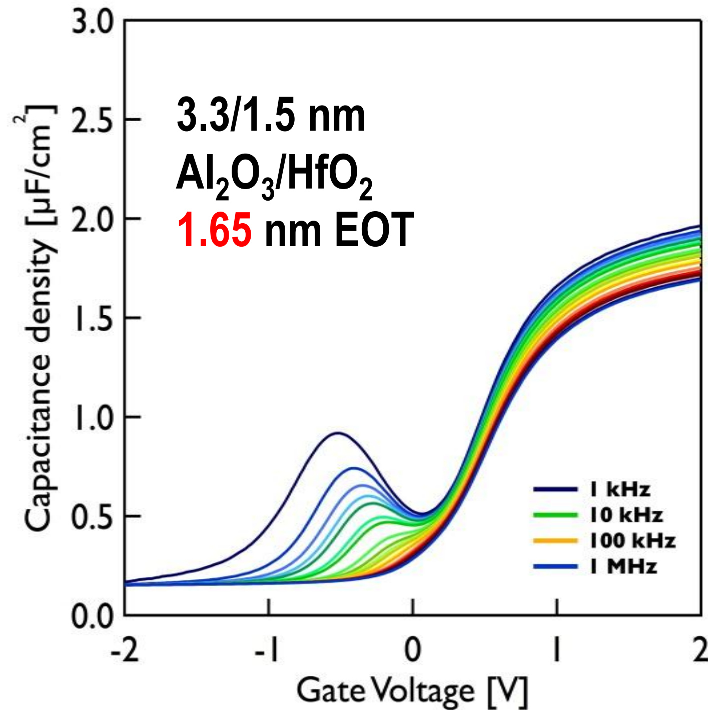
Gate Dielectric : D_{it} Passivation

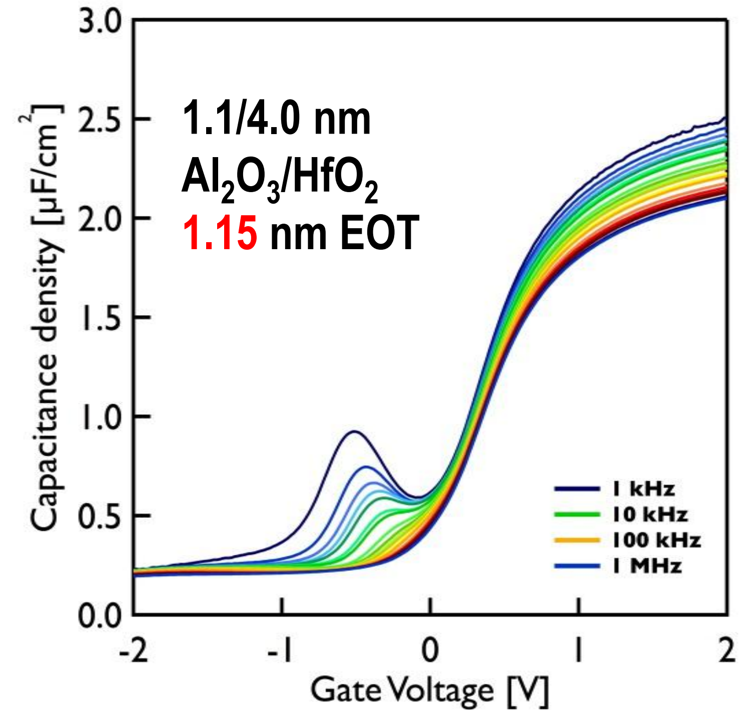


Cyclic hydrogen plasma / TMA treatments before dielectric growth → 50 cycle (~5 nm Al_2O_3) growth, 400°C anneal, Ni metallization

A. Carter et al., APEX 2012

Gate Dielectric : Dielectric Scaling





Using H_2+TMA+H_2 treatment and Al_2O_3/HfO_2 bilayer

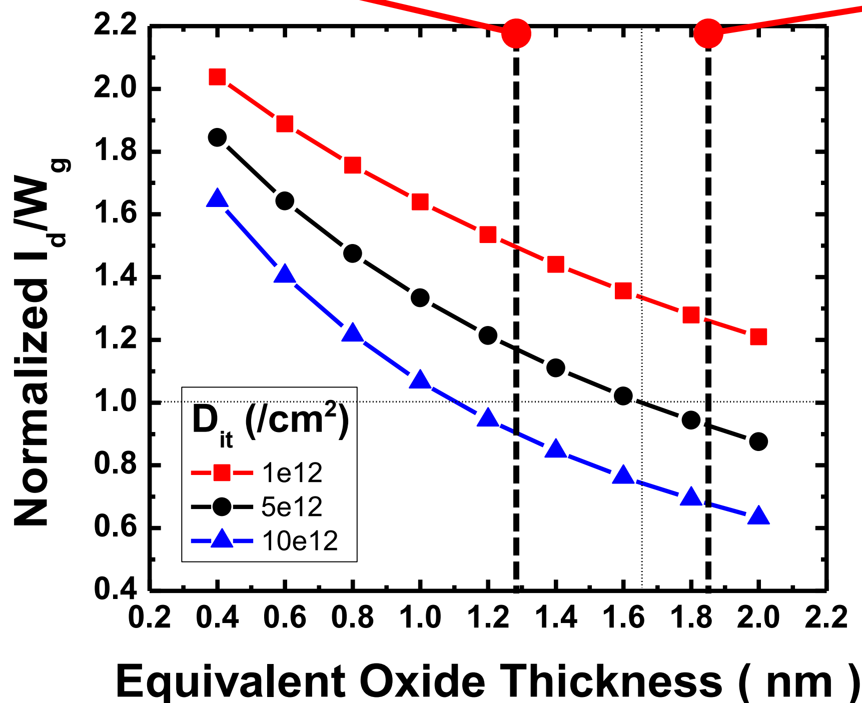
~40% Thinner EOT with similar dispersion

Courtesy of Gift in Stemmer's Group

Gate Dielectric : Calculation for Dielectric scaling

1.1/4.0 nm Al_2O_3/HfO_2(Experimental)
1.15 nm EOT

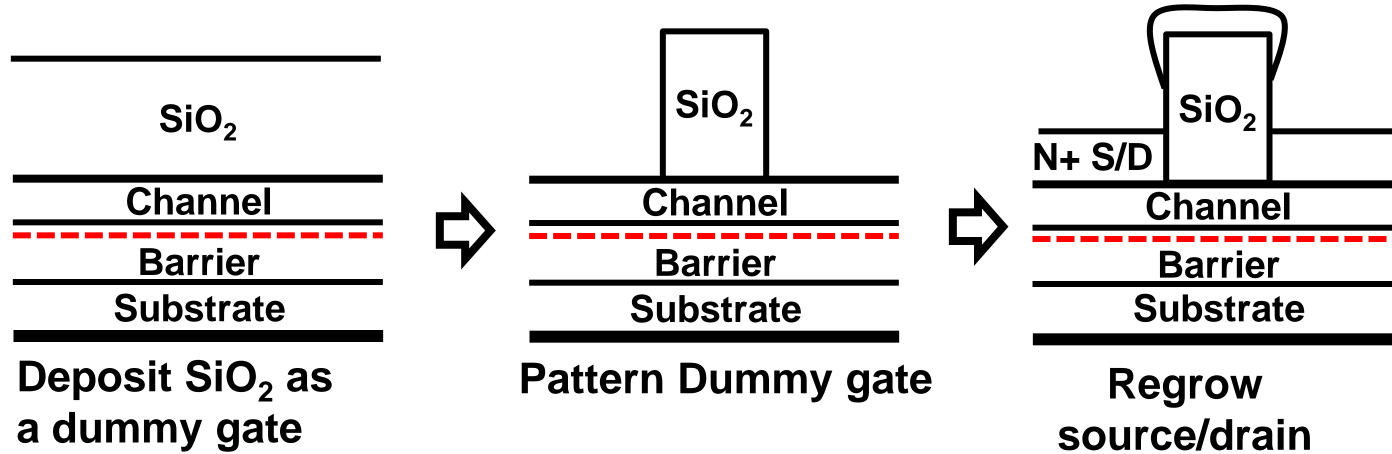
3.3/1.5 nm Al_2O_3/HfO_2(Control)
1.65 nm EOT

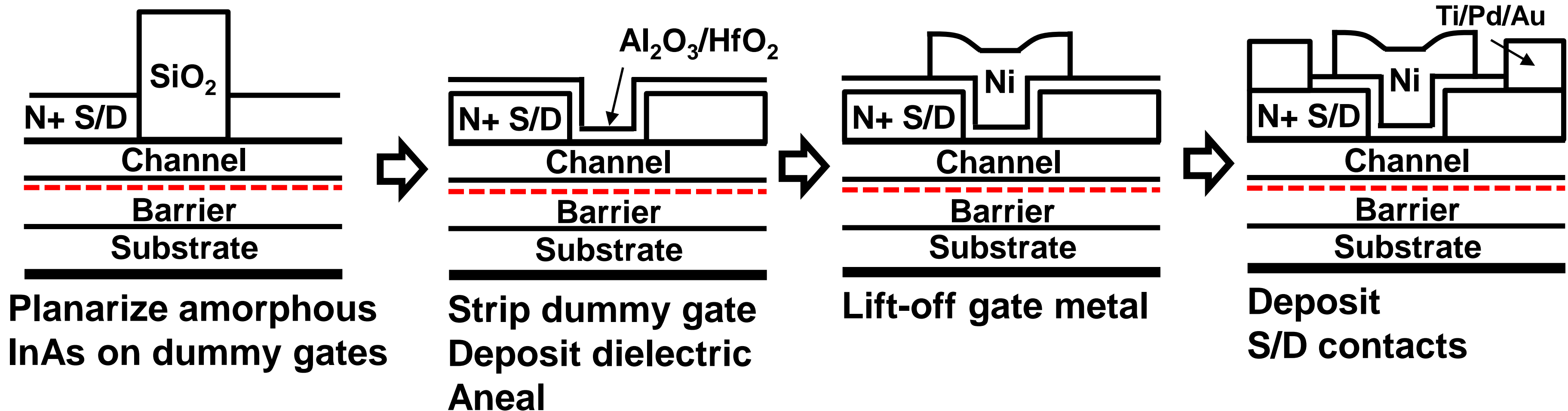


Assuming Ballistic FETs in the limit of degenerate carrier concentrations.

Given a 7.5 nm channel, reducing 1.65 nm to 1.15 nm EOT
→ ~25% increase in I_d/W_g

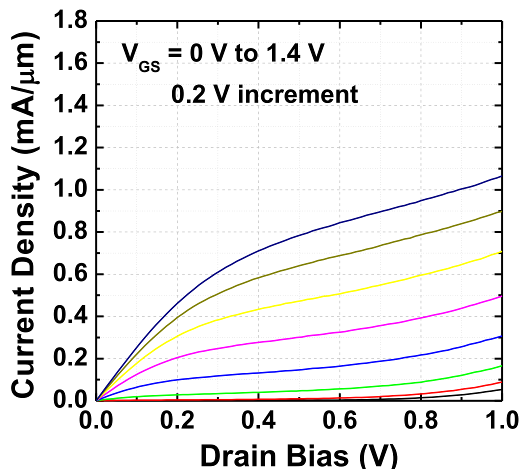
Process Flow

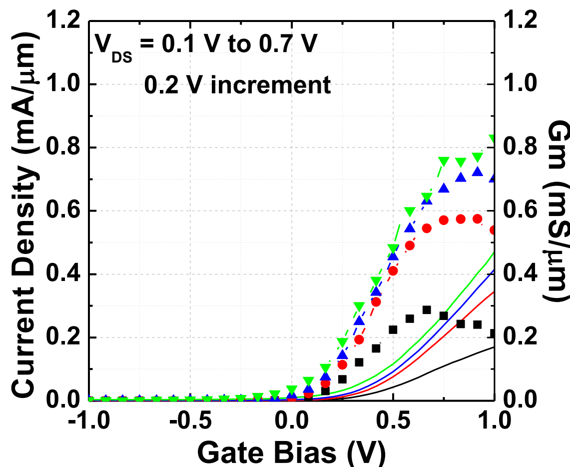


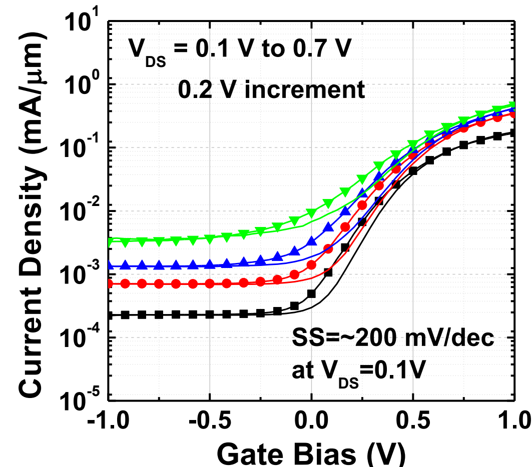


Measurement : I-V Curves for 50 nm-L_g devices

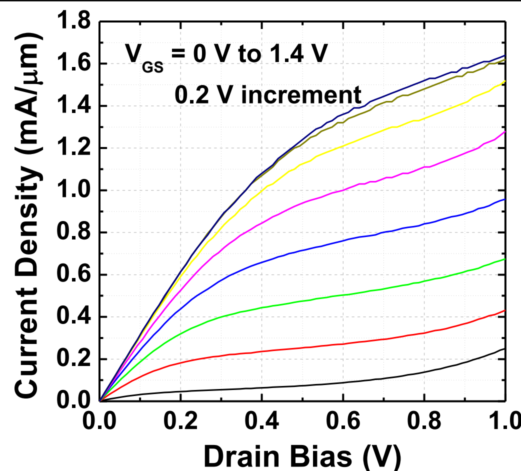
Control : 3.3 nm Al_2O_3 / 1.5 nm HfO_2 (1.65 nm EOT), 50 nm-Lg (as drawn)

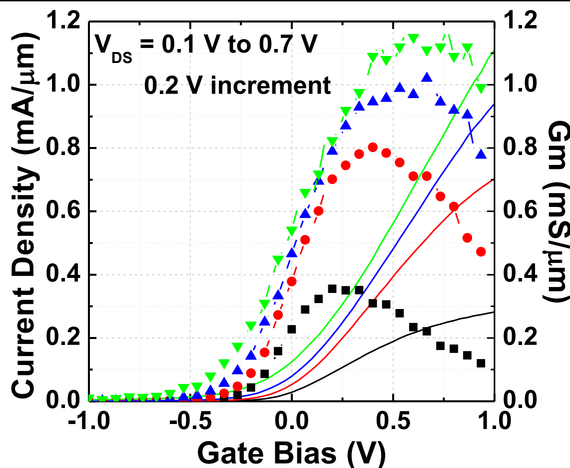


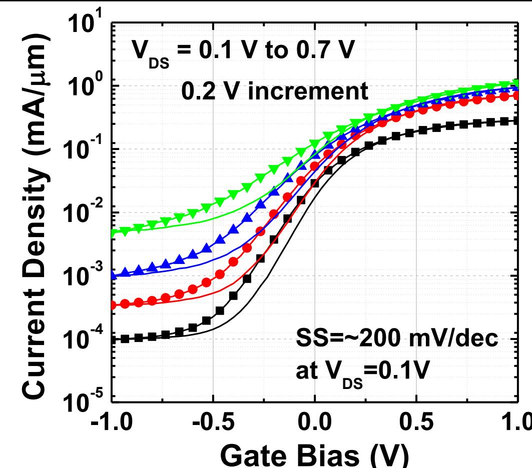




Experimental : 1.1 nm Al_2O_3 / 4.0 nm HfO_2 (1.15 nm EOT) , 50 nm-Lg (as drawn)





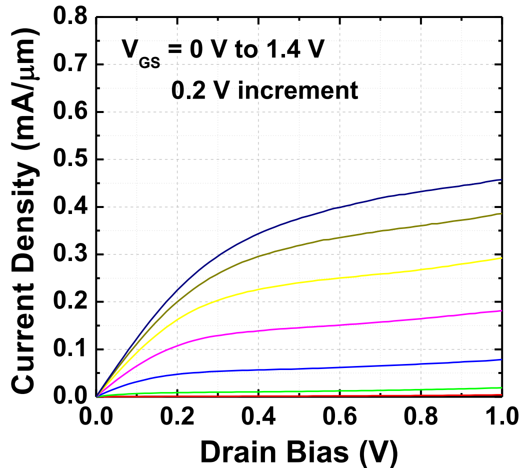


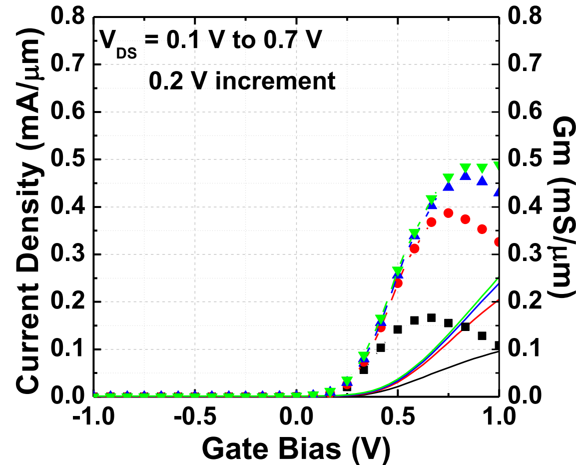
1.0 mS/μm at V_{ds} = 0.5 V : ~40% increase in transconductance.

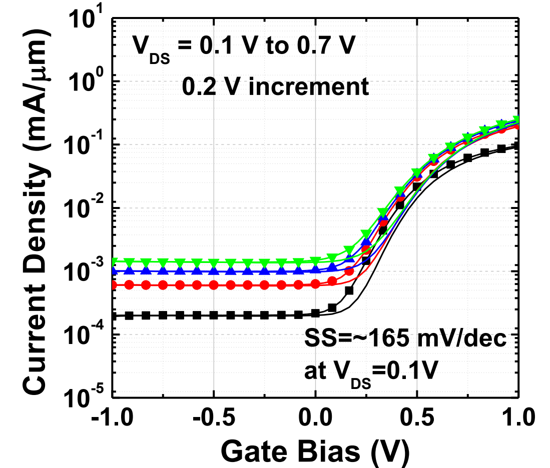
0.8 mA/um at V_{gs}-V_{th} =0.8 V and V_{ds}=0.5V : ~25% increase in on-current.

Measurement : I-V Curves for 200 nm-L_g devices

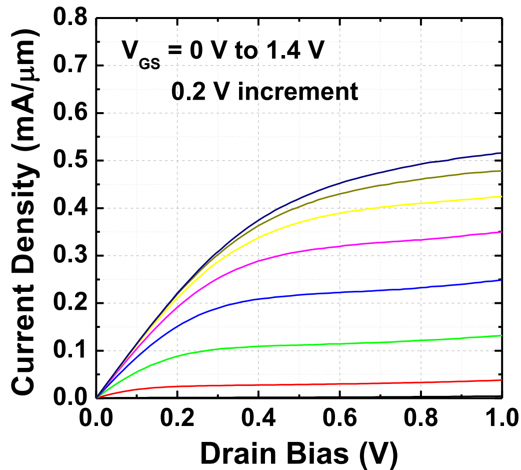
Control : 3.3 nm Al_2O_3 / 1.5 nm HfO_2 (1.65 nm EOT) , 200 nm-Lg (as drawn)

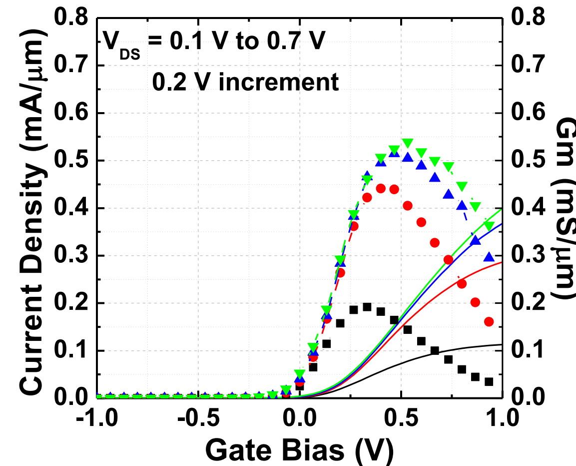


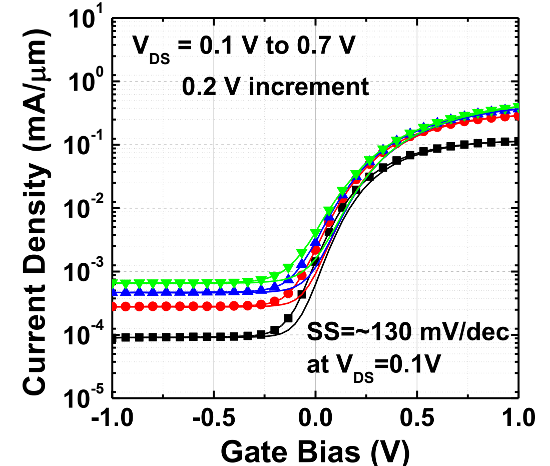




Experimental : 1.1 nm Al_2O_3 / 4.0 nm HfO_2 (1.15 nm EOT), 200 nm-Lg (as drawn)

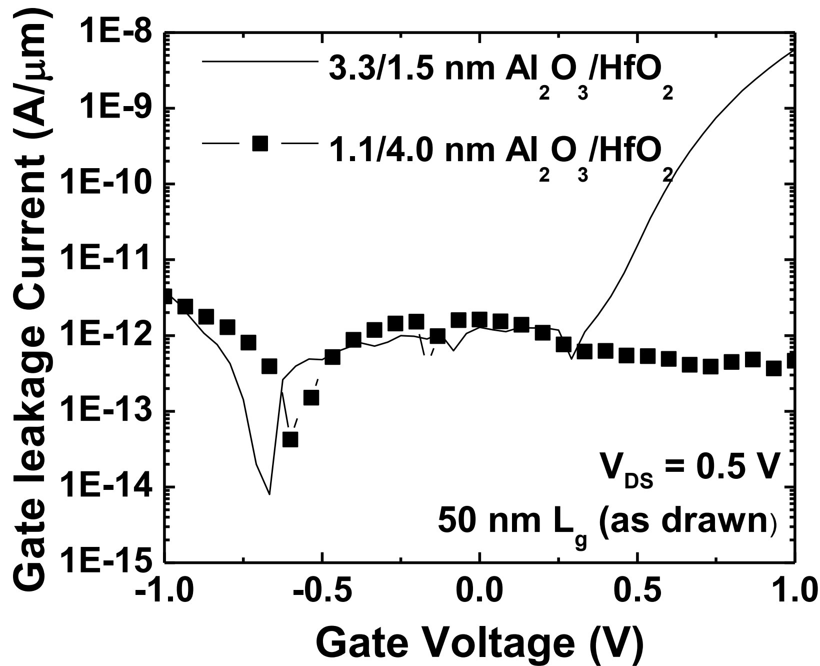


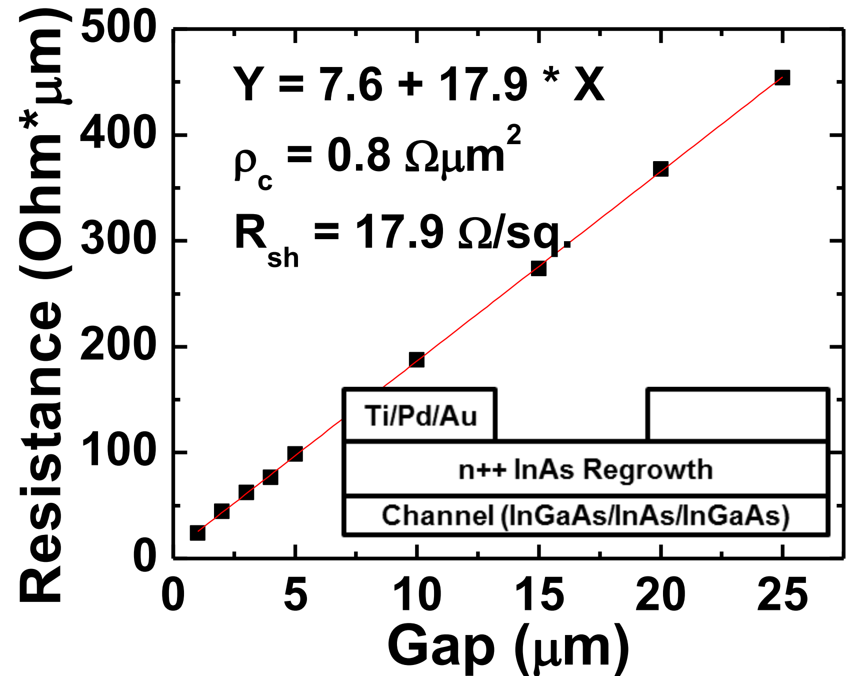




~130 mV/dec SS for 1.15 nm EOT device : D_{it} and back-barrier leakage

Measurement : Gate leakage and TLM measurement





Smaller gate leakage in 1.15 nm EOT device : slightly thick

For both cases, gate leakage <10 nA/µm at all bias range

~1.0 Ohm-µm^2 metal-semiconductor contact resistivity

~20 Ohm of sheet resistance

Conclusion

- Developed Gate-last MOSFETs using MBE S/D regrowth
- Decreasing EOT gives better performance with lower leakage
- g_m = ~ 1.0 mS/μm at V_{ds}=0.5 V for a 50 nm-L_g device
- J_d = 0.8 mA/μm at V_{gs}-V_{th} =0.8 V and V_{ds}=0.5 V for a 50 nm-L_g device
- Future work: Thinner dielectric, D_{it} passivation, and S/D leakage current

Thanks for your attention!
Questions?

This research was supported by the SRC Non-classical CMOS Research Center (Task 1437.006).
A portion of this work was done in the UCSB nanofabrication facility, part of NSF funded NNIN network and MRL Central Facilities supported by the MRSEC Program of the NSF under award No. MR05-20415.

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Device Physics : Ballistic transport

In the limit of degenerate carrier concentrations

$$I_d / W_g = q \cdot N_s \cdot \upsilon_{inj}$$

$$I_d / W_g = K(V_{gs} - V_{th})^{3/2}$$
$$g_m / W_g = K(3/2)(V_{gs} - V_{th})^{1/2}$$

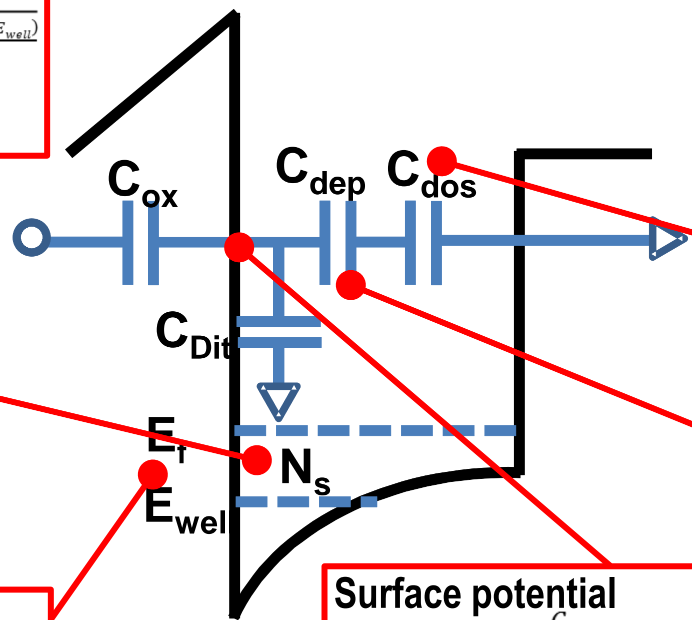
(Here, K is a function of m*, channel and dielectric thickness, and D_{it})

Injection velocity

$$\upsilon_{inj} = \sqrt{\frac{2kT}{\pi m^*}} \frac{\mathcal{F}_{1/2}\left(\frac{E_f - E_{well}}{kT}\right)}{\mathcal{F}_0\left(\frac{E_f - E_{well}}{kT}\right)}$$

Degenerate : $\frac{4}{3\pi}\sqrt{\frac{2q(E_f - E_{well})}{m^*}}$

Non-degenerate : $\sqrt{\frac{2kT}{\pi m^*}}$



Density of state capacitance

$$C_{dos} = \frac{\frac{q^2 m^*}{2\pi\hbar^2}}{1 + e^{\frac{E_{well} - Ef}{kT}}}$$

Degenerate : $\frac{q^2 m^*}{2\pi\hbar^2}$

Non-degenerate : $\frac{q^2 m^*}{2\pi\hbar^2} e^{\frac{E_f - Ewe_{ll}}{kT}}$

2DEG electron density

$$N_s = \int_{E_{well}}^{\infty} \frac{\frac{m^*}{2\pi\hbar^2}}{1 + e^{\frac{E_{well} - E_f}{kT}}} dE = \frac{m^* kT}{2\pi\hbar^2} \ln\left(1 + e^{\frac{E_f - Ewe_{ll}}{kT}}\right)$$

Degenerate : $\frac{C_{dos}}{q}(E_f - E_{well})$

Non-degenerate : $\frac{m^* kT}{2\pi\hbar^2} e^{\frac{E_f - Ewe_{ll}}{kT}} = \frac{kT}{q^2} C_{dos}$

Wavefunction depth C

$$C_{dep} = \frac{2 \cdot \varepsilon_0 \varepsilon_{channel}}{T_{channel}}$$

E_{fermi}-$E_{well\#1}$

$$(E_f - E_{well}) = \frac{C_{dep}}{C_{dep} + C_{dos}} \cdot \psi_s$$

Surface potential

$$\psi_s = \frac{C_{ox}}{C_{dit} + \left(\frac{C_{dos} \cdot C_{dep}}{C_{dos} + C_{dep}}\right) + C_{ox}} \cdot (V_{gs} - V_{th})$$