A Photonic Integrated Circuit for a 40 Gbaud/s Homodyne Receiver Using a Optical Costas Loop

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Abstract—**A highly-integrated optical Costas loop has been realized within a foodprint of 10×10 mm^2 by using a photonic integrated circuit. 40 Gbaud/s data demodulation has been achieved.**

Keywords- photonic integration, coherent receiver; Costas loop; phase-locked loop

Coherent fiber optic communication is receiving a lot of interest recently. Compared to traditional optical receivers that are used for direct detection, coherent receivers have many advantages. They have high bandwidth efficiency, are more tolerant to noise, and are compatible with different modulation formats (such as multi-level amplitude/phase shift keying) [1-2]. Most efforts focusing on long-haul and metro systems today use an intradyne approach in which a free running local oscillator (LO) laser is mixed with the incoming signal, and digital signal processing is required to track the drift in the relative phase between the LO laser and the incoming laser signal. The high-speed digital signal processors that are being used for this have very high power consumption, limited speed, and high cost. In this work, we present the 40 Gbaud/s integrated homodyne coherent receiver with a simple architecture and low power consumption.

Although considerable research on homodyne phase-locked coherent receivers has been carried out [3-4], it was proved hard to implement because of the loop delay [3,5]. As a rule of thumb, a 100 MHz open-loop bandwidth requires ~ 1 ns loop delay, which is not feasible with fiber pigtailed components or micro optics.

In this work, a highly integrated Costas loop is proposed and demonstrated. By photonic and electronic integration, the whole receiver is realized within a footprint of 10 mm × 10 mm area, and 120 ps loop delay is achieved. The architecture of the Costas loop is shown in Fig. 1. The receiver consists of three main parts: a photonic integrated circuit (PIC), and an electronic integrated circuit (EIC) and a hybrid loop filter.

The incoming signal and the LO are mixed in the optical 90 degree hybrid, and I/Q signals are generated on four photodetectors. The I/Q signals are mixed at the XOR gate on the EIC, and therefore the data-OPLL cross-talk is eliminated by the phase doubling. The XOR gate together with the delay line works as a quadric-correlator frequency detector, and the XOR itself also acts as a phase detector. The phase/frequency error signals are then fed back to the laser phase tuning section through the loop filter.

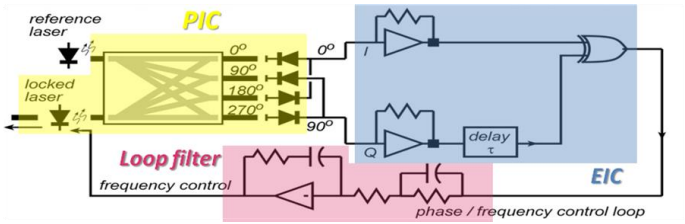

Fig. 1. The architecture of the OPLL.

On the PIC, a widely tunable sampled-grating DBR (SG-DBR) laser, a directional-coupler-based 90 degree hybrid, four uni-travelling-carrier (UTC) photodetectors and microstrip transmission lines are integrated monolithically. A centered-QW InGaAsP/InP integration platform is chosen, quantum well intermixing technology is used to define the active and passive area, and electron-beam lithography is applied to define the gratings. A blanket UTC layer regrowth and a blanket P-cladding regrowth are carried out, followed by waveguide definition using Methane/Hydrogen/Argon reactive-ion etching (RIE), and HCl-based crystallographic wet etch. This is followed by N-mesa definition and N-contact metal deposition. Helium implantation is used to isolate photodetectors. BCB is used as the dielectric for the RF transmission lines. Capacitors are also integrated for photodetector high-speed performance. After P-metal and pad metal deposition, the wafer is lapped down to 120 μm thick and cleaved. The picture and the cross sections of the fully-fabricated PIC are shown in Fig. 2 (a), (b).

The testing results show that the on-PIC SG-DBR laser can output around 30 mW power, measured by reverse biasing the boosting SOA on PIC. The tuning range is 40 nm and the threshold current is 30 mA. The UTC photodetectors have a 30 GHz 3-dB bandwidth. The measured data is shown in Fig. 3(c). There is no I/Q phase error introduced by the optical 90 degree hybrid. The four photodetectors have more than 1 mA AC current output with 4% power imbalance. The size of the PIC is 4.3 mm × 0.54 mm, and the light propagation delay is only 40 ps.

As for the EIC, four trans-impedance limiting amplifiers were integrated as the frond-end. A delay line and XOR gate are used as the phase/frequency detector for the phase locking, and also act as the mixer for recovering the carrier phase. The

loop filter is made on an AlN substrate using surface-mount components. More detailed information about EIC and the loop filter can be found in [6].

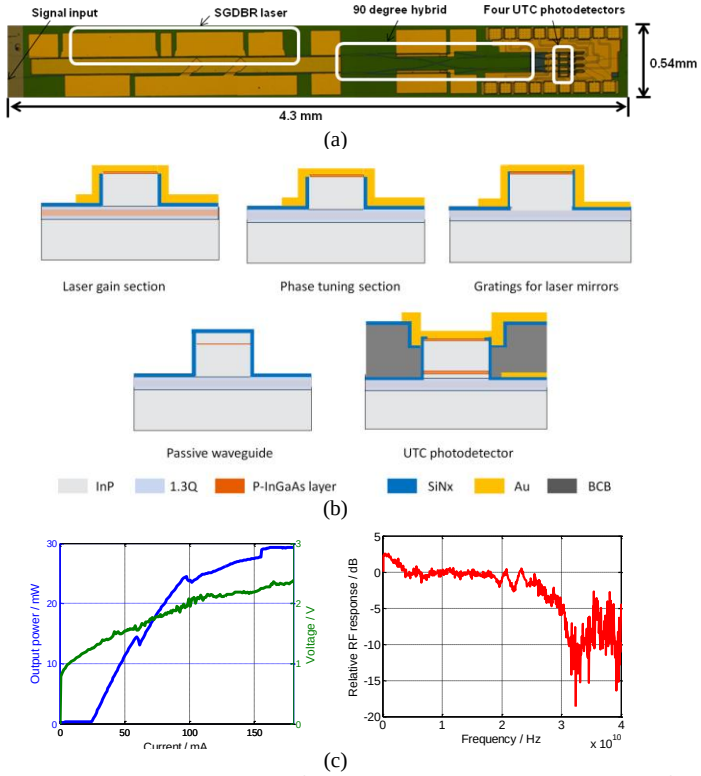

Fig.2. (a) A microscope picture of the PIC; (b) shows the cross sections of the fabricated devices. (c) L-I-V curve of the SG-DBR laser and the banwidth of the UTC photodetector.

The PIC, EIC, and loop filter are connected together using wirebonds. Because of the highly integration, a 120 ps total loop delay is achieved in this system, and the designed closed-loop bandwidth is approximately 1 GHz.

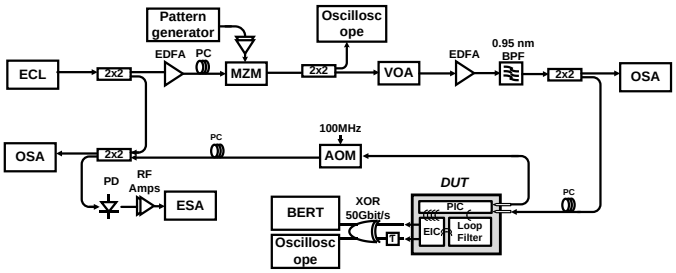

Fig. 3. The schematics of the test setup. (ECL: external-cavity laser, OSA: opitcal spectrum analyzer, ESA: electrical spectrum analyzer, MZM: Mach-Zehnder modulator, VOA: variable optical attenuator, PC: polairzation controller, AOM: acousto-optic modulator, BERT: bit error rate tester, PD: photodetector.)

The experimental setup is shown in Fig. 3. 2^{31}-1 PRBS data is applied to the transmitting laser using the NRZ BPSK format. A VOA and an EDFA are used to control the OSNR of the received signal. The BPSK signal is coupled into the PIC through a lensed fiber, and the power of the SG-DBR laser is coupled out through another lensed fiber, and beat with the transmitting laser on a high-speed photodetector for the monitoring purpose. Bit error rates (BERs) are also measured. Due to the phase ambiguity of the Costas loop, a differential decoding circuit is applied. No differential encoding circuit is used in this system simply because the differential of PRBS is PRBS itself.

We successfully locked the SG-DBR laser to the reference laser. The beating spectrum measured by the ESA showed 1.1 GHz closed-loop bandwidth. BER is also measured with various OSNR of the input signal. Error free (BER < 10^{-12}) is achieved with a data rate up to 35 Gbit/s. Both measured BER and the theoretical BER are plotted in Fig. 4, and the difference between them is mainly due to the noise figure of on-PIC SOAs and on-EIC TIAs. The power consumption of the system is around 0.5 Watt, not including the TEC cooling.

More detailed information will be presented at the conference.

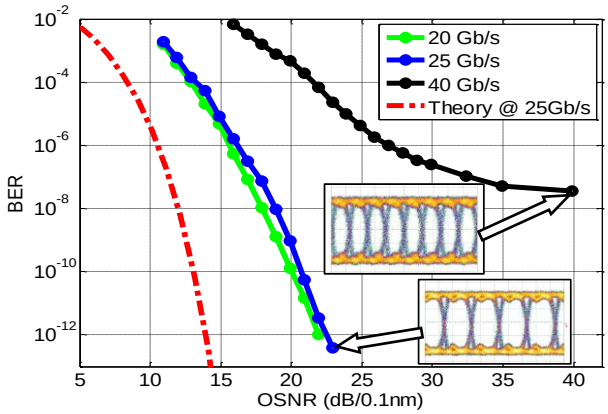

Fig. 4. BER vs. OSNR for 20 Gbit/s, 25 Gbit/s and 40 Gbit/s and the theoretical curve. Eye diagrams are also shown for 25 Gbit/s and 40 Gbit/s.

Acknowledgement

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