High-Speed Track-and-Hold Circuit Design

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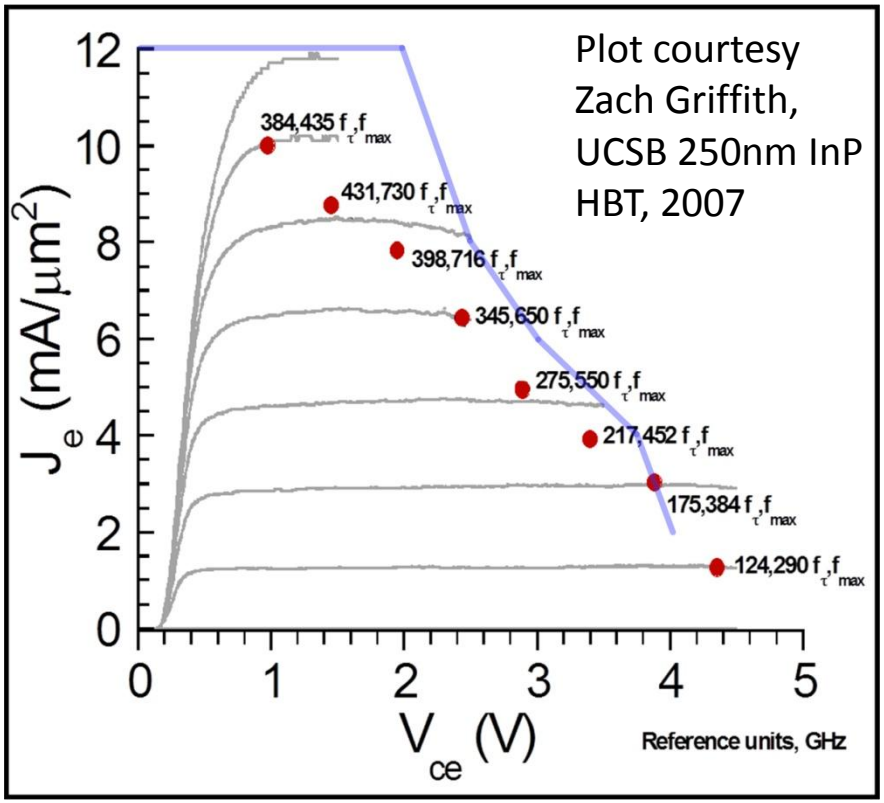
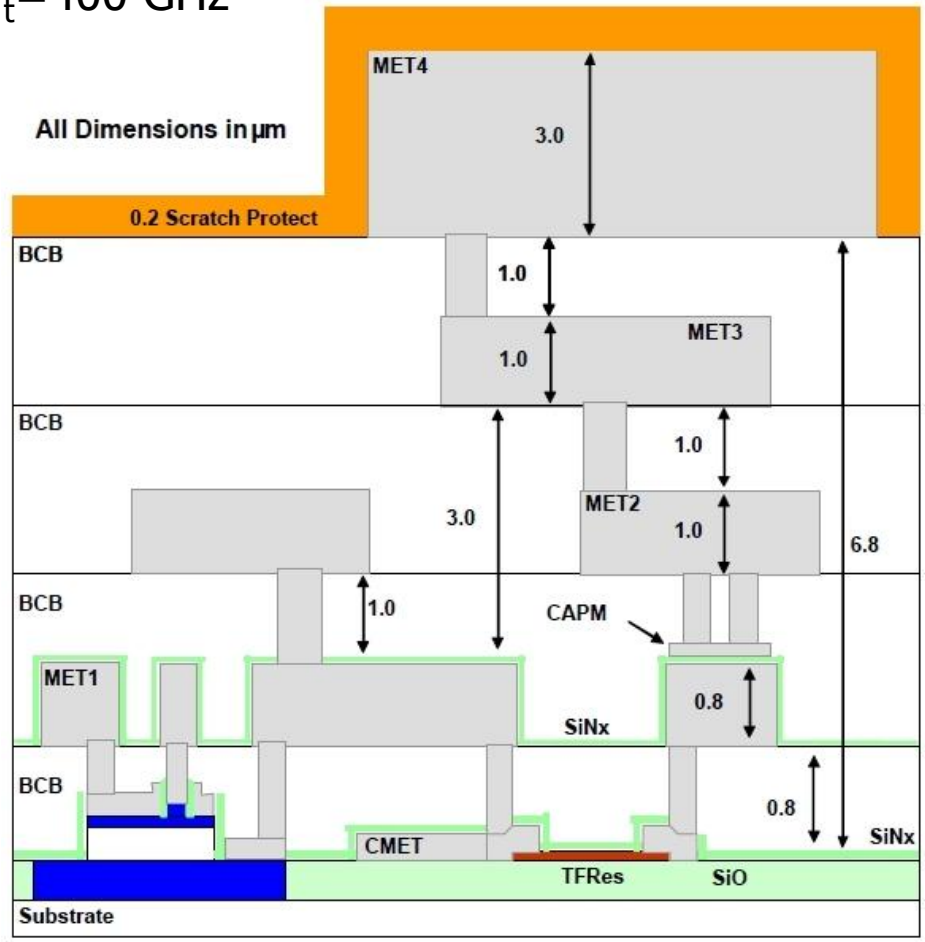
Outline

- 250 nm InP HBT technology review
- Applications and Motivation
- Key design features and contributions
- Review of circuit design and layout
- Measurement results and comparison

TSC 250nm InP HBT Process

- Four metal interconnect stack
- Peak bandwidth of f_{max} = 700 GHz & f_t=400 GHz
- MIM caps of 0.3 fF/μm^2
- Thin-film resistors 50 Ω/square



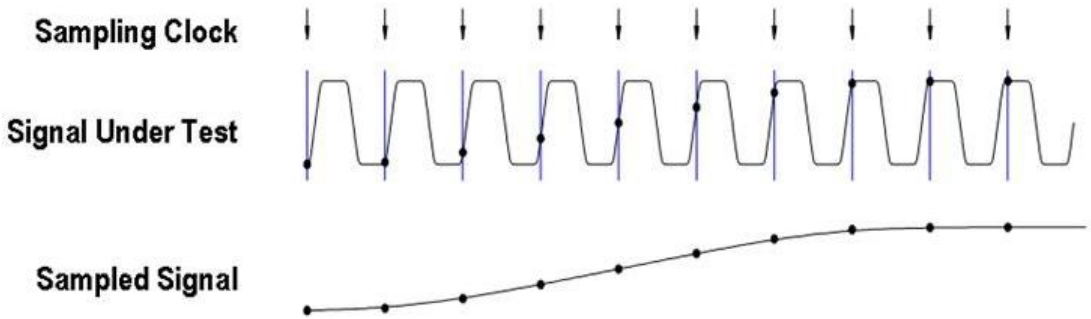


Representative cross-section of TSC250 IC technology. Drawing is not to scale.

Wideband Sample & Hold Applications

- **Sub-sampling applications:** automated test equipment (ATE), oscilloscope, jitter measurement …

Slide courtesy
MJC Teledyne



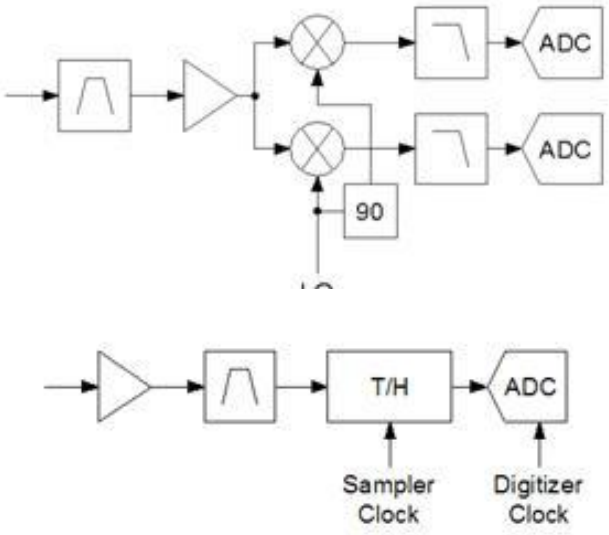
- **Undersampling applications:** undersampling receivers

Direct conversion receiver:

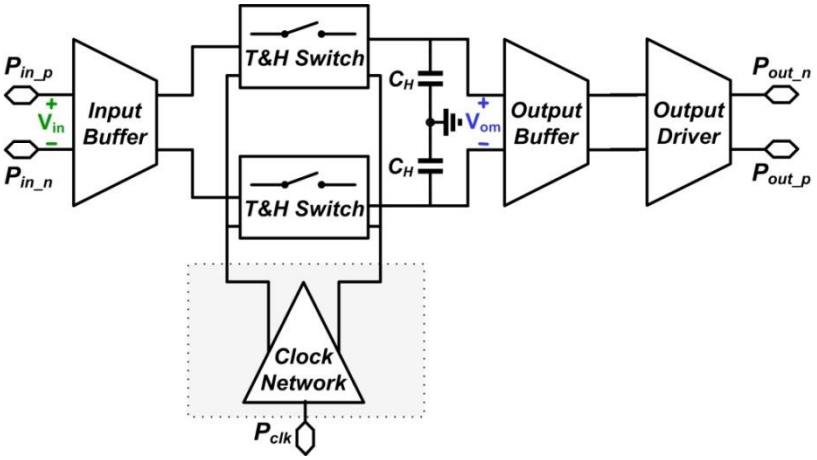
- Problems such as DC offset, noise, distortion, I/Q mismatch, etc

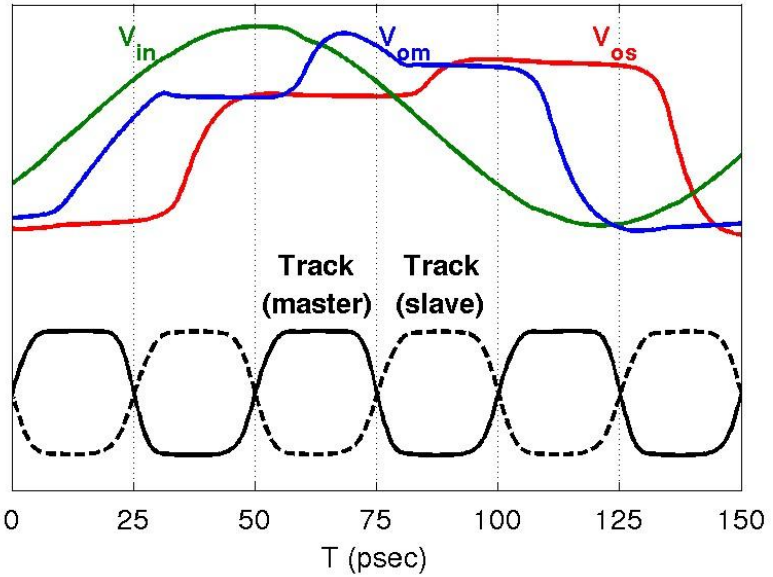
Undersampling receiver:

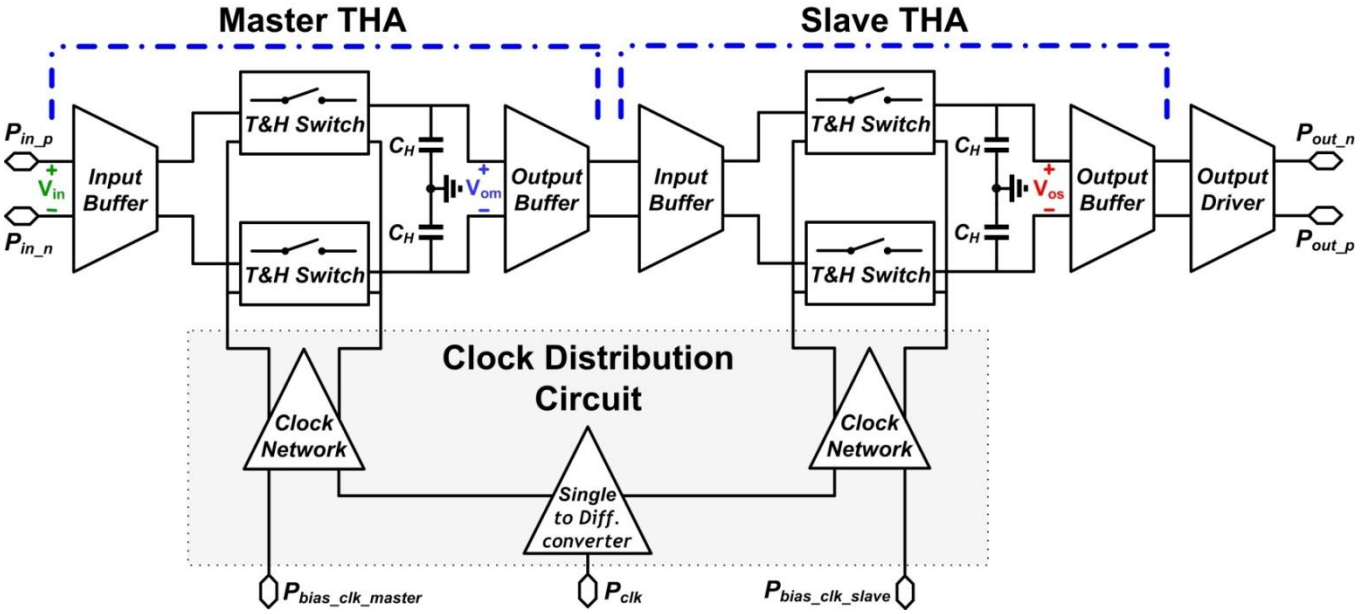
- T/H replaces downconversion mixer
- Elimintaes IF filter, IF gain stages, mixer and high frequency LO
- DC offset, IQ mismatch problem goes away
- Noise folding is a problem



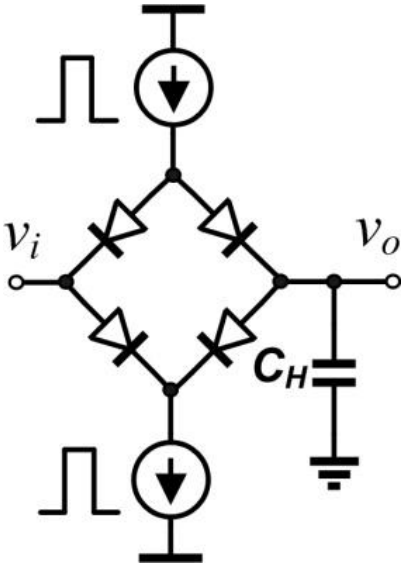
Motivation: Sample & Hold vs Track & Hold





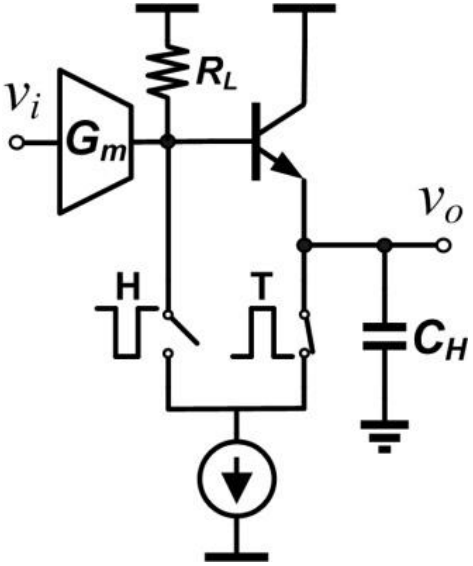


High Frequency Sampling Techniques



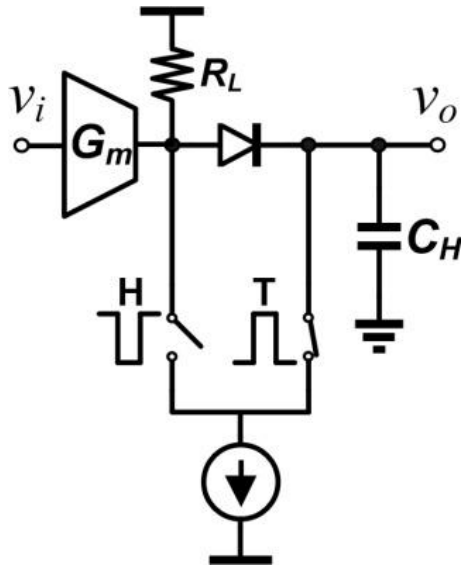
Diode bridge: [1]

- ☺ Wide bandwidth
- ☹ Linearity
- ☹ Dynamic Range



Switched Emitter Follower (SEF): [2]

- ☺ Good linearity
- ☺ Better dynamic range
- ☹ Stability issues with EF



Base-collector diode:

- ☺ Widest bandwidth
- ☺ Good linearity
- ☺ Highest dynamic range
- ☺ No stability issues
- ☺ Flat AC response

[1] J. C. Jensen and L. E. Larson, "A broadband 10-GHz track-and-hold in Si/SiGe HBT technology," IEEE JSSC, Mar. 2001.
[2] S. Shahramian, A. C. Carusone and S. P. Voinigescu, "Design Methodology for a 40-GSamples/s Track and Hold Amplifier in 0.18-μm SiGe BiCMOS Technology," IEEE JSSC, Oct. 2006.

Key Design Features

Track & hold switch: base-collector diode

lower R_{on}, lower C_{off} than HBT e-b junction

minority carrier storage time approximately equal to base transit time

Common reports in the literature:

switch voltage swings set very small and fast,

but high IP3 only for $f_{signal} << f_{Nyquist}$

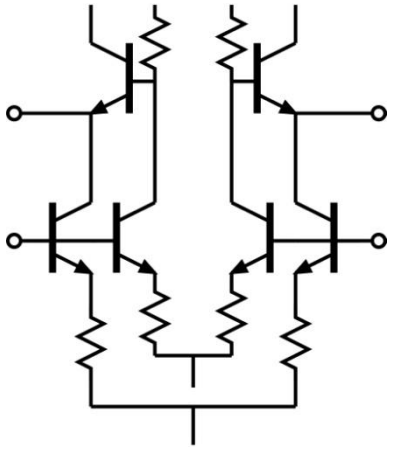
Real-world design requires:

switch voltages set for high IP3 with Nyquist-frequency input

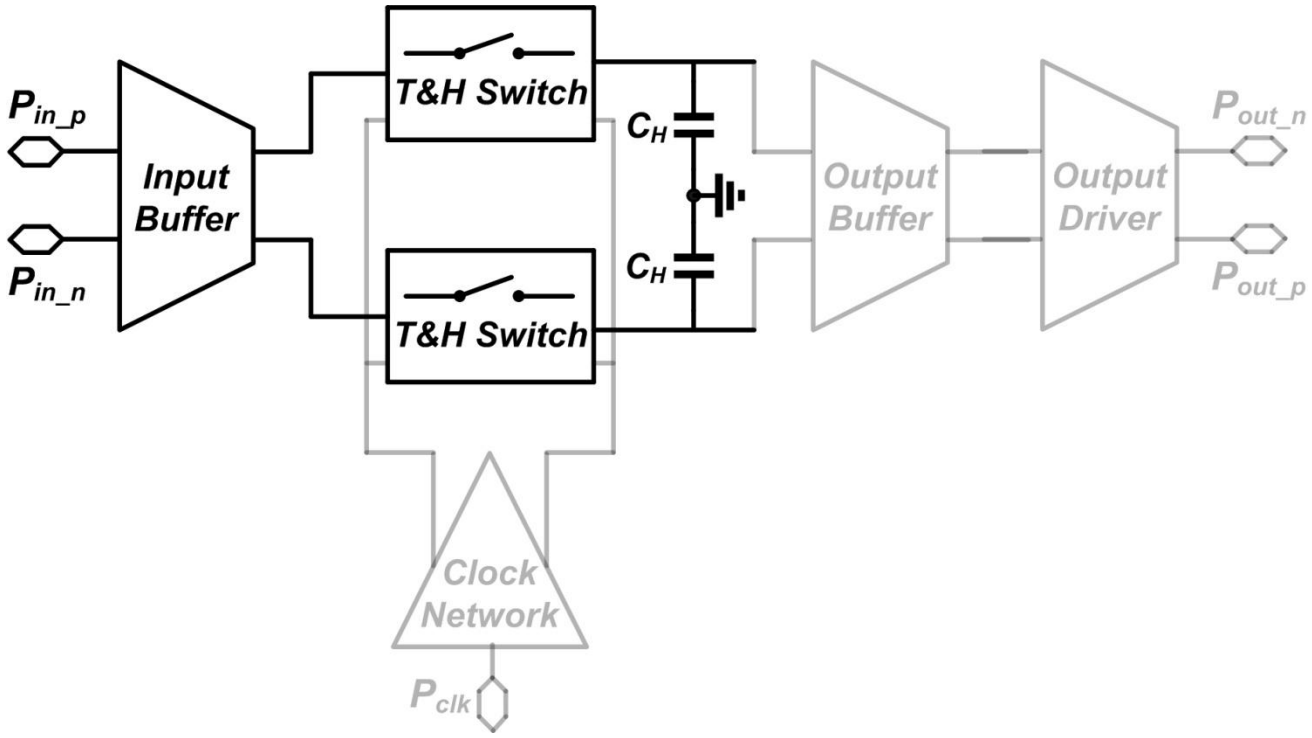
Linearization of input buffer for high IP3

cubic feedforward path cancels

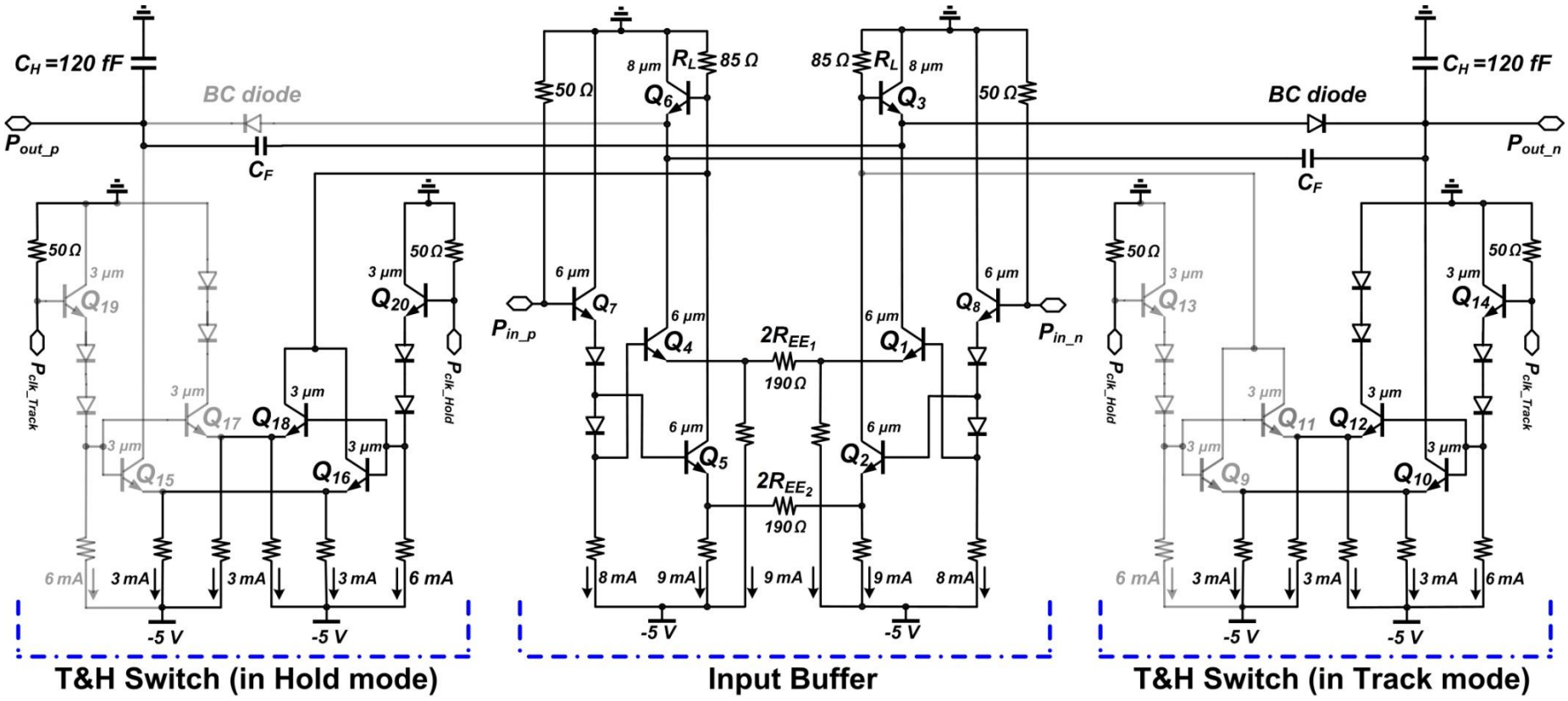
IM3 from differential pair



Input Buffer & TH Switch



Input Buffer & TH Switch



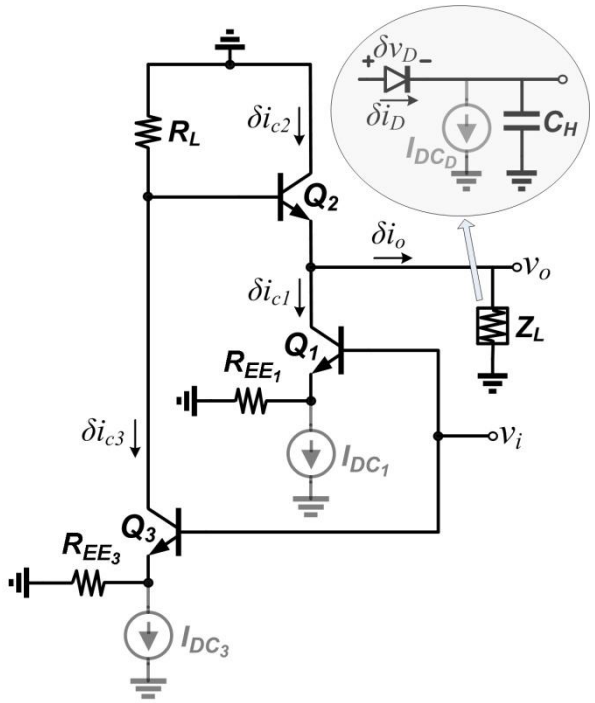
Nonlinearity Derivation - I

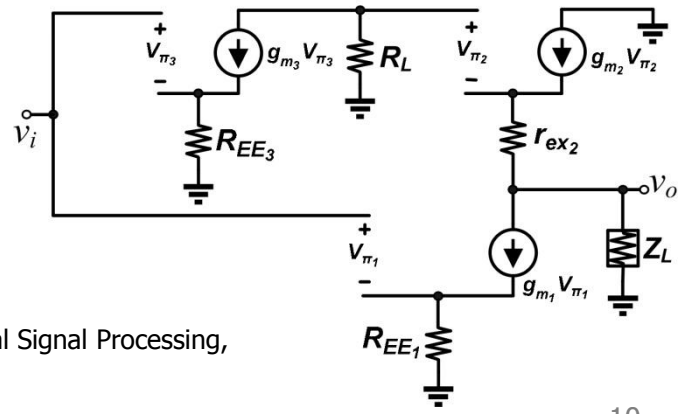
$$v_o(t) \approx \alpha_0 + \alpha_1 v_i(t) + \alpha_2 v_i^2(t) + \alpha_3 v_i^3(t), \qquad (1)$$

$$v_i(t) = V_p \sin \omega t$$

$$HD_3 = \frac{1}{4}\frac{\alpha_3}{\alpha_1} V_P^2 \qquad [1]$$

$$\alpha_1 = \frac{v_o}{v_i} = \frac{-Z_L}{Z_L + r_{ex_2} + 1/g_{m_2}} \left[\frac{r_{ex_2} + 1/g_{m_2}}{R_{EE_1} + 1/g_{m_1}} + \frac{R_L}{R_{EE_3} + 1/g_{m_3}} \right] \qquad (3)$$





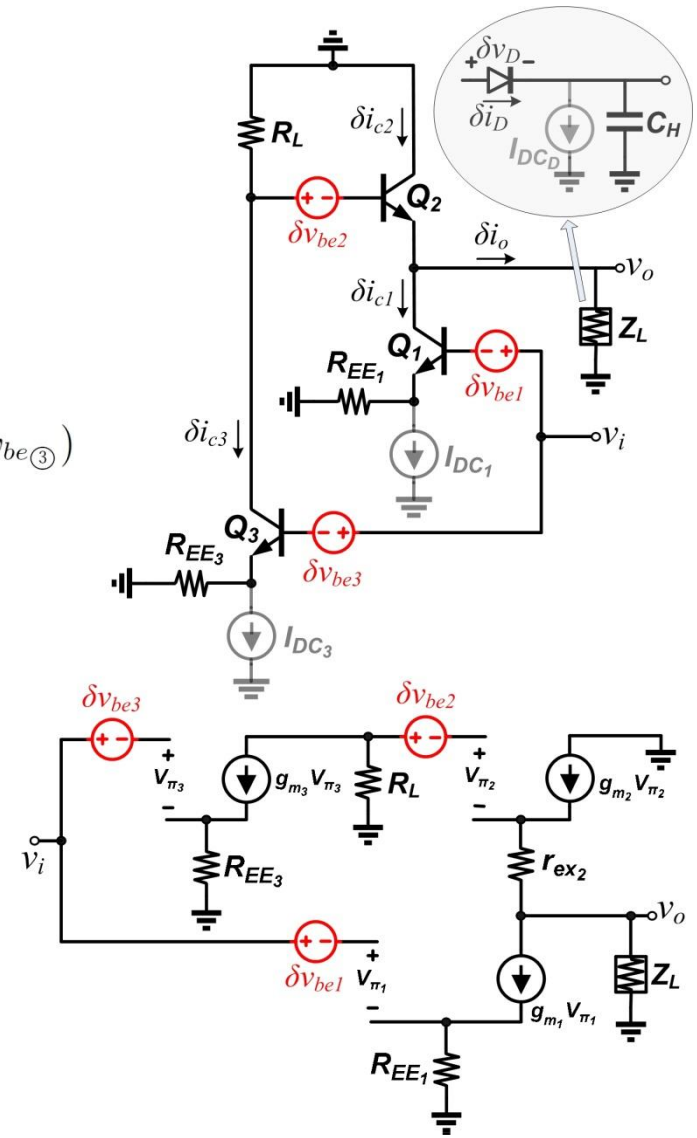
[1] W. Sansen, "Distortion in Elementary Transistor Circuits," IEEE TCAS-II: Analog and Digital Signal Processing, vol. 46, no. 3, pp. 315-325, Mar 1999.

Nonlinearity Derivation-II

$$
\begin{cases}
\delta i_{c1} = \dfrac{1/g_{m_1}}{R_{EE_1}+1/g_{m_1}}\delta v_i, \\
\delta i_{c3} = \dfrac{1/g_{m_3}}{R_{EE_3}+1/g_{m_3}}\delta v_i, \\
\delta i_o = \dfrac{-1}{Z_L+r_{ex_2}+1/g_{m_2}}\left[\dfrac{r_{ex_2}+1/g_{m_2}}{R_{EE_1}+1/g_{m_1}}+\dfrac{R_L}{R_{EE_3}+1/g_{m_3}}\right]\delta v_i, \\
\delta i_{c2} = \delta i_{c1} + \delta i_o.
\end{cases} \tag{4}
$$

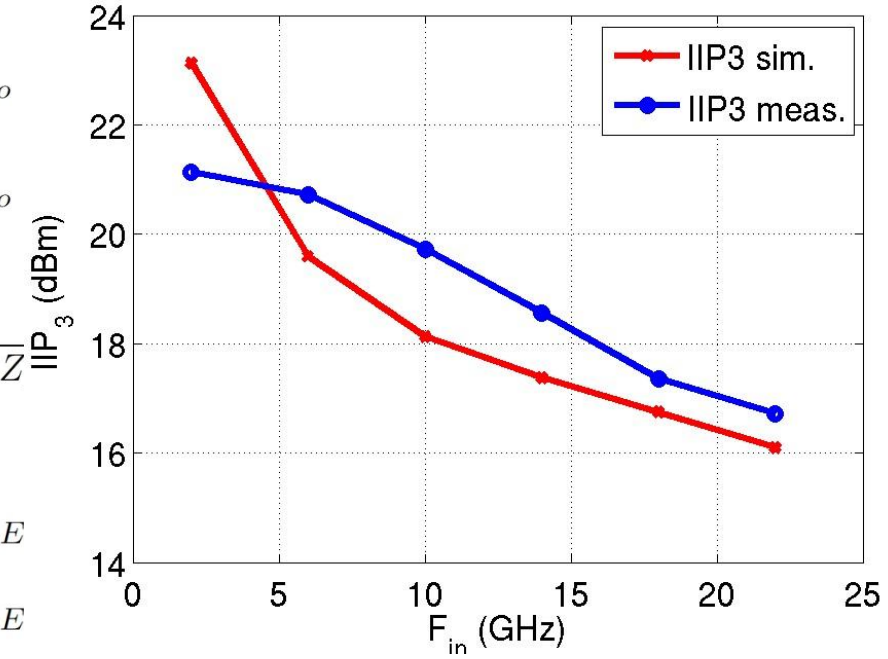
$$
\begin{cases}
\delta v_{be_1} = \left(\dfrac{V_T}{I_{DC_1}}\right)\delta i_{C1} - \left(\dfrac{V_T}{2I_{DC_1}^2}\right)\delta i_{C1}{}^2 + \left(\dfrac{V_T}{3I_{DC_1}^3}\right)\delta i_{C1}{}^3 \text{ cubic terms } (\delta v_{be③}) \\
\delta v_{be_2} = \left(\dfrac{V_T}{I_{DC_2}}\right)\delta i_{C2} - \left(\dfrac{V_T}{2I_{DC_2}^2}\right)\delta i_{C2}{}^2 + \left(\dfrac{V_T}{3I_{DC_2}^3}\right)\delta i_{C2}{}^3 \\
\delta v_{be_3} = \left(\dfrac{V_T}{I_{DC_3}}\right)\delta i_{C3} - \left(\dfrac{V_T}{2I_{DC_3}^2}\right)\delta i_{C3}{}^2 + \left(\dfrac{V_T}{3I_{DC_3}^3}\right)\delta i_{C3}{}^3
\end{cases} \tag{5}
$$

$$
\begin{cases}
\delta v_{be_1③} = \left(\dfrac{V_T}{3I_{DC_1}^3}\right)\left(\dfrac{1/g_{m_1}}{R_{EE_1}+1/g_{m_1}}\right)^3 \delta v_i^3 \\
\delta v_{be_2③} = \left(\dfrac{V_T}{3I_{DC_2}^3}\right)\left[\dfrac{1/g_{m_1}}{R_{EE_1}+1/g_{m_1}} - \dfrac{1}{Z_L+r_{ex_2}+1/g_{m_2}} \times \right. \\
\qquad \left. \left[\dfrac{r_{ex_2}+1/g_{m_2}}{R_{EE_1}+1/g_{m_1}}+\dfrac{R_L}{R_{EE_3}+1/g_{m_3}}\right]\right]^3 \delta v_i^3 \\
\delta v_{be_3③} = \left(\dfrac{V_T}{3I_{DC_3}^3}\right)\left(\dfrac{1/g_{m_3}}{R_{EE_3}+1/g_{m_3}}\right)^3 \delta v_i^3
\end{cases} \tag{6}
$$

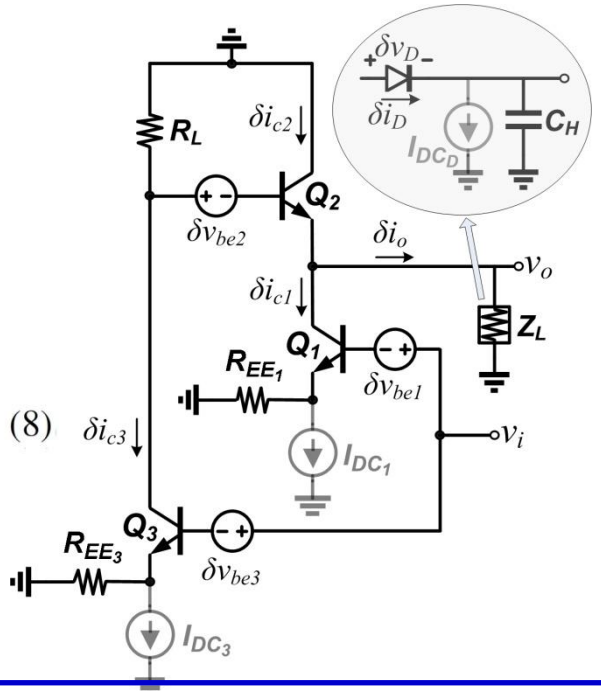


Nonlinearity Derivation - III

$$\begin{cases} \delta v_o = \dfrac{Z_L}{Z_{\quad} + r_{\quad} + 1/g_{\quad}} \times \dfrac{r_{ex_2} + 1/g_{m_2}}{R_{\quad} + 1/g_{\quad}} \delta v_{be_1}, \\ \delta v_o \\ \delta v_o \end{cases}$$



$$\delta v_o = \frac{1}{Z} \left[\frac{R_L}{R_{EE} + 1/g_{m_3}} \delta v_{be_3} \right] \quad (8)$$



$$R_{EE}$$

$$R_{EE}$$

$$I_{DC_1} = I_{DC}, \qquad I_{DC_2} = k_2 I_{DC}, \qquad I_{DC_3} = k_3 I_{DC}, \quad (9)$$

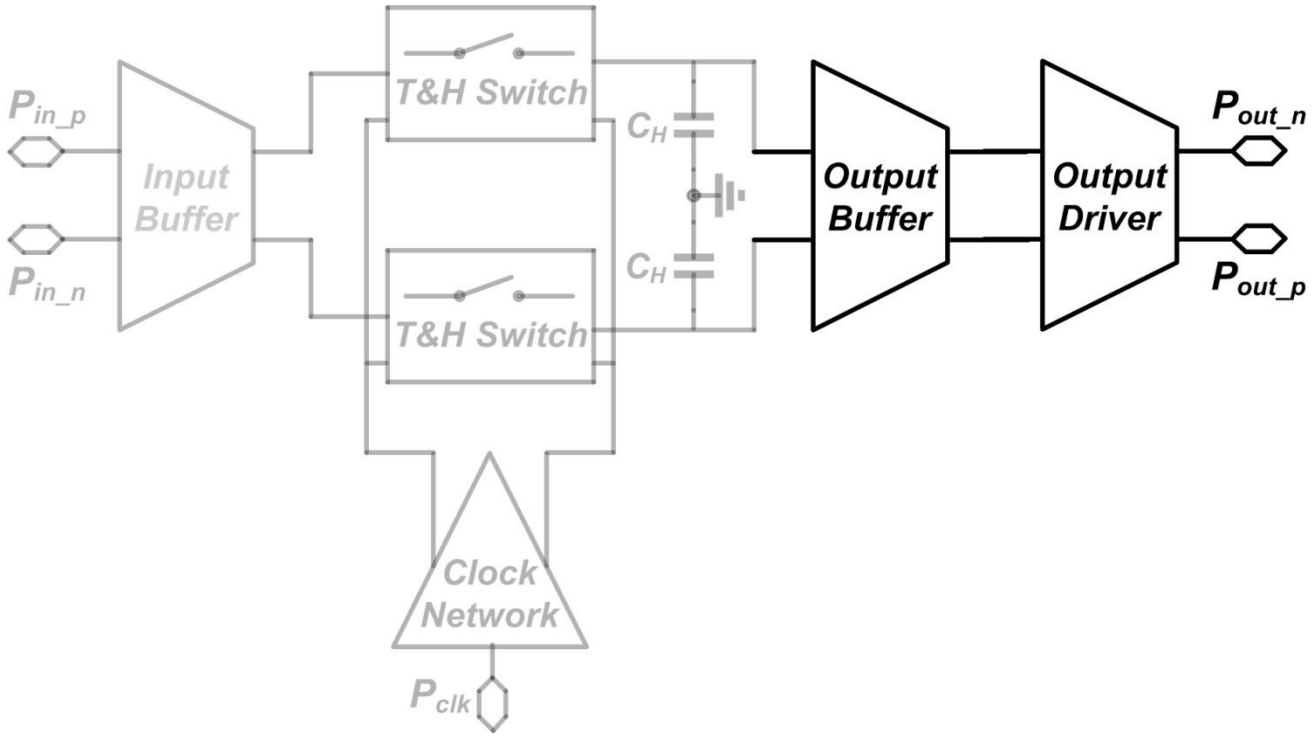
$$g_{m_1} = g_m, \qquad g_{m_2} = k_2 g_m, \qquad g_{m_3} = k_3 g_m.$$

$$k_1 = k_2 = k_3 = 1 \quad ,$$

$$R_{EE} = R_L + r_{ex_2} + 1/g_m$$

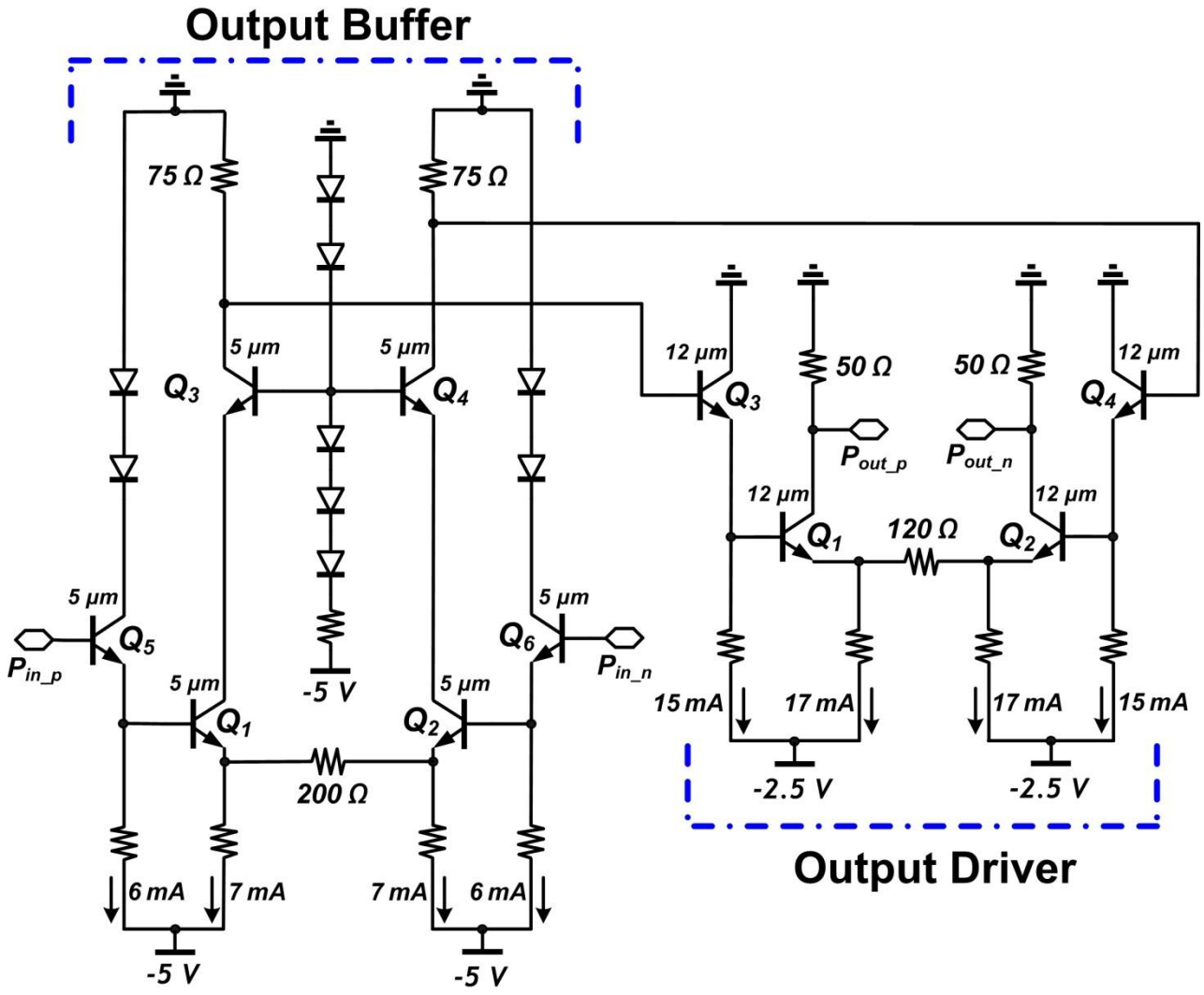
$$IM_3 \approx \frac{-V_T^4 V_P^2}{4 I_{DC}^6 R_{EE}^3 \left(r_{ex_2} + \dfrac{1}{k_2 g_m} + \dfrac{R_L}{k_1} \right)} \times \left[\frac{R_{EE}}{k_2^3} \left(\frac{g_m \left(\dfrac{R_L}{k_1} + r_{ex_2} + \dfrac{1}{k_2 g_m} \right)}{Z_L + r_{ex_2} + \dfrac{1}{k_2 g_m}} - 1 \right)^3 + \frac{R_L}{K_3^6 k_1^4} + r_{ex_2} + \frac{1}{k_2 g_m} \right] \quad (10)$$

Output Buffer & Output Driver

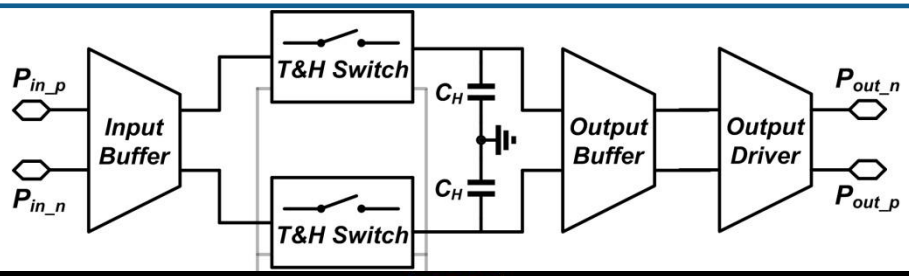


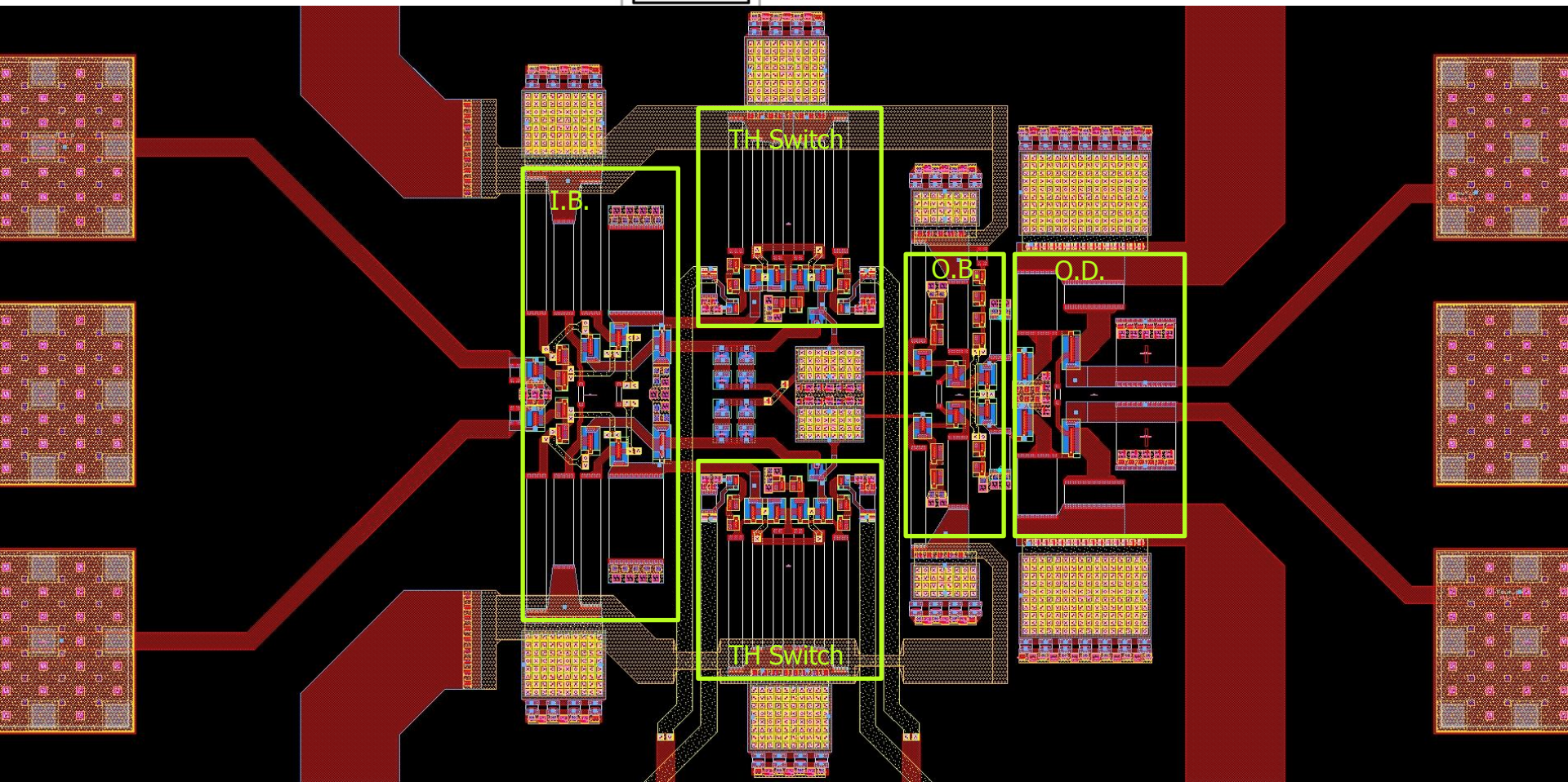
Output Buffer & Output Driver

- Output buffer should always be **on** in Sample & Hold circuit
- Output stage needs to be designed linear enough not to affect total nonlinearity of the circuit

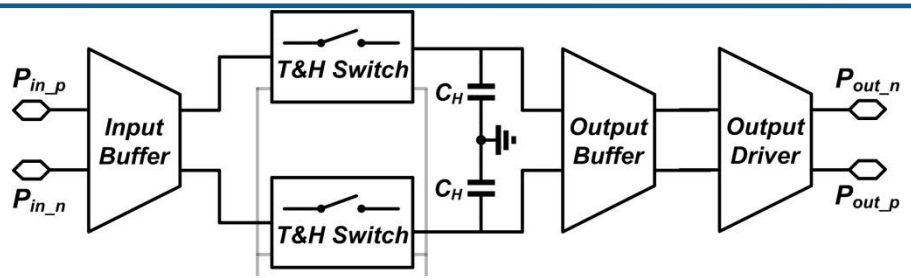


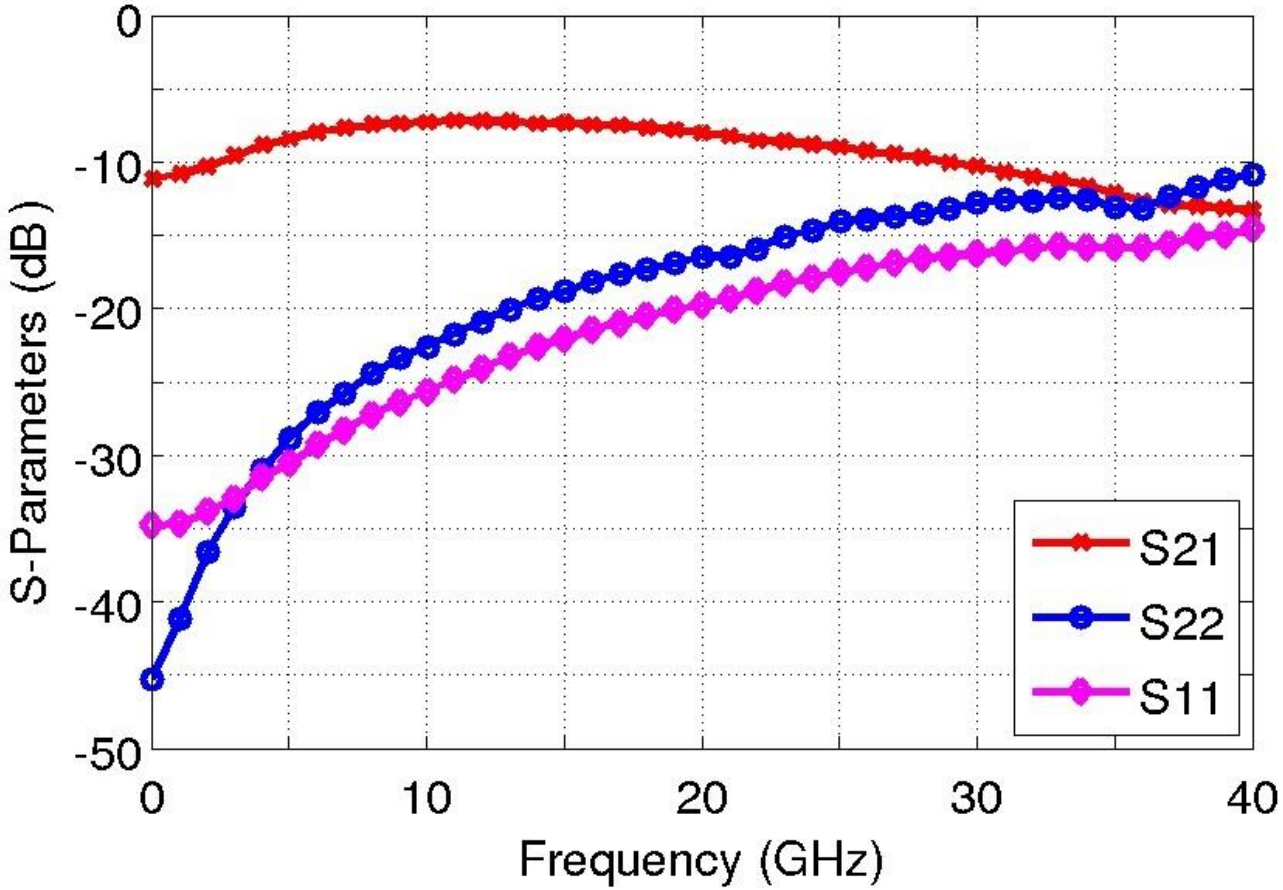
Layout (Signal path)



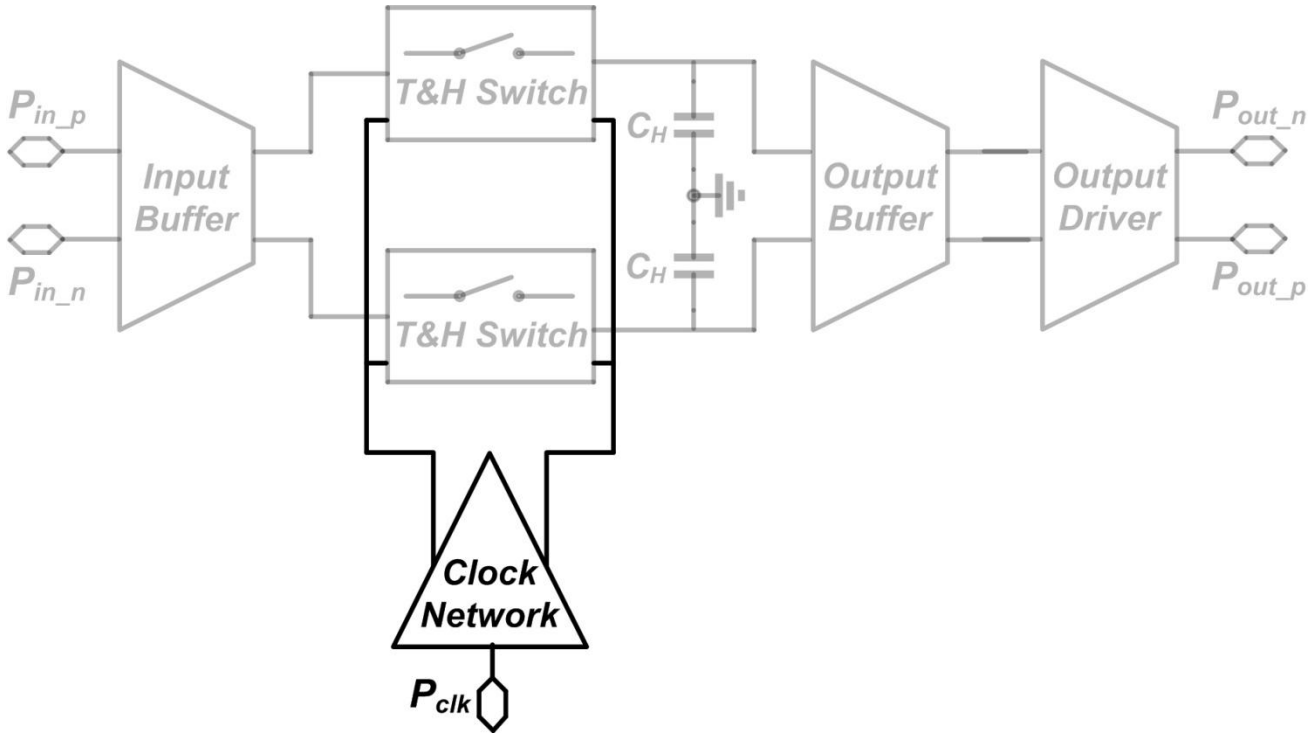


S-parameters measurement

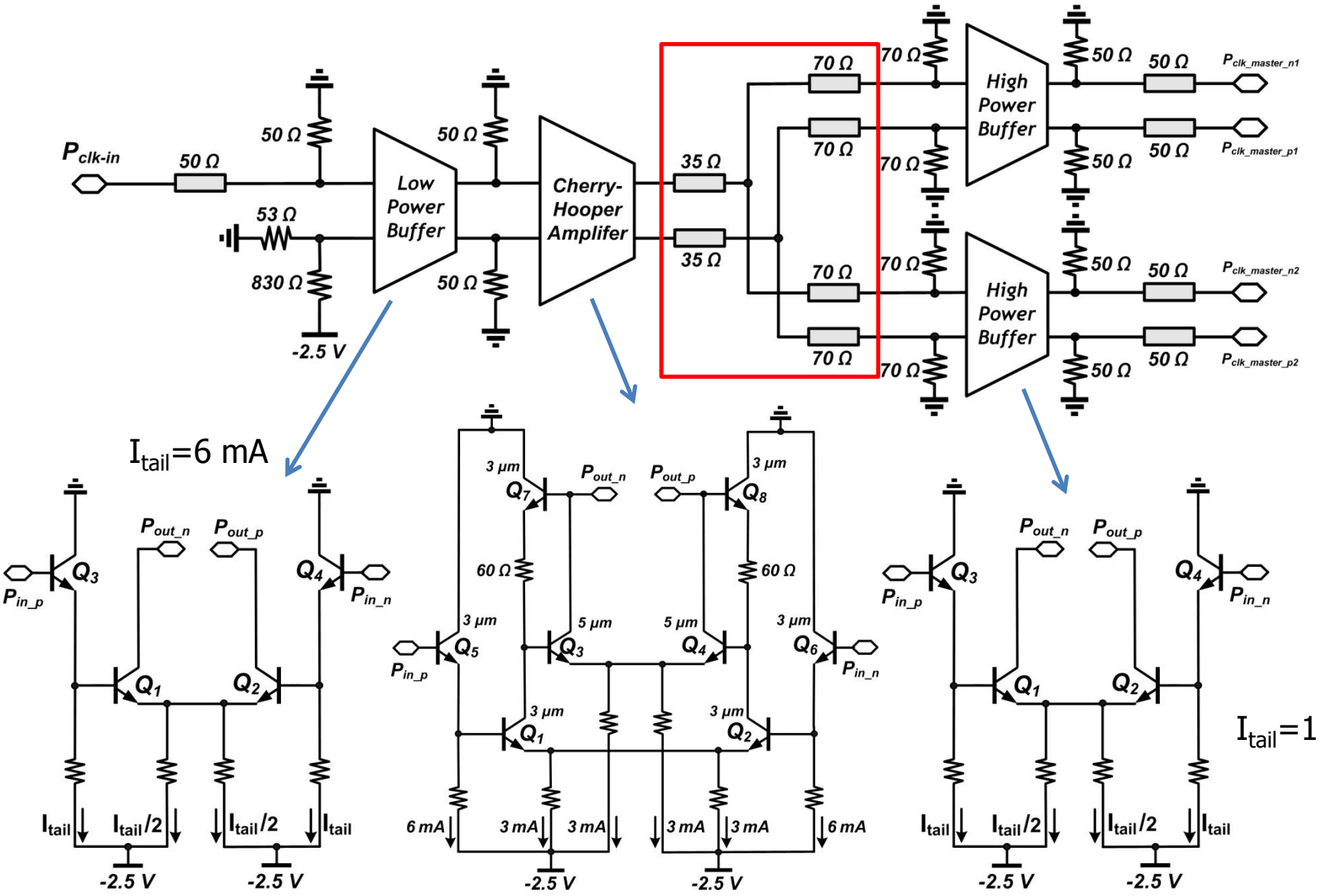




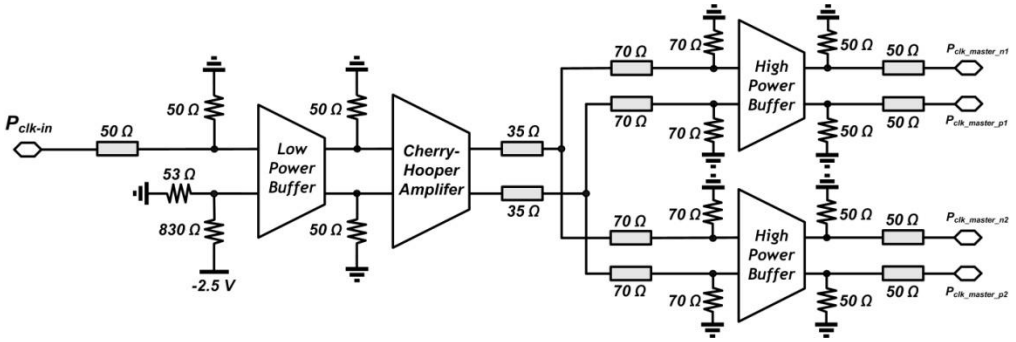
Clock Distribution Circuit

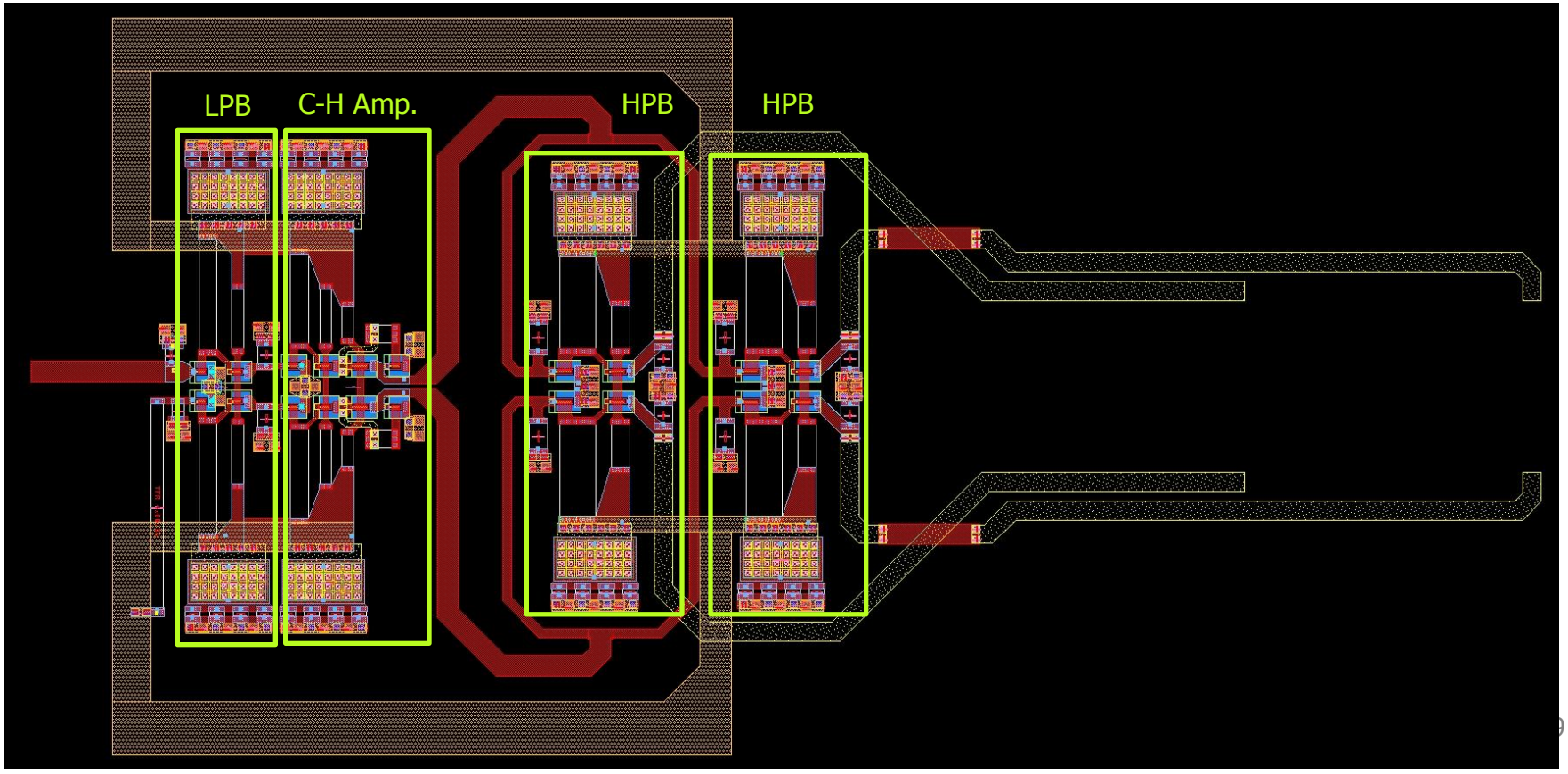


Clock Distribution Circuit



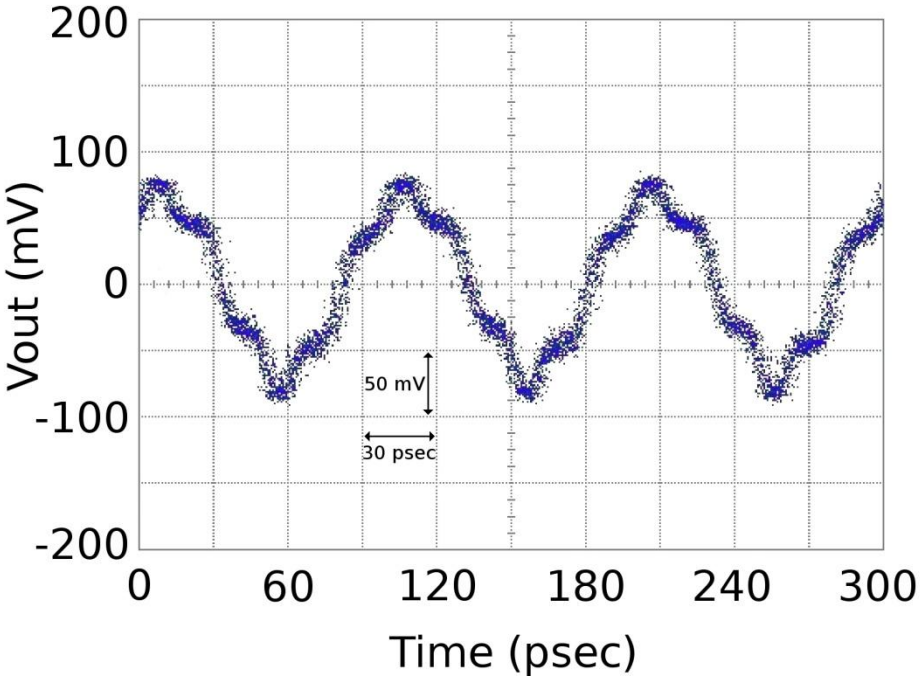
Clock Distribution Circuit - layout



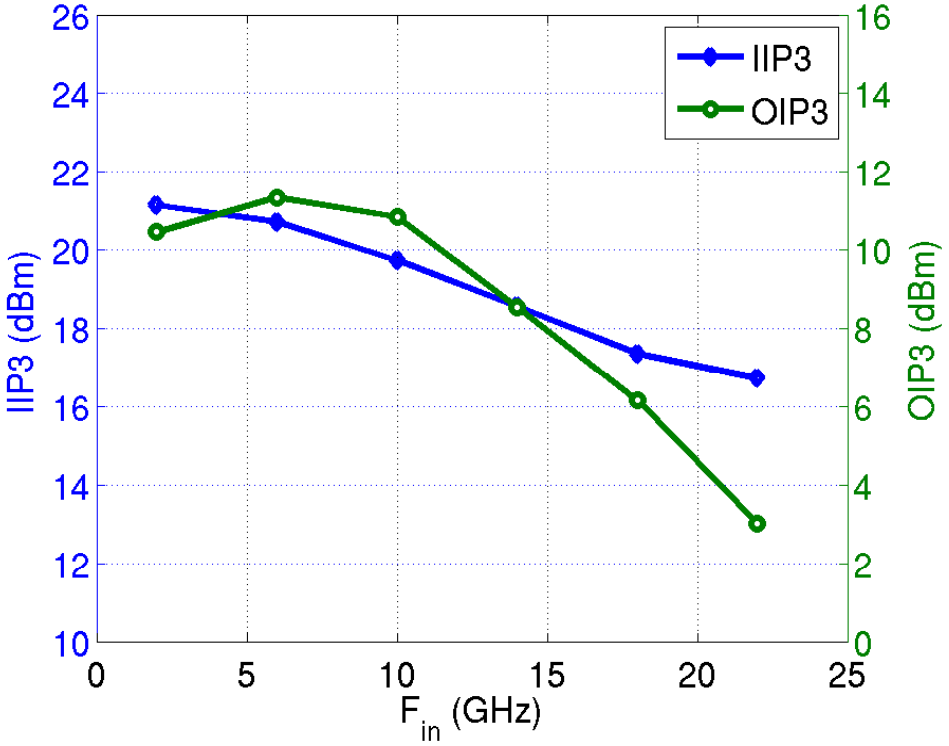


Transient and Linearity Measurements

10 GHz RF input signal with a 50 GHz clock

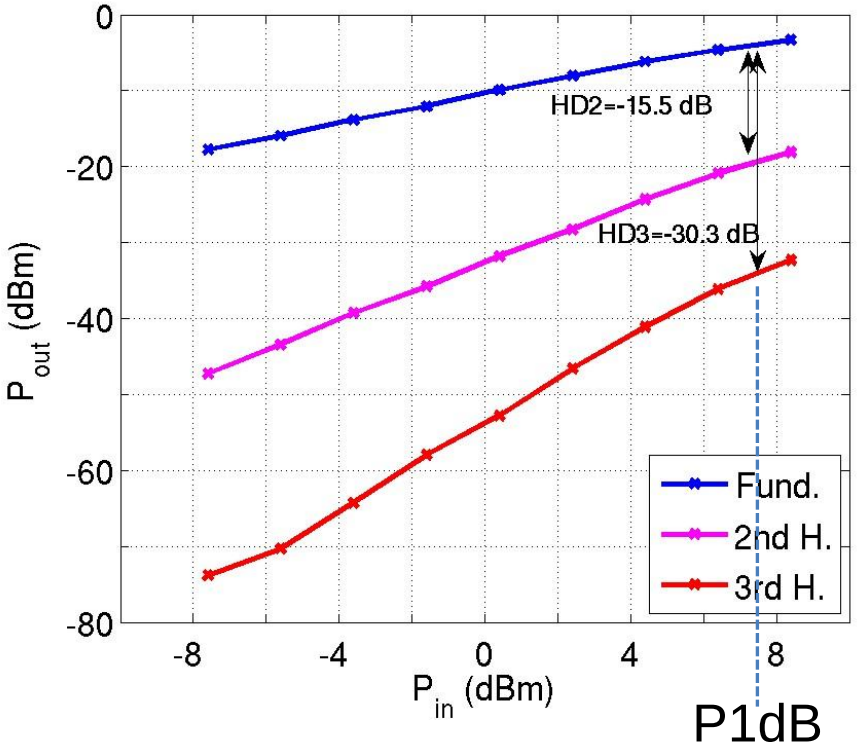


IIP3 & OIP3 vs Fin for Fclk = 50GHz

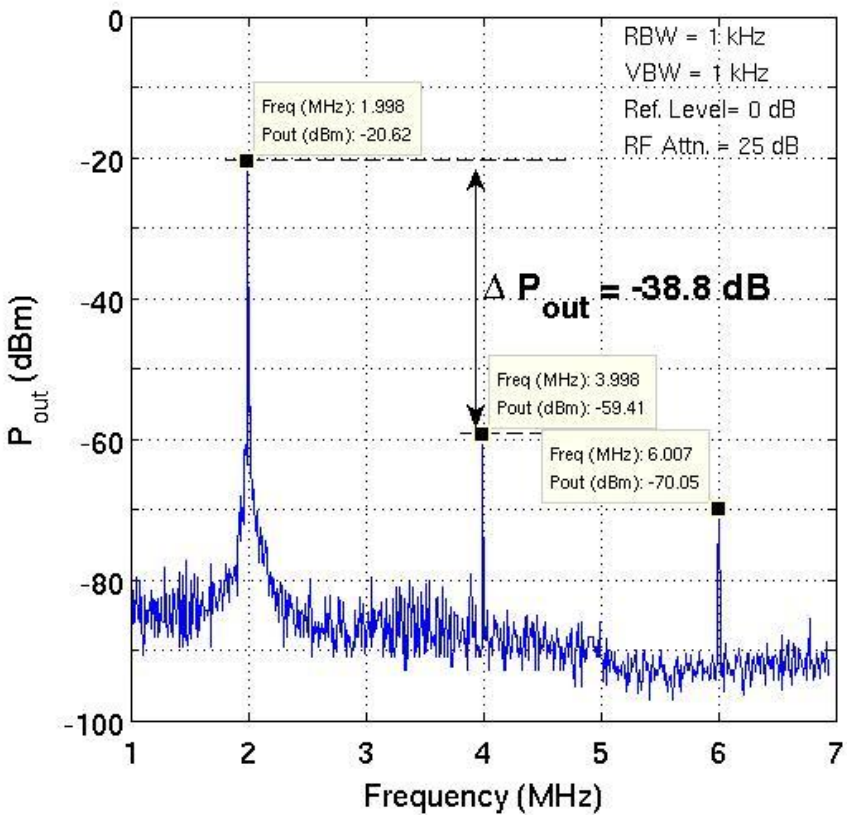


THD and Beat test Measurements

Measured HD_2 and HD_3



40.002 GHz input signal is being sampled by 40 GSamples/s sampling rate.



Comparison with the State of the Art Works

	Sample Rate (GS/s)	BW (GHz)	Input Range Output Range	IIP3 @f_{in}/f_s (dBm @ GHz/GHz)	Power (mW)	V_{Supply} (V)	Die-Size (mm^2)	Process f_t
[1]	30	7	$-12\,dBm$ $< 150\,mV_{pp}$	1@5/30 0@9/30	270	1.8	1.0	CMOS
[2]	40	43	$< -8\,dBm$ $500\,mV_{pp}$	8@6/40 0@19/40	540	3.6	1.0×1.1	SiGe HBT 160 GHz
[3]	50	42	0 dBm N.A.	21@30/50	640	4, 3.3	1.28×1.15	SiGe BiCMOS
[4]	20	20	$500\,mV_{pp}$ $500\,mV_{pp}$	16@2/20	1990	-6	1.6×1.4	InP HBT 210 GHz
[5]	40	16	$1000\,mV_{pp}$ $< 100\,mV_{pp}$	15.6@10/40	560	5.5	1.8×1.0	SiGe HBT 200 GHz
[6]	40	27	7 dBm N.A.	N.A.	1900	-6	1.4×1.6	InP DHBT 210 GHz
This work	50	40	9 dBm $800\,mV_{pp}$	20.7@6/40 19.7@10/40 17.4@18/40 16.7@22/40	1200	$-5, -2.5$	0.875×1.075	InP HBT 400 GHz

REFERENCES

[1] S. Shahramian, S. P. Voinigescu and A. C. Carusone, "A 30-GS/sec Track and Hold Amplifier in 0.13-μm CMOS Technology," in *Proceeding of IEEE Custom Integrated Circuits Conference (CICC)*, pp. 493-496, Sep. 2006.

[2] S. Shahramian, A. C. Carusone and S. P. Voinigescu, "Design Methodology for a 40-GSamples/s Track and Hold Amplifier in 0.18-μm SiGe BiCMOS Technology," *IEEE Journal of Solid State Circuits*, vol. 41, No. 10, pp. 2233-2240, Oct. 2006.

[3] J. Lee, Y. Baeyens, J. Weiner and Y. K. Chen, "A 50GS/s Distributed T/H Amplifier in 0.18μm SiGe BiCMOS," in *Proceeding of IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 466-616, Feb. 2007.

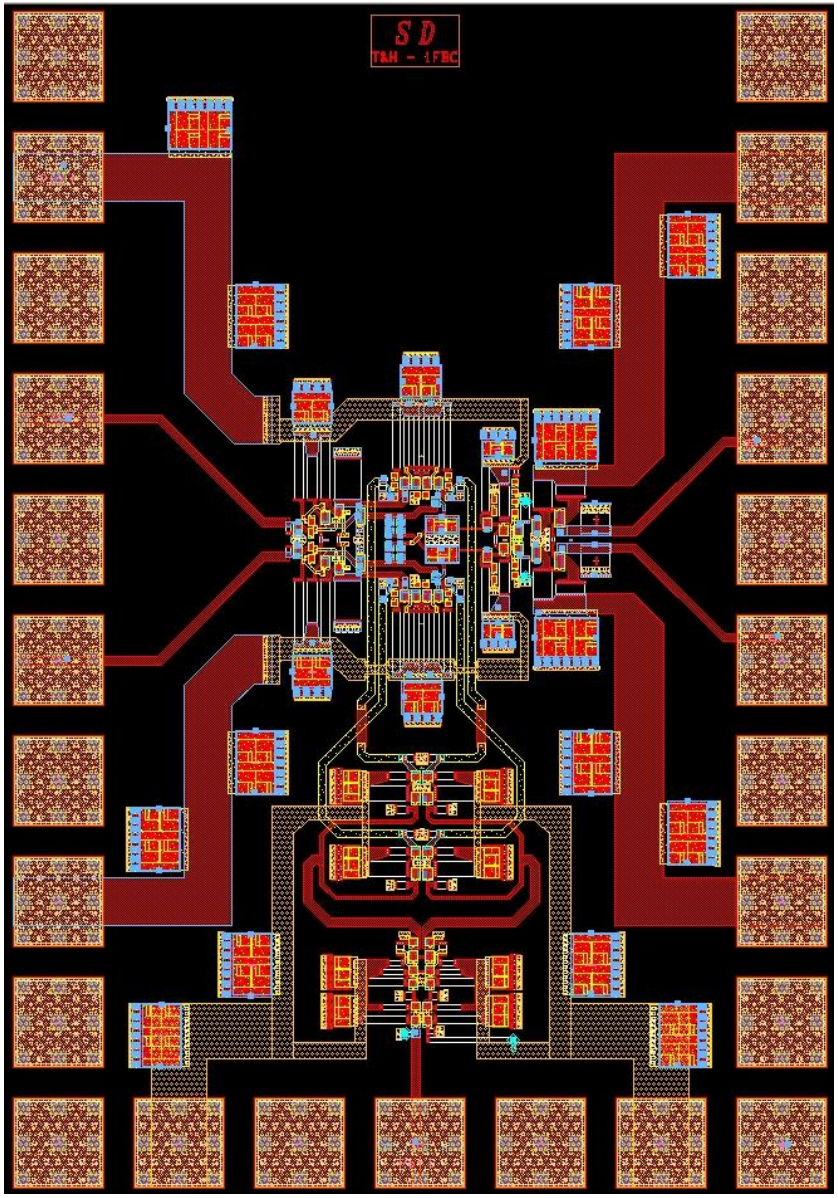
[4] Y. Bouvier, A. Konczykowska, A. Ouslimani, F. Jorge, M. Riet and J. Godin, "A 20-GSamples/s Track-Hold Amplifier in InP DHBT technology," in *Proceeding of European Microwave Integrated Circuit Conference (EuMIC)*, pp. 1-4, Oct. 2007.

[5] X. Li, W. M. L. Kuo and J. D. Cressler, "A 40 GS/s SiGe track-and-hold amplifier," in *Proceeding of the Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, pp. 1-4, Oct. 2008.

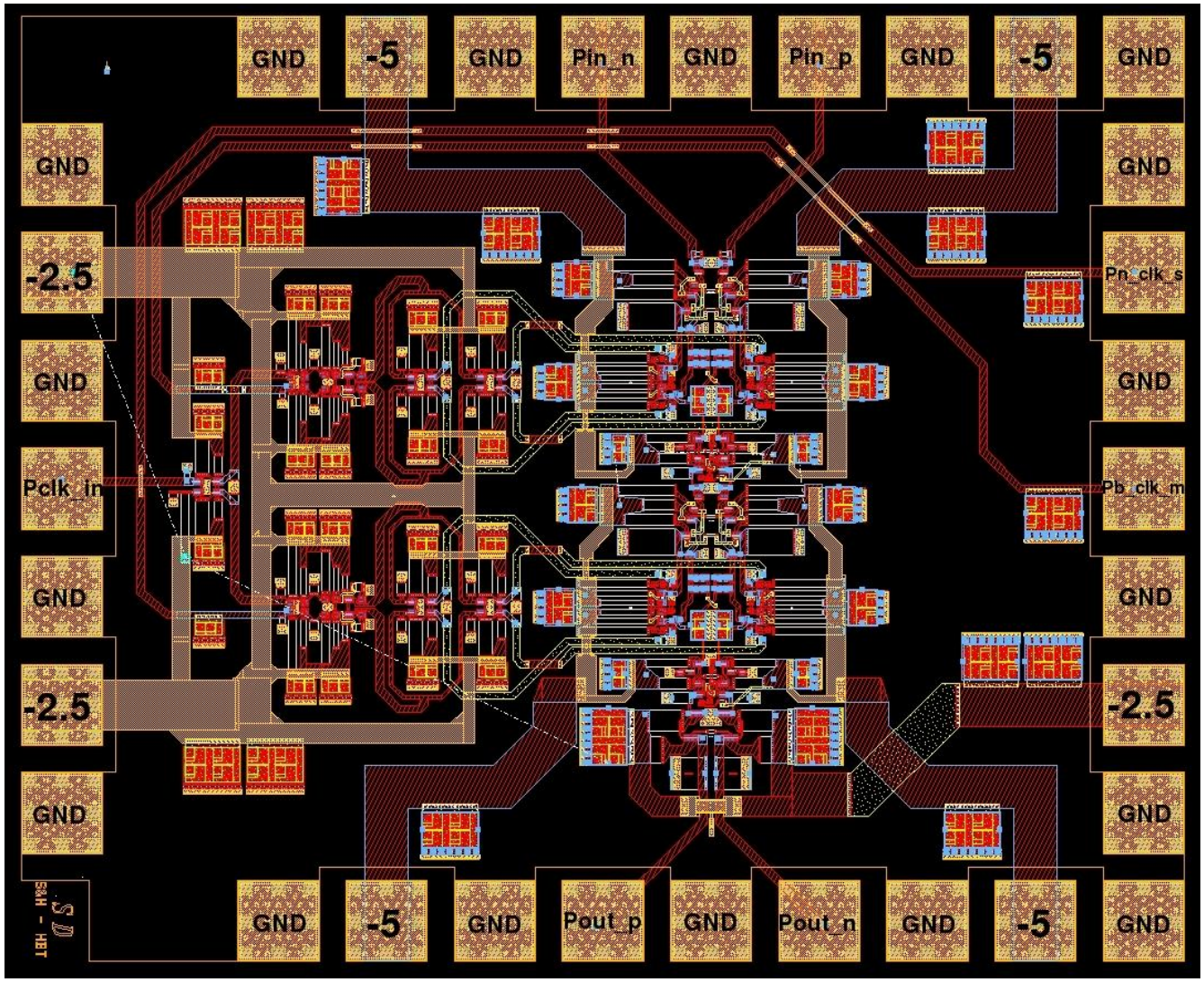
[6] Y. Bouvier, A. Ouslimani, A. Konczykowska and J. Godin, "A 40 Gsamples/s InP-DHBT Track-&-Hold Amplifier," in *Proceeding of European Microwave Integrated Circuit Conference (EuMIC)*, pp. 61-64, Sep. 2010.

Questions?

T&H Chip layout



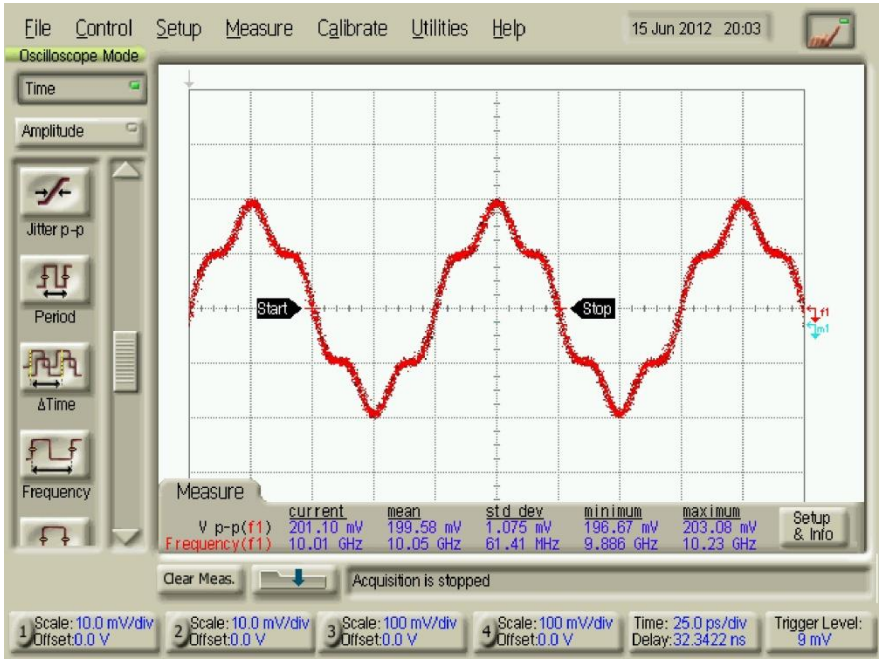
S&H Chip layout



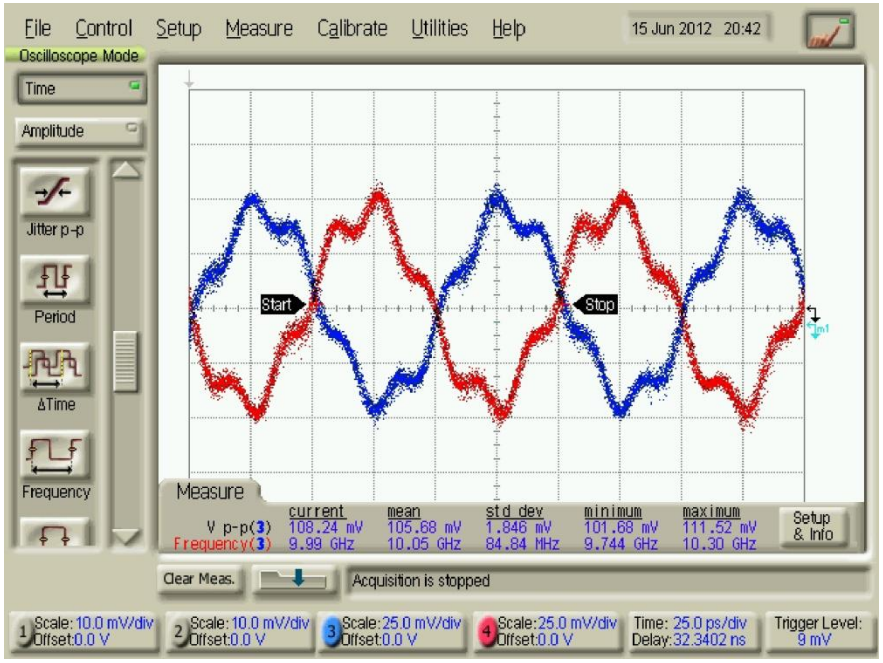
Sample & Hold Transient waveforms

- 10 GHz RF input signal is being sampled by a 50 GHz clock

Differential



Single-ended

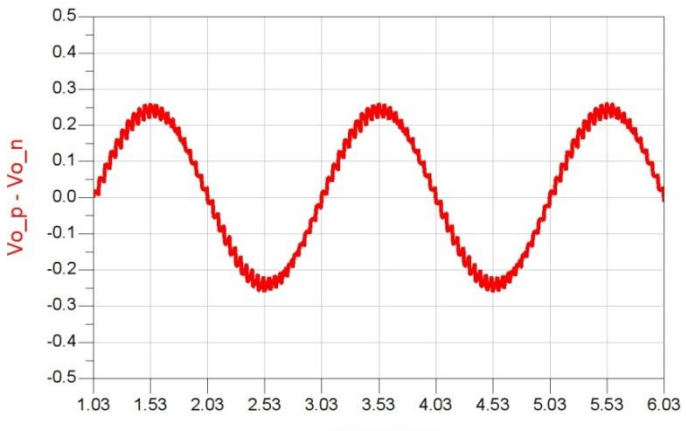


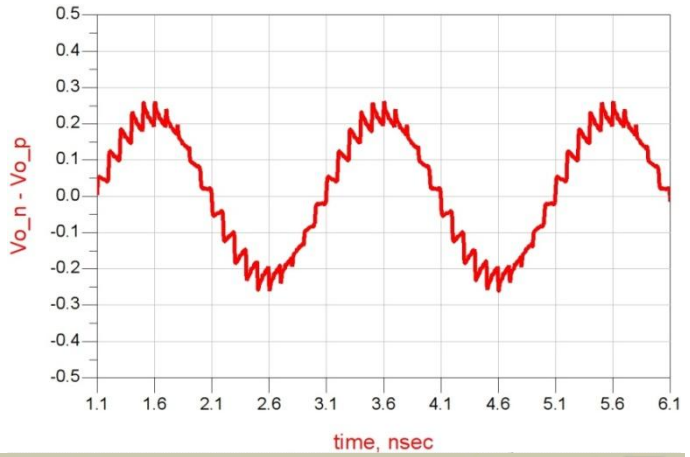
Sample & Hold Beat frequency test

Fin=20.5 GHz, Fclk=20 GHz

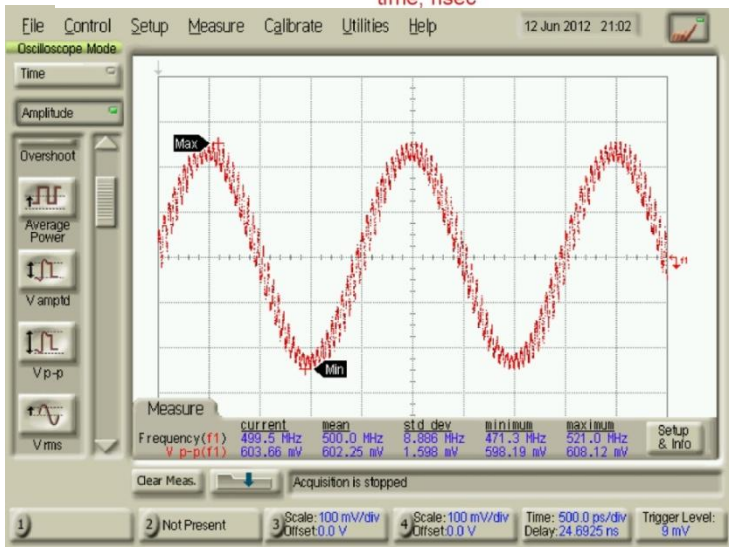
Fin=20.5 GHz, Fclk=10 GHz

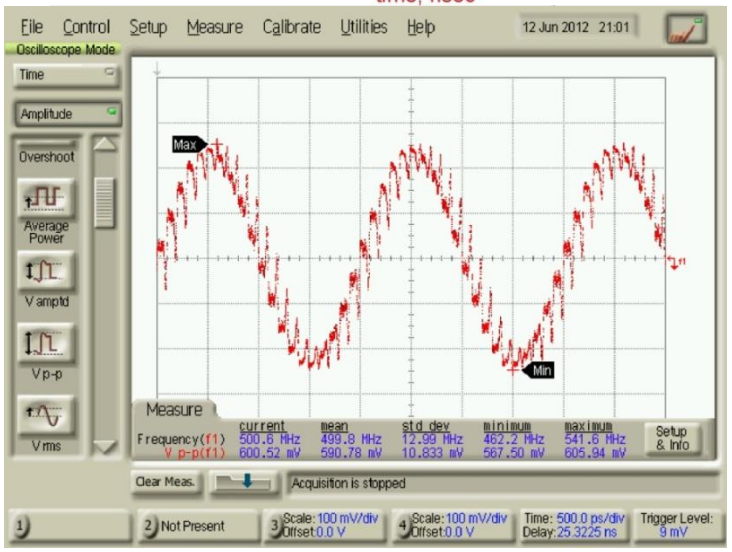
Simulation





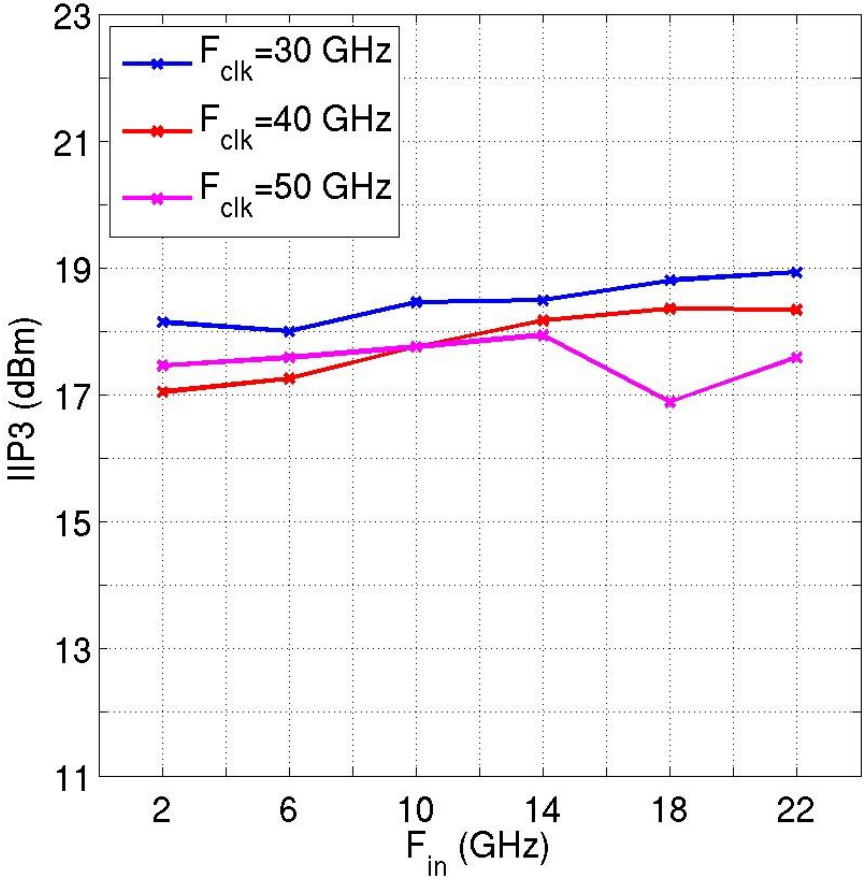
Experiment

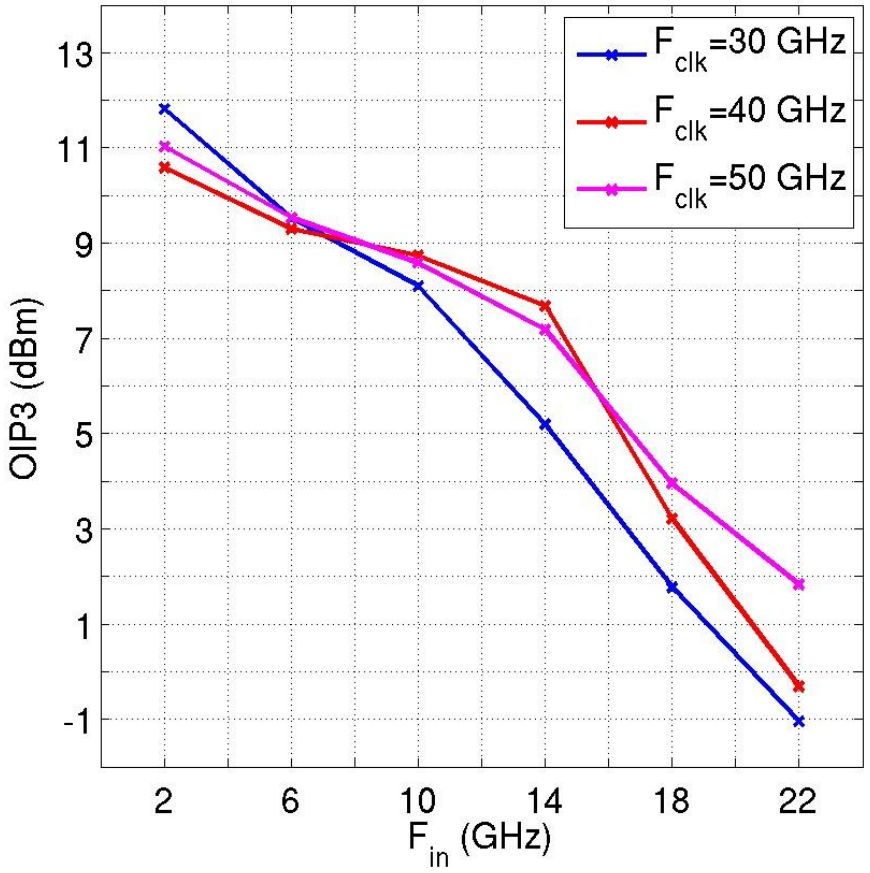




Sample & Hold Linearity Measurements

Calculated ENOB using simulated noise figure of 20dB is more than 6bits.





Base-Collector Diode modeling - I

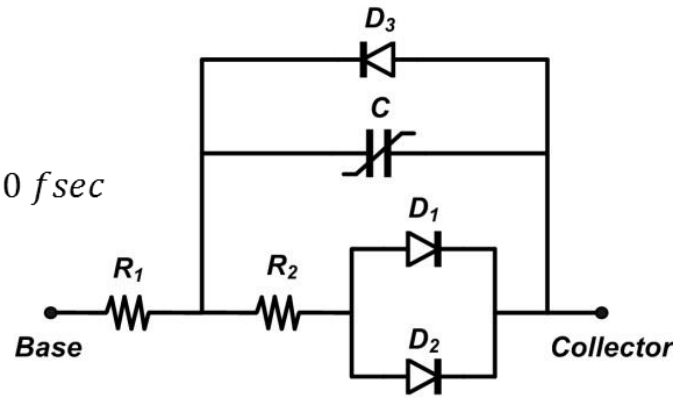
$W = 0.6\mu m\,, \quad L_B = 2.4\mu m$

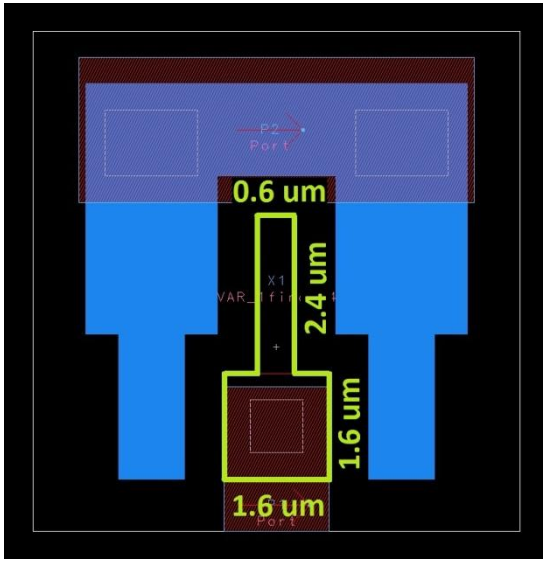
$Area = 1.6\mu m \times 1.6\mu m + W \times L_B$

D_1: $I_{S1} = \frac{2.45e-10}{Area}, \quad N = 1.9, \quad T_t = 50\ fsec$

D_2: $I_{S2} = \frac{1.47e-12}{Area}, \quad N = 1.3$

D_3: $I_{S3} = \frac{2.38e-9}{Area}, \quad N = 20.7$





$R_1 = \frac{\rho_{cp}}{Area} = \frac{6e-12}{Area}$

$R_2 = \frac{78e-12}{Area}, \qquad R_1 + R_2 = 21\Omega.$

$$C = \frac{a_5 {V_C}^5 + a_4 {V_C}^4 + a_3 {V_C}^3 + a_2 {V_C}^2 + a_1 {V_C}^1 + a_0}{Area}$$

$a_5 = -0.007\ fF$

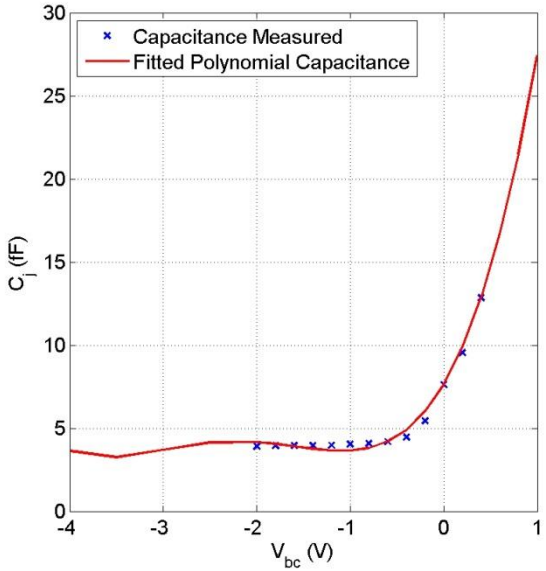
$a_4 = 0.209\ fF$

$a_3 = 2.345\ fF$

$a_2 = 7.705\ fF$

$a_1 = 9.557\ fF$

$a_0 = 7.637\ fF$

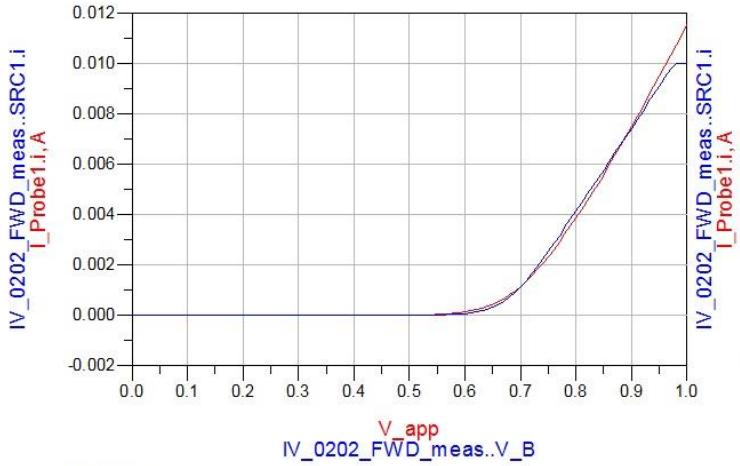


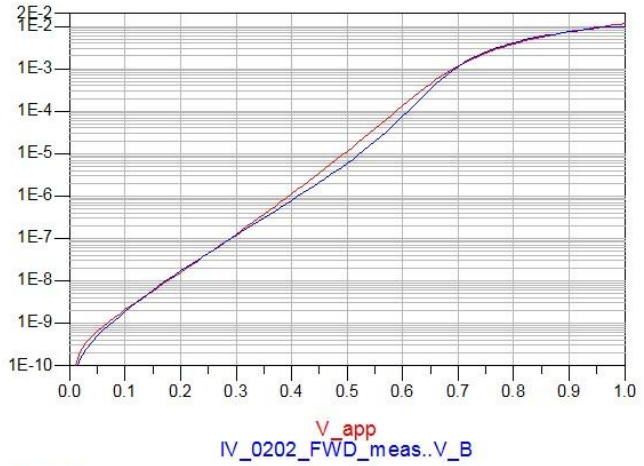
Base-Collector Diode modeling - II

Linear Scale

Log Scale

I-V Characteristic
Forward biased





I-V Characteristic
Reverse biased